TEXAS INSTRUMENTS

AHC/AHCT, HC/HCT, and LV CMOS Logic

Performance Budgeting for 5-V and 3.3-V Systems

Data Book

1996

Advanced System Logic Products

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AHC/AHCT, HC/HCT, and LV CMOS Logic Data Book

Performance Budgeting for 5-V and 3.3-V Systems

TEXAS INSTRUMENTS

INTRODUCTION

High-speed CMOS (HCMOS) has earned its place as the number-one-selling logic family by delivering low power and low noise at a low price. HCMOS is here to stay, but for designers wanting to keep the features of HCMOS while achieving higher speeds, Texas Instruments (TI) offers the newer and faster advanced high-speed CMOS (AHC) and low-voltage (LV) families with attractive low pricing.

AHC

- Three times faster than HCMOS
- 50% of the static power consumption of HCMOS
- Noise performance similar to HCMOS
- Supply voltage 2.0 V to 5.5 V (optimized to 5 V with specification for 3.3 V, 5-V input tolerant for AHC devices)
- Available in both CMOS (AHC) and TTL (AHCT) switching levels

AHC MicroGate – Same features as AHC with additional benefits:

- Single-gate devices (5 pin)
- Simplifies routing
- ASIC modification

AHC Widebus™ – Same features as AHC with additional benefits:

- TI introduces the first performance-budgeting 16-bit logic devices
- Lower package inductance delivers improved simultaneous-switching performance and better noise performance

HCMOS

- Low power
- Low noise
- Available in both CMOS (HC) and TTL (HCT) switching levels
- TI is committed to being the last supplier of HCMOS

LV

- Two times faster than HCMOS
- 25% of the static power consumption of HCMOS
- Noise performance similar to HCMOS
- Optimized for 3.3-V operation with specifications for 5-V operation
- Standard LVTTL switching levels

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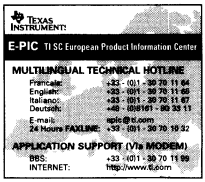

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>
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Contents

ALPHANUMERIC INDEX

INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

operating conditions and characteristics (in sequence by letter symbols)

C_i **Input capacitance**
The internal capacitance at an input of the device

C_o **Output capacitance**
The internal capacitance at an output of the device

C_{pd} **Power dissipation capacitance**
Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages): $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$

f_{max} **Maximum clock frequency**
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification

I_{CC} **Supply current**
The current into* the V_{CC} supply terminal of an integrated circuit

ΔI_{CC} **Supply current change**
The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}

I_{CEX} **Output high leakage current**
The maximum leakage current into the collector of the pulldown output transistor when the output is high and the output forcing condition V_O = 5.5 V

$I_{I(hold)}$ **Input hold current**
Input current that holds the input at the previous state when the driving device goes to a high-impedance state

I_{IH} **High-level input current**
The current into* an input when a high-level voltage is applied to that input

I_{IL} **Low-level input current**
The current into* an input when a low-level voltage is applied to that input

I_{off} **Input/output power-off leakage current**
The maximum leakage current into/out of the input/output transistors when forcing the input/output to 4.5 V and V_{CC} = 0 V

I_{OH} **High-level output current**
The current into* an output with input conditions applied that, according to the product specification, establishes a high level at the output

I_{OL} **Low-level output current**
The current into* an output with input conditions applied that, according to the product specification, establishes a low level at the output

*Current out of a terminal is given as a negative value.

GLOSSARY
SYMBOLS, TERMS, AND DEFINITIONS

I_{OZ} **Off-state (high-impedance-state) output current (of a 3-state output)**

The current flowing into* an output having 3-state capability with input conditions established that, according to the product specification, establishes the high-impedance state at the output

t_a **Access time**

The time interval between the application of a specified input pulse and the availability of valid signals at an output

t_c **Clock cycle time**

Clock cycle time is $1/f_{max}$.

t_{dis} **Disable time (of a 3-state or open-collector output)**

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state

NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or t_{PLZ}. Open-collector outputs change only if they are low at the time of disabling, so $t_{dis} = t_{PLH}$.

t_{en} **Enable time (of a 3-state or open-collector output)**

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low)

NOTE: In the case of memories, this is the access time from an enable input (e.g., $\overline{OE}$). For 3-state outputs, $t_{en} = t_{PZH}$ or t_{PZL}. Open-collector outputs change only if they are responding to data that would cause the output to go low, so $t_{en} = t_{PHL}$.

t_h **Hold time**

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is to be expected.

t_{pd} **Propagation delay time**

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level ($t_{pd} = t_{PHL}$ or t_{PLH})

t_{PHL} **Propagation delay time, high-to-low level output**

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level

t_{PHZ} **Disable time (of a 3-state output) from high level**

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined high level to the high-impedance (off) state

t_{PLH} **Propagation delay time, low-to-high level output**

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level

*Current out of a terminal is given as a negative value.

t_{PLZ} **Disable time (of a 3-state output) from low level**

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined low level to the high-impedance (off) state

t_{PZH} **Enable time (of a 3-state output) to high level**

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined high level

t_{PZL} **Enable time (of a 3-state output) to low level**

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined low level

t_{su} **Setup time**

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value, in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_w **Pulse duration (width)**

The time interval between specified reference points on the leading and trailing edges of the pulse waveform

V_{IH} **High-level input voltage**

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables

NOTE: A *minimum* is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is to be expected.

V_{IL} **Low-level input voltage**

An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables

NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is to be expected.

V_{OH} **High-level output voltage**

The voltage at an output terminal with input conditions applied that, according to product specification, establishes a high level at the output

V_{OL} **Low-level output voltage**

The voltage at an output terminal with input conditions applied that, according to product specification, establishes a low level at the output

V_{IT+} **Positive-going input threshold level**

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{IT-}

V_{IT-} **Negative-going input threshold level**

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{IT+}

EXPLANATION OF FUNCTION TABLES

The following symbols are used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
↶	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state output
a . . . h	=	the level of steady-state inputs A through H, respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$	=	complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
⎍	=	one high-level pulse
⎌	=	one low-level pulse
Toggle	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⎌, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

Among the most complex function tables are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register.

FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	H	H	H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	L	L	L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs occurs while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A is at output Q_A, data entered at B is at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D, respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

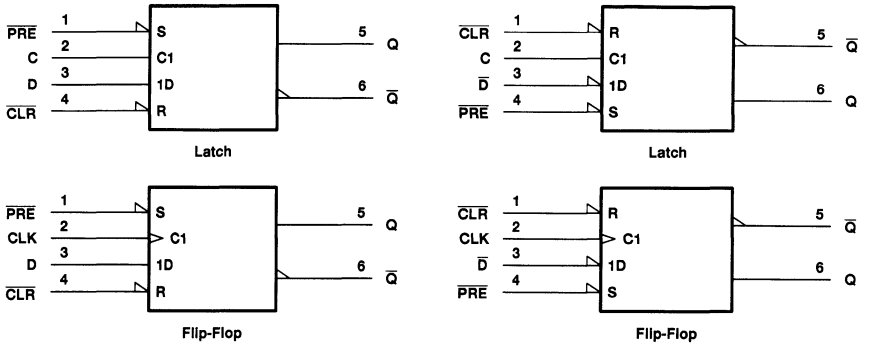
The function table functional tests do not reflect all possible combinations or sequential modes.

D FLIP-FLOP AND LATCH SIGNAL CONVENTIONS

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called preset ($\overline{PRE}$). An input that causes a $\overline{Q}$ output to go high or a Q output to go low is called clear ($\overline{CLR}$). Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active low.

The devices on several data sheets are second-source designs, and the pin-name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits $\overline{D}$ and Q.

In some applications, it may be advantageous to redesignate the data input from D to $\overline{D}$ or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown.



The figures show that when Q and $\overline{Q}$ exchange names, the preset and clear pins also exchange names. The polarity indicators (⊾) on $\overline{PRE}$ and $\overline{CLR}$ remain, as these inputs are still active low, but the presence or absence of the polarity indicator changes at D (or $\overline{D}$), Q, and $\overline{Q}$. Pin 5 (Q or $\overline{Q}$) is still in phase with the data input (D or $\overline{D}$); their active levels change together.

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Example:

1 Standard Prefix

2 Military (54) or Commercial (74)

3 Family

Examples: Blank – Transistor-Transistor Logic
ABT – Advanced BiCMOS Technology
ABTE – Advanced BiCMOS Technology/ Enhanced Transceiver Logic
AC/ACT – Advanced CMOS Logic
AHC/AHCT – Advanced High-Speed CMOS Logic
ALS – Advanced Low-Power Schottky Logic
AS – Advanced Schottky Logic
ALVC – Advanced Low-Voltage CMOS Technology
BCT – BiCMOS Bus-Interface Technology
CBT – Crossbar Technology
CDC – Clock-Distribution Circuits
F – F Logic
FB – Backplane Transceiver Logic/Futurebus+
GTL – Gunning-Transceiver Logic
HC/HCT – High-Speed CMOS Logic
LS – Low-Power Schottky Logic
LV – Low-Voltage HCMOS Technology
LVC – Low-Voltage CMOS Technology
LVT – Low-Voltage BiCMOS Technology
S – Schottky Logic
SSTL – Series-Stub Terminated Logic

4 Special Features

Examples: Blank = No Special Features
D – Level-Shifting Diode (CBTD)
H – Bus Hold (ALVCH)
R – Damping Resistor on Inputs/Outputs (LVCR)
S – Schottky Clamping Diode (CBTS)
U – Unbuffered Output (AHCU)

5 Bit Width

Examples: Blank = Gates, MSI, and Octals
1G – MicroGate (Single Gate)
8 – Octal IEEE 1149.1 (JTAG)
16 – Widebus™ (16, 18, and 20 Bit)
18 – Widebus™ IEEE 1149.1 (JTAG)
32 – Widebus+™ (32 and 36 Bit)

6 Options

Examples: Blank = No Options
2 – Series-Damping Resistor on Outputs
4 – Level Shifter

7 Function

Examples: 244 – Noninverting Octal Buffer/Driver
374 – Octal D-Type Flip-Flop
573 – D-Type Transparent Latch
640 – Inverting Octal Transceiver

8 Device Revision

Examples: Blank = No Revision
Letter Designator A–Z

9 Packages

Examples: D, DW – Small-Outline Integrated Circuit (SOIC)
DB, DL – Shrink Small-Outline Package (SSOP)
DBB, DGV – Thin Very Small-Outline Package (TVSOP)
DBV – Small-Outline Transistor Package
DGG, PW – Thin Shrink Small-Outline Package (TSSOP)
FK – Leadless Ceramic Chip Carrier
FN – Plastic Leaded Chip Carrier
GB – Ceramic Pin Grid Array
HFP, HS, HT, HV – Ceramic Quad Flat Package
J, JT – Ceramic Dual In-Line Package
N, NT – Plastic Dual-In-Line Package (DIP)
PH, PQ, RC – Plastic Quad Flat Package
PAG, PAH, PCA, PCB, PM, PN, PZ – Plastic Thin Quad Flat Package
W, WA, WD – Ceramic Flat Package

10 Tape and Reel

Examples: LE – Left Embossed (Required for DB and PW Packages)
R – Standard (Required for DGG, DBB, DGV, and DBV; Optional for D, DW, and DL Packages)

THERMAL INFORMATION

In digital system design, consideration must be given to thermal management of components. The small size of the small-outline package makes this even more critical. Figure 1 shows the thermal resistance of these packages for various rates of air flow.

The thermal resistances in Figure 1 can be used to approximate typical and maximum virtual junction temperatures. In general, the junction temperature for any device can be calculated using the following equation:

$$T_J = R_{\theta JA} \times P_T + T_A$$

where:

T_J = virtual junction temperature
$R_{\theta JA}$ = thermal resistance, junction to free air
P_T = total power dissipation of the device
T_A = free-air temperature

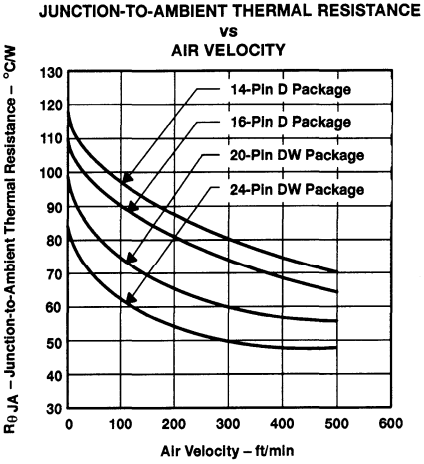


Figure 1

Derating curves for 210-mil shrink small-outline package are shown in Figures 2 through 5.

DERATING CURVES FOR 210-MIL SHRINK SMALL-OUTLINE PACKAGE (DB)

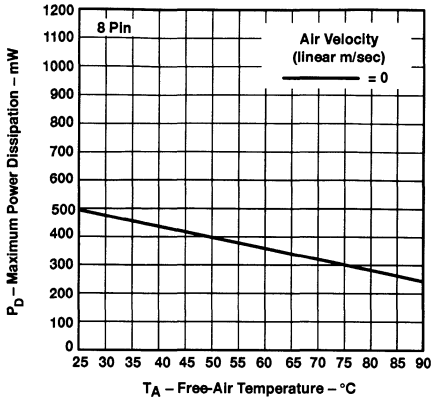


Figure 2

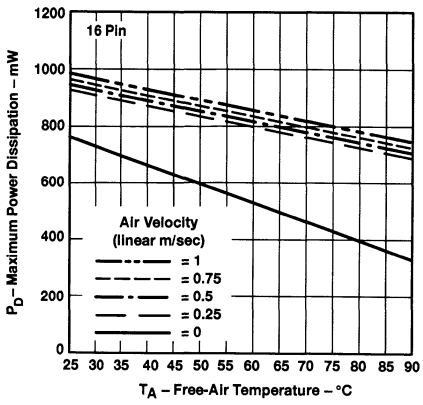


Figure 3

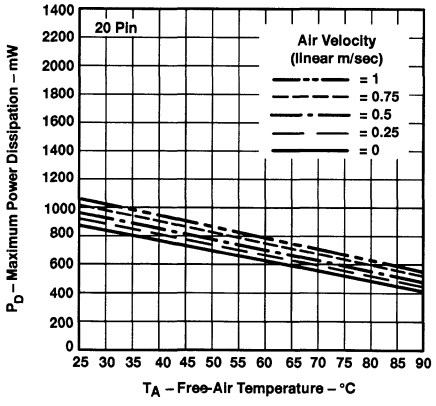


Figure 4

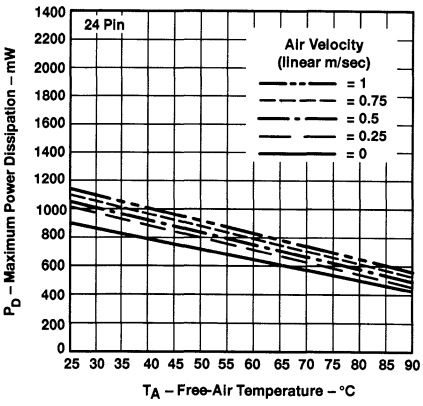


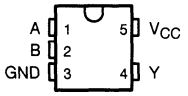
Figure 5

Contents

SCLS313A – MARCH 1996 – REVISED MAY 1996

- **Operating Range: 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Packaged in Plastic Small-Outline Transistor Package**

DBV PACKAGE
(TOP VIEW)



description

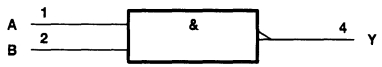
The SN74AHC1G00 performs the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN74AHC1G00 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

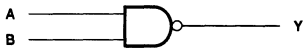
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5
Input clamp current, I_{IK} ($V_I < 0$) ..... − 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 50 mA
Maximum power dissipation at T_A = 55°C (in still air)(see Note 2) ..... 0.2 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 25 millimeters.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		−50	μA
		V_{CC} = 3.3 V ± 0.3 V		−4	mA
		V_{CC} = 5 V ± 0.5 V		−8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
					MIN	TYP	MAX			
V_{OH}		I_{OH} = –50 μA		2 V	1.9	2		1.9		V
				3 V	2.9	3		2.9		
				4.5 V	4.4	4.5		4.4		
		I_{OH} = –4 mA		3 V	2.58			2.48		
		I_{OH} = –8 mA		4.5 V	3.94			3.8		
V_{OL}		I_{OL} = 50 μA		2 V			0.1		0.1	V
				3 V			0.1		0.1	
				4.5 V			0.1		0.1	
		I_{OL} = 4 mA		3 V			0.36		0.44	
		I_{OL} = 8 mA		4.5 V			0.36		0.44	
I_I	A or B inputs	V_I = V_{CC} or GND		5.5 V			±0.1		±1	μA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	5.5 V			2		20	μA
C_i		V_I = V_{CC} or GND		5 V		2	10		10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		5.5	7.9	1	9.5	ns
t_{PHL}					5.5	7.9	1	9.5	
t_{PLH}	A or B	Y	C_L = 50 pF		8	11.4	1	13	ns
t_{PHL}					8	11.4	1	13	

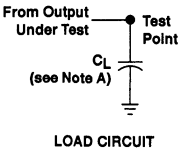
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		3.7	5.5	1	6.5	ns
t_{PHL}					3.7	5.5	1	6.5	
t_{PLH}	A or B	Y	C_L = 50 pF		5.2	7.5	1	8.5	ns
t_{PHL}					5.2	7.5	1	8.5	

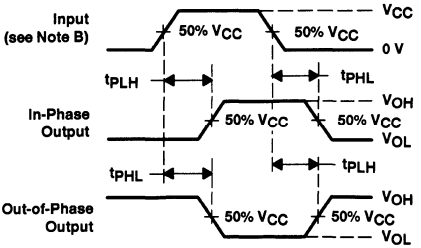
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	9.5	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES

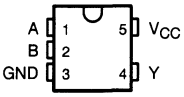
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The output is measured with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCLS316A – MARCH 1996 – REVISED MAY 1996

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Packaged in Plastic Small-Outline Transistor Package**

DBV PACKAGE
(TOP VIEW)



description

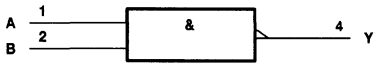
The SN74AHCT1G00 performs the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN74AHCT1G00 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2) ..... 0.2 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 25 millimeters.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = –50 µA	4.5 V	3.15	3.65		3.15		V
	I_{OH} = –8 mA		2.5			2.4		
V_{OL}	I_{OL} = 50 µA	4.5 V			0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	µA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			2		20	µA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5	mA
I_{off}	V_O = 5.5 V	0 V			0.5		5	µA
C_i	$V_I = V_{CC}$ or GND	5 V		2	10		10	pF

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

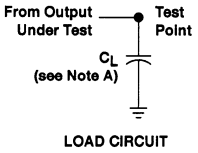
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		5	6.9	1	8	ns
t_{PHL}					5	6.9	1	8	
t_{PLH}	A or B	Y	C_L = 50 pF		5.5	7.9	1	9	ns
t_{PHL}					5.5	7.9	1	9	

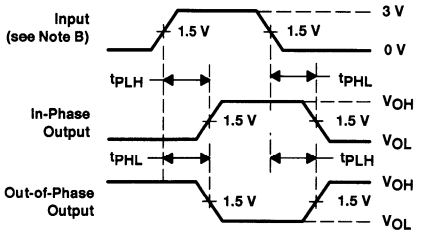
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	10.5	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES

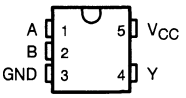
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The output is measured with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCLS342A – APRIL 1996 – REVISED MAY 1996

- **Operating Range: 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Packaged in Plastic Small-Outline Transistor Package**

DBV PACKAGE
(TOP VIEW)



description

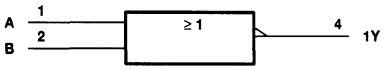
This device contains a single 2-input NOR gate that performs the Boolean function $Y = \overline{A} \cdot \overline{B}$ or $Y = \overline{A + B}$ in positive logic.

The SN74AHC1G02 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

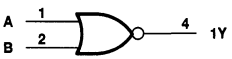
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2) ..... 0.2 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 25 millimeters.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		−50	μA
		V_{CC} = 3.3 V ± 0.3 V		−4	mA
		V_{CC} = 5 V ± 0.5 V		−8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = –50 μA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I_{OH} = –4 mA	3 V	2.58			2.48		
	I_{OH} = –8 mA	4.5 V	3.94			3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20	μA
C_i	V_I = V_{CC} or GND	5 V		4	10		10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		5.6	7.9	1	9.5	ns
t_{PHL}					5.6	7.9	1	9.5	
t_{PLH}	A or B	Y	C_L = 50 pF		8.1	11.4	1	13	ns
t_{PHL}					8.1	11.4	1	13	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

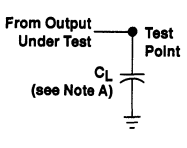
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		3.6	5.5	1	6.5	ns
t_{PHL}					3.6	5.5	1	6.5	
t_{PLH}	A or B	Y	C_L = 50 pF		5.1	7.5	1	8.5	ns
t_{PHL}					5.1	7.5	1	8.5	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

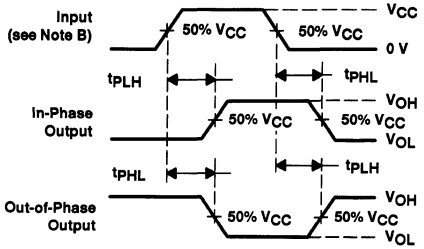
PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load,	f = 1 MHz	15	pF

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES

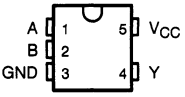
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The output is measured with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCLS341A – APRIL 1996 – REVISED MAY 1996

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Packaged In Plastic Small-Outline Transistor Package**

DBV PACKAGE
(TOP VIEW)



description

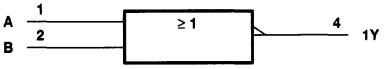
This device contains a single 2-input NOR gate that performs the Boolean function $Y = \overline{A} \bullet \overline{B}$ or $Y = \overline{A + B}$ in positive logic.

The SN74AHCT1G02 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

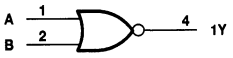
INPUTS		OUTPUTS
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2) ..... 0.2 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 25 millimeters.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25°C$			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	$I_{OH} = -50\ \mu A$		4.5 V	3.15	3.65		3.15		V
	$I_{OH} = -8$ mA			2.5			2.4		
V_{OL}	$I_{OL} = 50\ \mu A$		4.5 V			0.1		0.1	V
	$I_{OL} = 8$ mA					0.36		0.44	
I_I	$V_I = V_{CC}$ or GND		5.5 V			±0.1		±1	µA
I_{CC}	$V_I = V_{CC}$ or GND,	$I_O = 0$	5.5 V			2		20	µA
ΔI_{CC}‡	One input at 3.4 V,	Other inputs at GND or V_{CC}	5.5 V			1.35		1.5	mA
I_{off}	$V_O = 5.5$ V		0 V			0.5		5	µA
C_i	$V_I = V_{CC}$ or GND		5 V		4	10		10	pF

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

PRODUCT PREVIEW

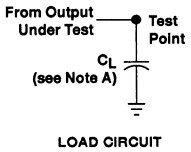
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF				1		ns
t_{PHL}							1		
t_{PLH}	A or B	Y	C_L = 50 pF				1		ns
t_{PHL}							1		

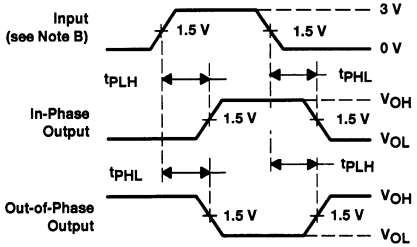
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	17	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The output is measured with one input transition per measurement.

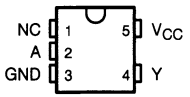
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

SCLS318A – MARCH 1996 – REVISED MAY 1996

- **Operating Range: 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Packaged in Plastic Small-Outline Transistor Package**

DBV PACKAGE
(TOP VIEW)



NC – No internal connection

description

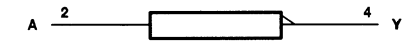
The SN74AHC1G04 contains one inverter gate. The device performs the Boolean function $Y = \overline{A}$.

The SN74AHC1G04 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

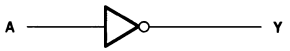
INPUTS A	OUTPUT Y
H	L
L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 50 mA
Maximum power dissipation at T_A = 55°C (in still air)(see Note 2) ..... 0.2 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 25 millimeters.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		−50	μA
		V_{CC} = 3.3 V ± 0.3 V		−4	mA
		V_{CC} = 5 V ± 0.5 V		−8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = – 50 μA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I_{OH} = –4 mA	3 V	2.58			2.48		
	I_{OH} = – 8 mA	4.5 V	3.94			3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20	μA
C_i	V_I = V_{CC} or GND	5 V		2	10		10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		5	7.1	1	8.5	ns
t_{PHL}					5	7.1	1	8.5	
t_{PLH}	A	Y	C_L = 50 pF		7.5	10.6	1	12	ns
t_{PHL}					7.5	10.6	1	12	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

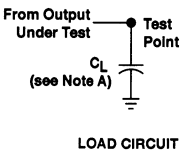
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		3.8	5.5	1	6.5	ns
t_{PHL}					3.8	5.5	1	6.5	
t_{PLH}	A	Y	C_L = 50 pF		5.3	7.5	1	8.5	ns
t_{PHL}					5.3	7.5	1	8.5	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

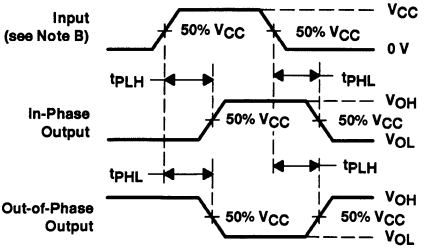
PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	12	pF

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



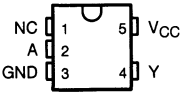
VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The output is measured with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Operating Range: 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Unbuffered Output**
- **Packaged in Plastic Small-Outline Transistor Package**

DBV PACKAGE
(TOP VIEW)



NC – No internal connection

description

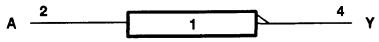
The SN74AHC1GU04 contains a single inverter gate. The device performs the Boolean function $Y = \overline{A}$. Internal circuitry consists of a single-stage inverter that can be used in analog applications, such as crystal oscillators.

The SN74AHC1GU04 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... –20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2) ..... 0.2 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 25 millimeters.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.7		V
		V_{CC} = 3 V	2.4		
		V_{CC} = 5.5 V	4.4		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.3	V
		V_{CC} = 3 V		0.6	
		V_{CC} = 5.5 V		1.1	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50	µA
		V_{CC} = 3.3 V ± 0.3 V		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	µA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
T_A	Operating free-air temperature		–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = –50 µA	2 V	1.8	2		1.8		V
		3 V	2.7	3		2.7		
		4.5 V	4	4.5		4		
	I_{OH} = –4 mA	3 V	2.58			2.48		
	I_{OH} = –8 mA	4.5 V	3.94			3.8		
V_{OL}	I_{OL} = 50 µA	2 V			0.2		0.2	V
		3 V			0.3		0.3	
		4.5 V			0.5		0.5	
	I_{OL} = 4 mA	3 V			0.36		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.44	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	µA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			2		20	µA
C_i	$V_I = V_{CC}$ or GND	5 V		2	10		10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		5	8.9	1	10.5	ns
t_{PHL}					5	8.9	1	10.5	
t_{PLH}	A	Y	C_L = 50 pF		7.5	11.4	1	13	ns
t_{PHL}					7.5	11.4	1	13	

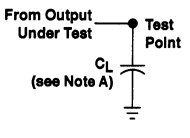
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		3.5	5.5	1	6.5	ns
t_{PHL}					3.5	5.5	1	6.5	
t_{PLH}	A	Y	C_L = 50 pF		5	7	1	8	ns
t_{PHL}					5	7	1	8	

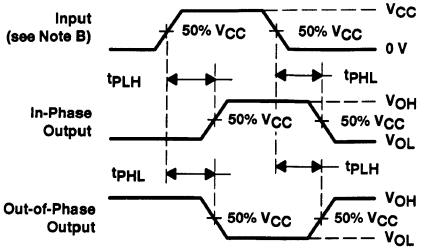
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	7.3	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The output is measured with one input transition per measurement.

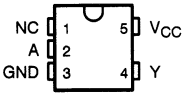
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

SCLS319A – MARCH 1996 – REVISED MAY 1996

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Packaged in Plastic Small-Outline Transistor Package**

DBV PACKAGE
(TOP VIEW)



NC – No internal connection

description

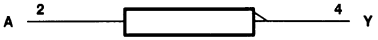
The SN74AHCT1G04 contains one gate. The device performs the Boolean function $Y = \overline{A}$.

The SN74AHCT1G04 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

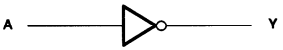
INPUT A	OUTPUT Y
H	L
L	H

logic symbol



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2) ..... 0.2 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 25 millimeters.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25°C$			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	$I_{OH} = -50\ \mu A$	4.5 V	3.15	3.65		3.15		V
	$I_{OH} = -8$ mA		2.5			2.4		
V_{OL}	$I_{OL} = 50\ \mu A$	4.5 V			0.1		0.1	V
	$I_{OL} = 8$ mA				0.36		0.44	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		20	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4	10		10	pF

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

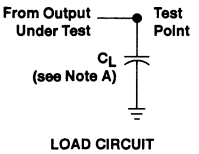
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		4.7	6.7	1	7.5	ns
t_{PHL}					4.7	6.7	1	7.5	
t_{PLH}	A	Y	C_L = 50 pF		5.5	7.7	1	8.5	ns
t_{PHL}					5.5	7.7	1	8.5	

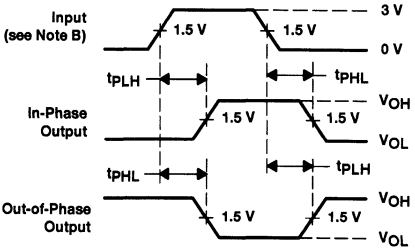
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	14	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The output is measured with one input transition per measurement.

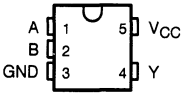
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

SCLS314A – MARCH 1996 – REVISED MAY 1996

- **Operating Range: 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Packaged in Plastic Small-Outline Transistor Package**

DBV PACKAGE
(TOP VIEW)



description

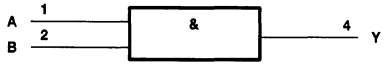
The SN74AHC1G08 is a single 2-input positive-AND gate. The device performs the Boolean function $Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

The SN74AHC1G08 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... − 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 50 mA
Maximum power dissipation at T_A = 55°C (in still air)(see Note 2) ..... 0.2 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 25 millimeters.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		−50	μA
		V_{CC} = 3.3 V ± 0.3 V		−4	mA
		V_{CC} = 5 V ± 0.5 V		−8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = –50 μA	2 V	1.9	2		1.9		V
			3 V	2.9	3		2.9		
			4.5 V	4.4	4.5		4.4		
		I_{OH} = –4 mA	3 V	2.58			2.48		
		I_{OH} = –8 mA	4.5 V	3.94			3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1	V
			3 V			0.1		0.1	
			4.5 V			0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.44	
I_I	A or B inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			2		20	μA
C_i		$V_I = V_{CC}$ or GND	5 V		4	10		10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		6.2	8.8	1	10.5	ns
t_{PHL}					6.2	8.8	1	10.5	
t_{PLH}	A or B	Y	C_L = 50 pF		8.7	12.3	1	14	ns
t_{PHL}					8.7	12.3	1	14	

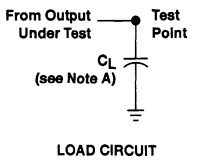
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		4.3	5.9	1	7	ns
t_{PHL}					4.3	5.9	1	7	
t_{PLH}	A or B	Y	C_L = 50 pF		5.8	7.9	1	9	ns
t_{PHL}					5.8	7.9	1	9	

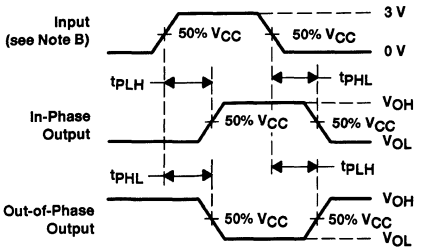
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	18	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES

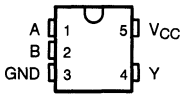
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The output is measured with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCLS315A – MARCH 1996 – REVISED MAY 1996

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Packaged in Plastic Small-Outline Transistor Package**

DBV PACKAGE
(TOP VIEW)



description

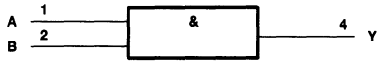
The SN74AHCT1G08 is a single 2-input positive-AND gate. The device performs the Boolean function $Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

The SN74AHCT1G08 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... − 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... − 20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 50 mA
Maximum power dissipation at T_A = 55°C (in still air)(see Note 2) ..... 0.2 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 25 millimeters.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	− 40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA		4.5 V	3.15	3.65		3.15		V
	I_{OH} = −8 mA			2.5			2.4		
V_{OL}	I_{OL} = 50 μA		4.5 V			0.1		0.1	V
	I_{OL} = 8 mA					0.36		0.44	
I_I	$V_I = V_{CC}$ or GND		5.5 V			±0.1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V			2		20	μA
ΔI_{CC}‡	One input at 3.4 V,	Other inputs at V_{CC} or GND	5.5 V			1.35		1.5	mA
I_{off}	V_O= 5.5 V		0 V			0.5		5	μA
C_i	$V_I = V_{CC}$ or GND		5 V		4	10		10	pF

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

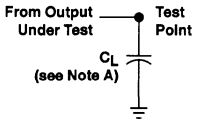
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		5	6.9	1	8	ns
t_{PHL}					5	6.9	1	8	
t_{PLH}	A or B	Y	C_L = 50 pF		5.5	7.9	1	9	ns
t_{PHL}					5.5	7.9	1	9	

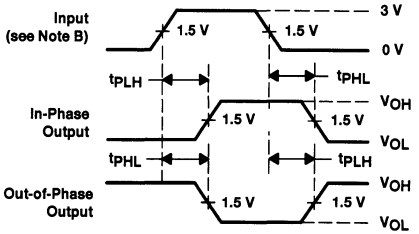
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	18	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



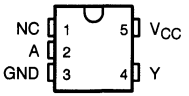
VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The output is measured with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Operating Range: 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Packaged in Plastic Small-Outline Transistor Package**

DBV PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN74AHC1G14 contains one inverter gate. The device performs the Boolean function $Y = \overline{A}$.

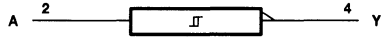
The device functions as an independent inverter gate, but because of the Schmitt action, gates may have different input threshold levels for positive- (V_{T+}) and negative-going (V_{T-}) signals.

The SN74AHC1G14 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

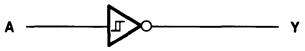
INPUTS A	OUTPUT Y
H	L
L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air)(see Note 2) ..... 0.2 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 25 millimeters.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		−50	µA
		V_{CC} = 3.3 V ± 0.3 V		−4	mA
		V_{CC} = 5 V ± 0.5 V		−8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	µA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{T+} Positive-going input threshold voltage		3 V			2.2		2.2	V
		4.5 V			3.15		3.15	
		5.5 V			3.85		3.85	
V_{T-} Negative-going input threshold voltage		3 V	0.9			0.9		V
		4.5 V	1.35			1.35		
		5.5 V	1.65			1.65		
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)		3 V	0.3		1.2	0.3	1.2	V
		4.5 V	0.4		1.4	0.4	1.4	
		5.5 V	0.5		1.6	0.5	1.6	
V_{OH}	I_{OH} = – 50 μA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I_{OH} = – 4 mA	3 V	2.58			2.48		
	I_{OH} = – 8 mA	4.5 V	3.94			3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.44	
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			2		20	μA
C_i	$V_I = V_{CC}$ or GND	5 V		2	10		10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		8.3	12.8	1	15	ns
t_{PHL}					8.3	12.8	1	15	
t_{PLH}	A	Y	C_L = 50 pF		10.8	16.3	1	18.5	ns
t_{PHL}					10.8	16.3	1	18.5	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

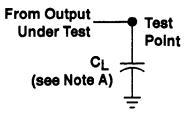
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		5.5	8.6	1	10	ns
t_{PHL}					5.5	8.6	1	10	
t_{PLH}	A	Y	C_L = 50 pF		7	10.6	1	12	ns
t_{PHL}					7	10.6	1	12	

PRODUCT PREVIEW

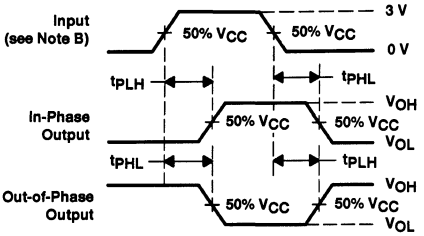
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	9	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The output is measured with one input transition per measurement.

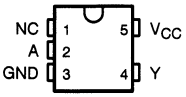
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

SCLS322A – MARCH 1996 – REVISED MAY 1996

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Packaged In Plastic Small-Outline Transistor Package**

DBV PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN74AHCT1G14 contains a single inverter gate. The device performs the Boolean function $Y = \overline{A}$.

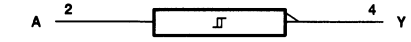
The device functions as an independent inverter gate, but because of the Schmitt action, gates may have different input threshold levels for positive- (V_{T+}) and negative-going (V_{T-}) signals.

The SN74AHCT1G14 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

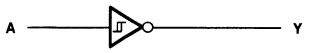
INPUTS A	OUTPUT Y
H	L
L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... − 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... − 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air)(see Note 2) ..... 0.2 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 25 millimeters.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2.1		V
V_{IL}	Low-level input voltage		0.5	V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	− 40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{T+} Positive-going input threshold voltage		4.5 V			2		2	V
		5.5 V			2		2	
V_{T-} Negative-going input threshold voltage		4.5 V	0.6			0.6		V
		5.5 V	0.6			0.6		
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)		4.5 V	0.4		1.4	0.4	1.4	V
		5.5 V	0.5		1.6	0.5	1.6	
V_{OH}	I_{OH} = – 50 μA	4.5 V	3.15	3.65		3.15		V
	I_{OH} = – 8 mA	4.5 V	2.5			2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1	V
	I_{OL} = 8 mA	4.5 V			0.36		0.44	
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			2		20	μA
C_i	$V_I = V_{CC}$ or GND	5 V		2	10		10	pF

switching characteristics over recommended operating free-air temperature range V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

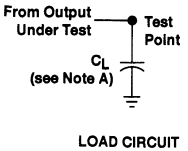
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		4	7	1	8	ns
t_{PHL}					4	7	1	8	
t_{PLH}	A	Y	C_L = 50 pF		5.5	8	1	9	ns
t_{PHL}					5.5	8	1	9	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

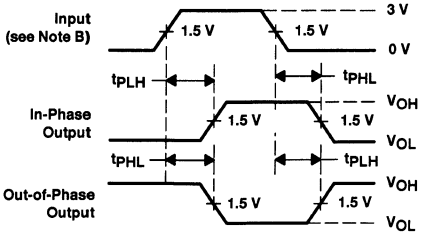
PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	12	pF

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The output is measured with one input transition per measurement.

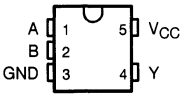
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

SCLS317A – MARCH 1996 – REVISED MAY 1996

- **Operating Range: 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Packaged in Plastic Small-Outline Transistor Package**

DBV PACKAGE
(TOP VIEW)



description

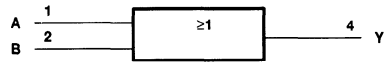
The SN74AHC1G32 is a single 2-input positive-OR gate. The device performs the Boolean function $Y = A + B$ or $Y = \overline{A \bullet B}$ in positive logic.

The SN74AHC1G32 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

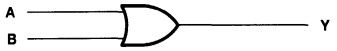
INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... − 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 50 mA
Maximum power dissipation at T_A = 55°C (in still air)(see Note 2) ..... 0.2 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 25 millimeters.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		− 50	μA
		V_{CC} = 3.3 V ± 0.3 V		− 4	mA
		V_{CC} = 5 V ± 0.5 V		−8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		− 40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = – 50 μA	2 V	1.9	2		1.9		V
			3 V	2.9	3		2.9		
			4.5 V	4.4	4.5		4.4		
		I_{OH} = –4 mA	3 V	2.58			2.48		
		I_{OH} = – 8 mA	4.5 V	3.94			3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1	V
			3 V			0.1		0.1	
			4.5 V			0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.44	
I_I	A or B inputs	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20	μA
C_i		V_I = V_{CC} or GND	5 V		2	10		10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		5.5	7.9	1	9.5	ns
t_{PHL}					5.5	7.9	1	9.5	
t_{PLH}	A or B	Y	C_L = 50 pF		8	11.4	1	13	ns
t_{PHL}					8	11.4	1	13	

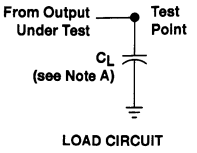
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

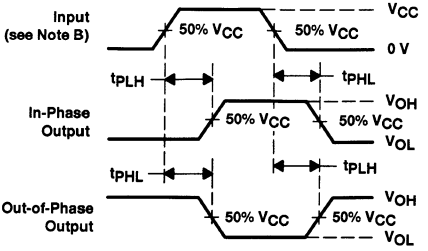
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		3.8	5.5	1	6.5	ns
t_{PHL}					3.8	5.5	1	6.5	
t_{PLH}	A or B	Y	C_L = 50 pF		5.3	7.5	1	8.5	ns
t_{PHL}					5.3	7.5	1	8.5	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	14	pF

PARAMETER MEASUREMENT INFORMATION





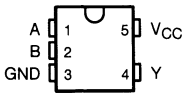
VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The output is measured with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Packaged in Plastic Small-Outline Transistor Package**

DBV PACKAGE
(TOP VIEW)



description

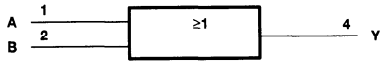
The SN74AHCT1G32 is a single 2-input positive-OR gate. The device performs the Boolean function $Y = A + B$ or $Y = \overline{\overline{A} \bullet \overline{B}}$ in positive logic.

The SN74AHCT1G32 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

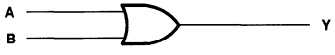
INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 50 mA
Maximum power dissipation at T_A = 55°C (in still air)(see Note 2) ..... 0.2 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 25 millimeters.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA		4.5 V	3.15	3.65		3.15		V
	I_{OH} = −8 mA			2.5			2.4		
V_{OL}	I_{OL} = 50 μA		4.5 V			0.1		0.1	V
	I_{OL} = 8 mA					0.36		0.44	
I_I	$V_I = V_{CC}$ or GND		5.5 V			±0.1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V			2		20	μA
ΔI_{CC}‡	One input at 3.4 V,	Other inputs at V_{CC} or GND	5.5 V			1.35		1.5	mA
I_{off}	V_O = 5.5 V		0 V			0.5		5	μA
C_i	$V_I = V_{CC}$ or GND		5 V		2	10		10	pF

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

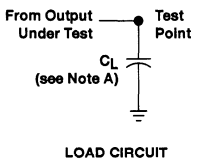
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		5	6.9	1	8	ns
t_{PHL}					5	6.9	1	8	
t_{PLH}	A or B	Y	C_L = 50 pF		5.5	7.9	1	9	ns
t_{PHL}					5.5	7.9	1	9	

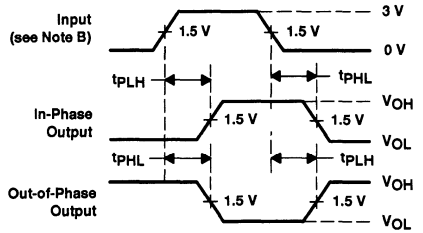
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	11.5	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES

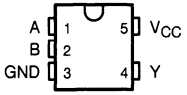
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The output is measured with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCLS323A – MARCH 1996 – REVISED MAY 1996

- **Operating Range: 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Packaged In Plastic Small-Outline Transistor Package**

DBV PACKAGE
(TOP VIEW)



description

The SN74AHC1G86 is a single 2-input exclusive-OR gate. The device performs the Boolean function $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

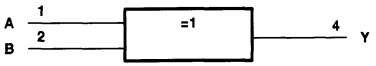
A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

The SN74AHC1G86 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

logic symbol†



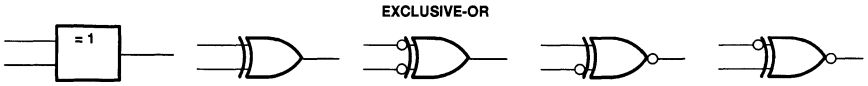
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

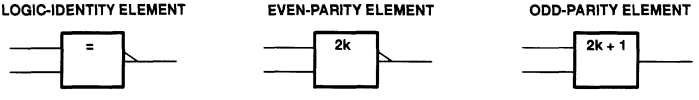
EPIC is a trademark of Texas Instruments Incorporated.

exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



These are five equivalent exclusive-OR symbols valid for an SN74AHC1G86 gate in positive logic; negation may be shown at any two ports.



The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Note 1)	–0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2)	0.2 W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 25 millimeters.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = –50 μA	2 V	1.9	2		1.9		V
			3 V	2.9	3		2.9		
			4.5 V	4.4	4.5		4.4		
		I_{OH} = –4 mA	3 V	2.58			2.48		
		I_{OH} = –8 mA	4.5 V	3.94			3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1	V
			3 V			0.1		0.1	
			4.5 V			0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.44	
I_I	A or B inputs	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20	μA
C_i		V_I = V_{CC} or GND	5 V		4	10		10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		7	11	1	13	ns
t_{PHL}					7	11	1	13	
t_{PLH}	A or B	Y	C_L = 50 pF		9.5	14.5	1	16.5	ns
t_{PHL}					9.5	14.5	1	16.5	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

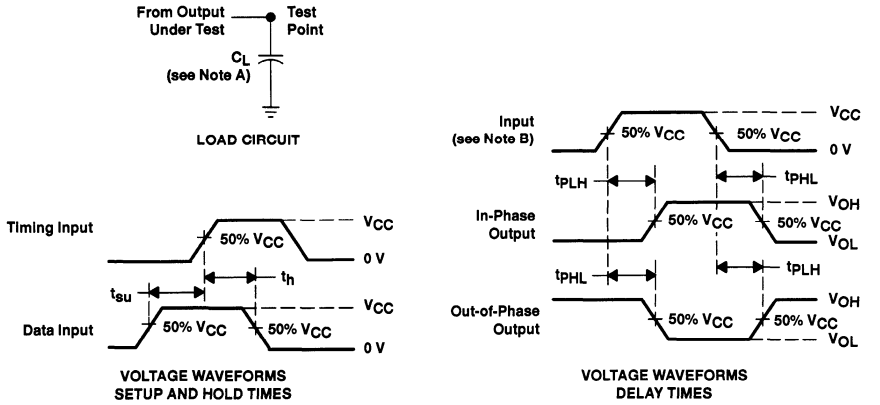
PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		4.8	6.8	1	8	ns
t_{PHL}					4.8	6.8	1	8	
t_{PLH}	A or B	Y	C_L = 50 pF		6.3	8.8	1	10	ns
t_{PHL}					6.3	8.8	1	10	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	18	pF

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The output is measured with one input transition per measurement.

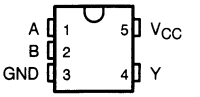
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

SCLS324A – MARCH 1996 – REVISED MAY 1996

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Packaged in Plastic Small-Outline Transistor Package**

DBV PACKAGE
(TOP VIEW)



description

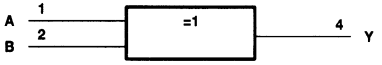
The SN74AHCT1G86 is a single 2-input exclusive-OR gate. The device performs the Boolean function $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

The SN74AHCT1G86 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

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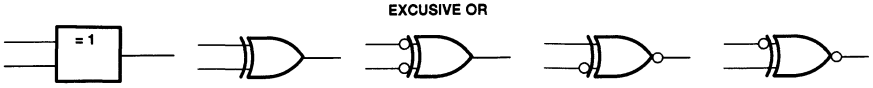
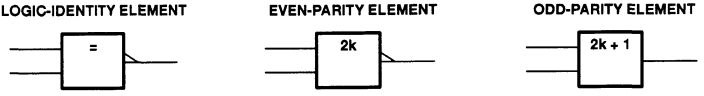
exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



These are five equivalent exclusive-OR symbols valid for an SN74AHCT1G86 gate in positive logic; negation may be shown at any two ports.



The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... – 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... – 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2) ..... 0.2 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 25 millimeters.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	– 40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = – 50 μA		4.5 V	3.15	3.65		3.15		V
	I_{OH} = – 8 mA			2.5			2.4		
V_{OL}	I_{OL} = 50 μA		4.5 V			0.1		0.1	V
	I_{OL} = 8 mA					0.36		0.44	
I_I	V_I = V_{CC} or GND		5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	5.5 V			2		20	μA
ΔI_{CC}†	One input at 3.4 V,	Other inputs at V_{CC} or GND	5.5 V			1.35		1.5	mA
I_{off}	V_O = 5.5 V		0 V			0.5		5	μA
C_i	V_I = V_{CC} or GND		5 V		4	10		10	pF

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

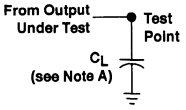
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		5	6.9	1	8	ns
t_{PHL}					5	6.9	1	8	
t_{PLH}	A or B	Y	C_L = 50 pF		5.5	7.9	1	9	ns
t_{PHL}					5.5	7.9	1	9	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

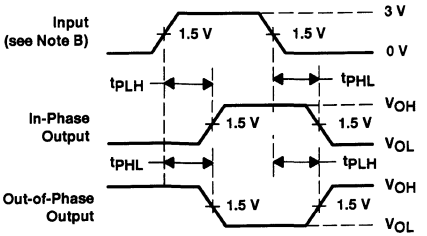
PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	18	pF

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The output is measured with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

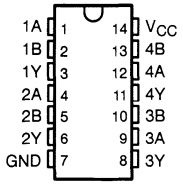
Contents

Contents (continued)

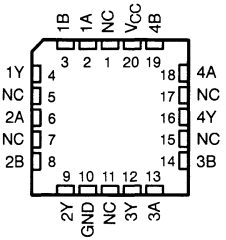
SCLS227A – OCTOBER 1995 – REVISED MARCH 1996

- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHC00 . . . J OR W PACKAGE
SN74AHC00 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC00 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

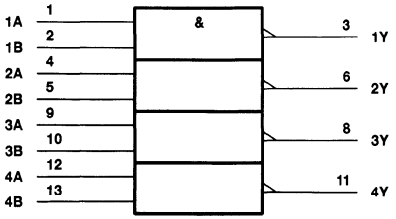
The 'AHC00 perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54AHC00 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC00 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	**B**	**Y**
H	H	L
L	X	H
X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

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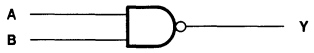
logic diagram, (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			SN54AHC00		SN74AHC00		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC00		SN74AHC00		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
			3 V	2.9	3		2.9		2.9		
			4.5 V	4.4	4.5		4.4		4.4		
		I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
		I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
			3 V			0.1		0.1		0.1	
			4.5 V			0.1		0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	A or B inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20		20	μA
C_i		V_I = V_{CC} or GND	5 V		2	10				10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHC00					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A or B	Y	C_L = 15 pF		5.5	7.9	1	9.5	ns
t_{PHL}*					5.5	7.9	1	9.5	
t_{PLH}	A or B	Y	C_L = 50 pF		8	11.4	1	13	ns
t_{PHL}					8	11.4	1	13	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHC00					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		5.5	7.9	1	9.5	ns
t_{PHL}					5.5	7.9	1	9.5	
t_{PLH}	A or B	Y	C_L = 50 pF		8	11.4	1	13	ns
t_{PHL}					8	11.4	1	13	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHC00					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A or B	Y	C_L = 15 pF		3.7	5.5	1	6.5	ns
t_{PHL}*					3.7	5.5	1	6.5	
t_{PLH}	A or B	Y	C_L = 50 pF		5.2	7.5	1	8.5	ns
t_{PHL}					5.2	7.5	1	8.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHC00					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		3.7	5.5	1	6.5	ns
t_{PHL}					3.7	5.5	1	6.5	
t_{PLH}	A or B	Y	C_L = 50 pF		5.2	7.5	1	8.5	ns
t_{PHL}					5.2	7.5	1	8.5	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

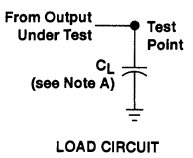
PARAMETER		SN74AHC00			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.3	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.3	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.6		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

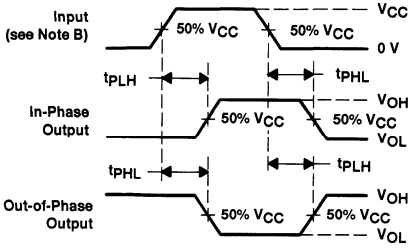
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	9.5	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



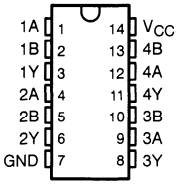
VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

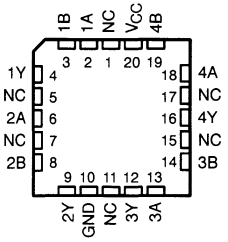
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHCT00 . . . J OR W PACKAGE
SN74AHCT00 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT00 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AHCT00 perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

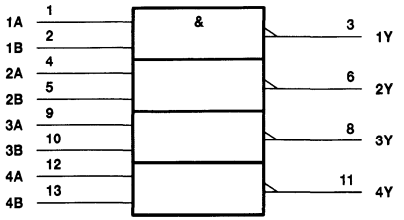
The SN54AHCT00 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT00 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

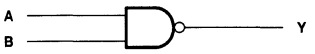
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, DB, J, N, PW, and W packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHCT00		SN74AHCT00		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT00		SN74AHCT00		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		3.15		V
	I_{OH} = –8 mA		2.5			2.4		2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20		20	μA
ΔI_{CC}†	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
I_{off}	V_O = 5.5 V	0 V			0.5*				5	μA
C_i	V_I = V_{CC} or GND	5 V		2	10				10	pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT00				UNIT
				T_A = 25°C			MIN MAX	
				MIN	TYP	MAX		
t_{PLH}*	A or B	Y	C_L = 15 pF		5	6.9	1 8	ns
t_{PHL}*					5	6.9	1 8	
t_{PLH}	A or B	Y	C_L = 50 pF		5.5	7.9	1 9	ns
t_{PHL}					5.5	7.9	1 9	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT00				UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		5	6.9	1	8	ns
t_{PHL}					5	6.9	1	8	
t_{PLH}	A or B	Y	C_L = 50 pF		5.5	7.9	1	9	ns
t_{PHL}					5.5	7.9	1	9	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

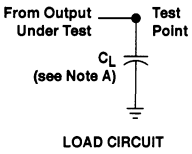
PARAMETER		SN74AHCT00			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.4	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.4	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.5		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

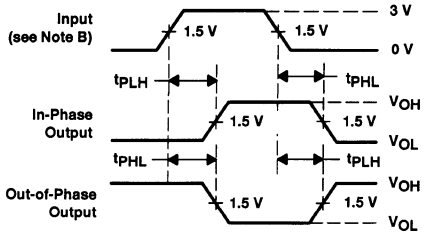
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	10.5	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



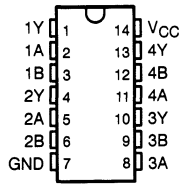
VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

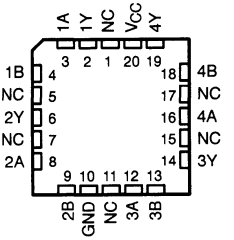
Figure 1. Load Circuit and Voltage Waveforms

- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHC02 . . . J OR W PACKAGE
SN74AHC02 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC02 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

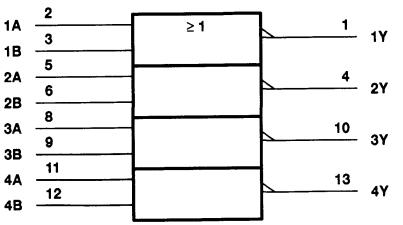
The 'AHC02 contain four independent 2-input NOR gates that perform the Boolean function $Y = \overline{A} \cdot \overline{B}$ or $Y = \overline{A + B}$ in positive logic.

The SN54AHC02 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC02 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†

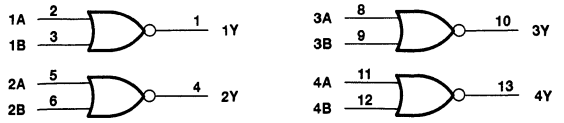


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			SN54AHC02		SN74AHC02		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC02		SN74AHC02		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
	I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20		20	μA
C_i	V_I = V_{CC} or GND	5 V		4	10				10	pF

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHC02					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A or B	Y	C_L = 15 pF		5.6	7.9	1	9.5	ns
t_{PHL}*					5.6	7.9	1	9.5	
t_{PLH}	A or B	Y	C_L = 50 pF		8.1	11.4	1	13	ns
t_{PHL}					8.1	11.4	1	13	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHC02					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		5.6	7.9	1	9.5	ns
t_{PHL}					5.6	7.9	1	9.5	
t_{PLH}	A or B	Y	C_L = 50 pF		8.1	11.4	1	13	ns
t_{PHL}					8.1	11.4	1	13	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHC02					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A or B	Y	C_L = 15 pF		3.6	5.5	1	6.5	ns
t_{PHL}*					3.6	5.5	1	6.5	
t_{PLH}	A or B	Y	C_L = 50 pF		5.1	7.5	1	8.5	ns
t_{PHL}					5.1	7.5	1	8.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHC02					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		3.6	5.5	1	6.5	ns
t_{PHL}					3.6	5.5	1	6.5	
t_{PLH}	A or B	Y	C_L = 50 pF		5.1	7.5	1	8.5	ns
t_{PHL}					5.1	7.5	1	8.5	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

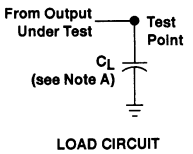
PARAMETER		SN74AHC02			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

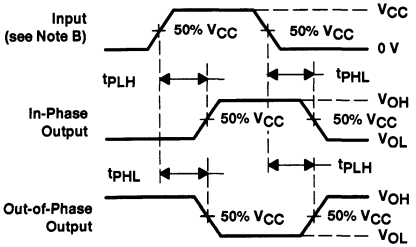
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load,	f = 1 MHz	15	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

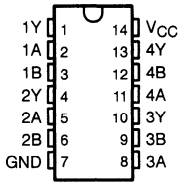
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

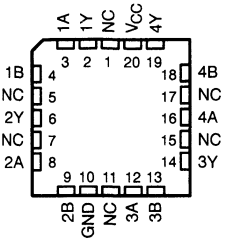
SCLS262B – DECEMBER 1995 – REVISED MARCH 1996

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHCT02 . . . J OR W PACKAGE
SN74AHCT02 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT02 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

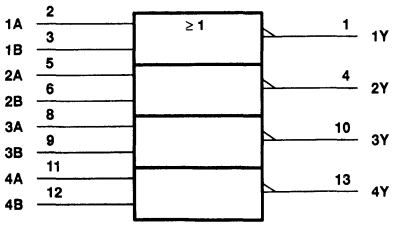
These devices contain four independent 2-input NOR gates that perform the Boolean function $Y = \overline{A} \cdot \overline{B}$ or $Y = \overline{A + B}$ in positive logic.

The SN54AHCT02 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT02 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†

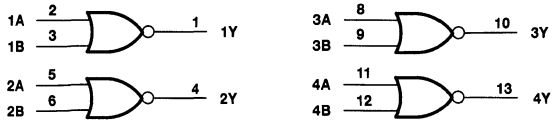


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHCT02		SN74AHCT02		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT02		SN74AHCT02		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		3.15		V
	I_{OH} = –8 mA		2.5			2.4		2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20		20	μA
ΔI_{CC}†	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			1.35		1.5		1.5	mA
I_{off}	V_O = 5.5 V	0 V			0.5*				5	μA
C_i	V_I = V_{CC} or GND	5 V		4	10				10	pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHCT02				UNIT
				T_A = 25°C			MIN MAX	
				MIN	TYP	MAX		
t_{PLH}*	A or B	Y	C_L = 15 pF				1	ns
t_{PHL}*							1	
t_{PLH}	A or B	Y	C_L = 50 pF				1	ns
t_{PHL}							1	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHCT02				UNIT
				T_A = 25°C			MIN MAX	
				MIN	TYP	MAX		
t_{PLH}	A or B	Y	C_L = 15 pF				1	ns
t_{PHL}							1	
t_{PLH}	A or B	Y	C_L = 50 pF				1	ns
t_{PHL}							1	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

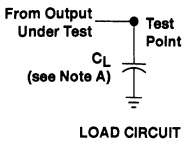
PARAMETER		SN74AHCT02			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

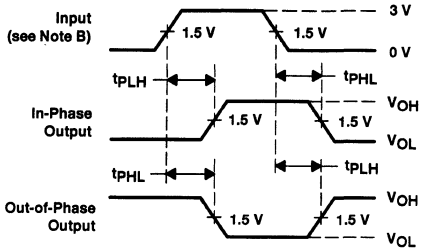
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	17	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



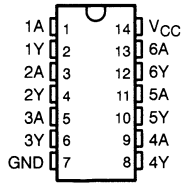
VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

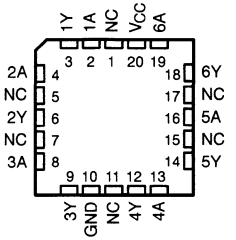
Figure 1. Load Circuit and Voltage Waveforms

- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHC04 . . . J OR W PACKAGE
SN74AHC04 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC04 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

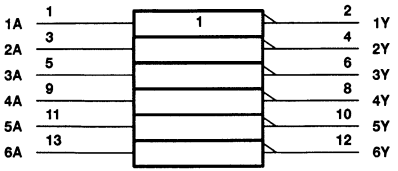
The 'AHC04 contain six independent inverters. These devices perform the Boolean function $Y = \overline{A}$.

The SN54AHC04 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC04 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

EPIC is a trademark of Texas Instruments Incorporated.

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			SN54AHC04		SN74AHC04		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC04		SN74AHC04		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
	I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20		20	μA
C_i	V_I = V_{CC} or GND	5 V		2	10				10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC04					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A	Y	C_L = 15 pF		5	7.1	1	8.5	ns
t_{PHL}*					5	7.1	1	8.5	
t_{PLH}	A	Y	C_L = 50 pF		7.5	10.6	1	12	ns
t_{PHL}					7.5	10.6	1	12	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC04					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		5	7.1	1	8.5	ns
t_{PHL}					5	7.1	1	8.5	
t_{PLH}	A	Y	C_L = 50 pF		7.5	10.6	1	12	ns
t_{PHL}					7.5	10.6	1	12	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC04					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A	Y	C_L = 15 pF		3.8	5.5	1	6.5	ns
t_{PHL}*					3.8	5.5	1	6.5	
t_{PLH}	A	Y	C_L = 50 pF		5.3	7.5	1	8.5	ns
t_{PHL}					5.3	7.5	1	8.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC04					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		3.8	5.5	1	6.5	ns
t_{PHL}					3.8	5.5	1	6.5	
t_{PLH}	A	Y	C_L = 50 pF		5.3	7.5	1	8.5	ns
t_{PHL}					5.3	7.5	1	8.5	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

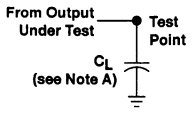
PARAMETER		SN74AHC04			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.4		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.4		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.8		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

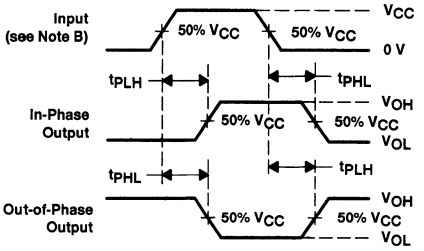
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	12	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



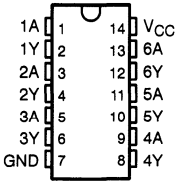
VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

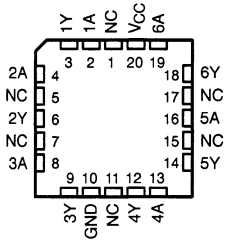
Figure 1. Load Circuit and Voltage Waveforms

- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Unbuffered Outputs**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHCU04 . . . J OR W PACKAGE
SN74AHCU04 . . . D, DB, N OR PW PACKAGE
(TOP VIEW)



SN54AHCU04 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

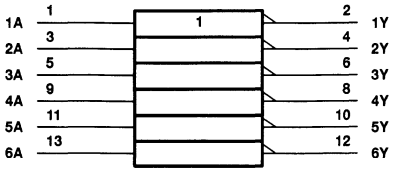
The 'AHCU04 contain six independent inverters. These devices perform the Boolean function $Y = \overline{A}$. Internal circuitry consists of single-stage inverters that can be used in analog applications such as crystal oscillators.

The SN54AHCU04 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCU04 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

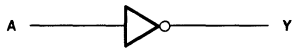
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, DB, J, N, PW, and W packages.

EPIC is a trademark of Texas Instruments Incorporated.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			SN54AHCU04		SN74AHCU04		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.7		1.7		V
		V_{CC} = 3 V	2.4		2.4		
		V_{CC} = 5.5 V	4.4		4.4		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.3		0.3	V
		V_{CC} = 3 V		0.6		0.6	
		V_{CC} = 5.5 V		1.1		1.1	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	µA
		V_{CC} = 3.3 V ± 0.3 V		–4		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	µA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCU04		SN74AHCU04		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	2 V	1.8	2		1.8		1.8		V
		3 V	2.7	3		2.7		2.7		
		4.5 V	4	4.5		4		4		
	I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
	I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.2		0.2		0.2	V
		3 V			0.3		0.3		0.3	
		4.5 V			0.5		0.5		0.5	
	I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			2		20		20	μA
C_i	$V_I = V_{CC}$ or GND	5 V		2	10				10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHCU04					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A	Y	C_L = 15 pF		5	8.9	1	10.5	ns
t_{PHL}*					5	8.9	1	10.5	
t_{PLH}	A	Y	C_L = 50 pF		7.5	11.4	1	13	ns
t_{PHL}					7.5	11.4	1	13	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHCU04					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		5	8.9	1	10.5	ns
t_{PHL}					5	8.9	1	10.5	
t_{PLH}	A	Y	C_L = 50 pF		7.5	11.4	1	13	ns
t_{PHL}					7.5	11.4	1	13	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHCU04					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A	Y	C_L = 15 pF		3.5	5.5	1	6.5	ns
t_{PHL}*					3.5	5.5	1	6.5	
t_{PLH}	A	Y	C_L = 50 pF		5	7	1	8	ns
t_{PHL}					5	7	1	8	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHCU04					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		3.5	5.5	1	6.5	ns
t_{PHL}					3.5	5.5	1	6.5	
t_{PLH}	A	Y	C_L = 50 pF		5	7	1	8	ns
t_{PHL}					5	7	1	8	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

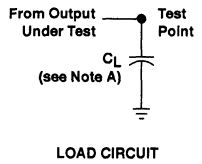
PARAMETER		SN74AHCU04			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.5		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.3		V
$V_{IH(D)}$	High-level dynamic input voltage	4			V
$V_{IL(D)}$	Low-level dynamic input voltage			1	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

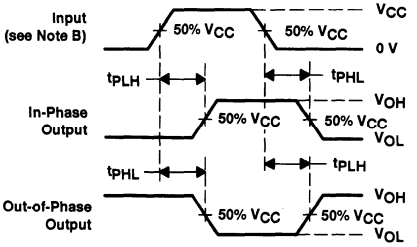
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	7.3	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES

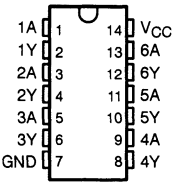
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

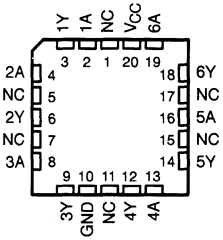
SCLS232B – OCTOBER 1995 – REVISED MARCH 1996

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHCT04 . . . J OR W PACKAGE
SN74AHCT04 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT04 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

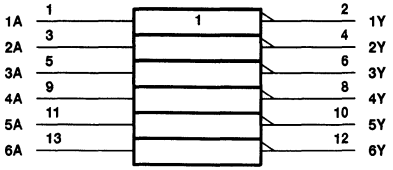
The 'AHCT04 contain six independent inverters. These devices perform the Boolean function $Y = \overline{A}$.

The SN54AHCT04 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT04 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

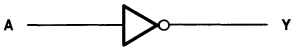
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, DB, J, N, PW, and W packages.

EPIC is a trademark of Texas Instruments Incorporated.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHCT04		SN74AHCT04		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT04		SN74AHCT04		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		3.15		V
	I_{OH} = –8 mA		2.5			2.4		2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20		20	μA
ΔI_{CC}†	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
C_i	V_I = V_{CC} or GND	5 V		4	10				10	pF

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT04					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A	Y	C_L = 15 pF		4.7	6.7	1	7.5	ns
t_{PHL}*					4.7	6.7	1	7.5	
t_{PLH}	A	Y	C_L = 50 pF		5.5	7.7	1	8.5	ns
t_{PHL}					5.5	7.7	1	8.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT04					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		4.7	6.7	1	7.5	ns
t_{PHL}					4.7	6.7	1	7.5	
t_{PLH}	A	Y	C_L = 50 pF		5.5	7.7	1	8.5	ns
t_{PHL}					5.5	7.7	1	8.5	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

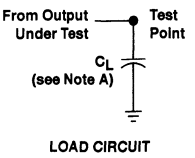
PARAMETER		SN74AHCT04			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.8		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

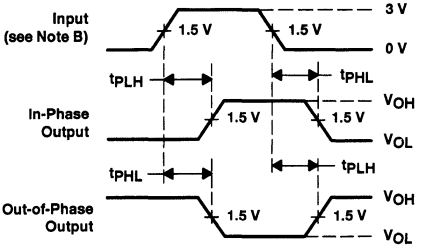
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	14	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



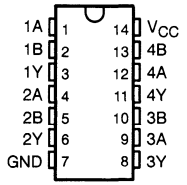
VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

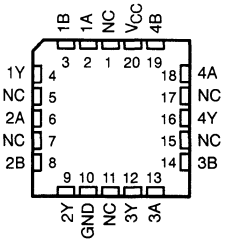
Figure 1. Load Circuit and Voltage Waveforms

- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHC08 . . . J OR W PACKAGE
SN74AHC08 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC08 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AHC08 are quadruple 2-input positive-AND gates. These devices perform the Boolean function $Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

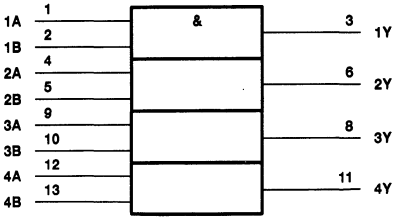
The SN54AHC08 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC08 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			SN54AHC08		SN74AHC08		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC08		SN74AHC08		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
			3 V	2.9	3		2.9		2.9		
			4.5 V	4.4	4.5		4.4		4.4		
		I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
		I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
			3 V			0.1		0.1		0.1	
			4.5 V			0.1		0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	A or B inputs	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20		20	μA
C_i		V_I = V_{CC} or GND	5 V		4	10				10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHC08					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A or B	Y	C_L = 15 pF		6.2	8.8	1	10.5	ns
t_{PHL}*					6.2	8.8	1	10.5	
t_{PLH}	A or B	Y	C_L = 50 pF		8.7	12.3	1	14	ns
t_{PHL}					8.7	12.3	1	14	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHC08					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		6.2	8.8	1	10.5	ns
t_{PHL}					6.2	8.8	1	10.5	
t_{PLH}	A or B	Y	C_L = 50 pF		8.7	12.3	1	14	ns
t_{PHL}					8.7	12.3	1	14	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHC08					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A or B	Y	C_L = 15 pF		4.3	5.9	1	7	ns
t_{PHL}*					4.3	5.9	1	7	
t_{PLH}	A or B	Y	C_L = 50 pF		5.8	7.9	1	9	ns
t_{PHL}					5.8	7.9	1	9	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHC08					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		4.3	5.9	1	7	ns
t_{PHL}					4.3	5.9	1	7	
t_{PLH}	A or B	Y	C_L = 50 pF		5.8	7.9	1	9	ns
t_{PHL}					5.8	7.9	1	9	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

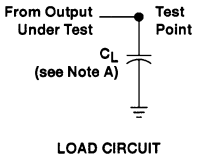
PARAMETER		SN74AHC08			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			–0.8	V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

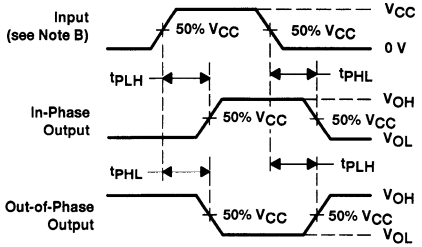
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	18	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES

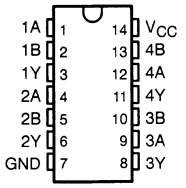
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

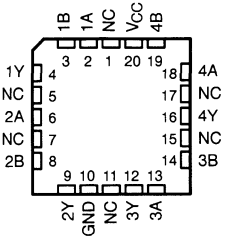
SCLS237A – OCTOBER 1995 – REVISED MARCH 1996

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHCT08 . . . J OR W PACKAGE
SN74AHCT08 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT08 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AHCT08 are quadruple 2-input positive-AND gates. These devices perform the Boolean function $Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

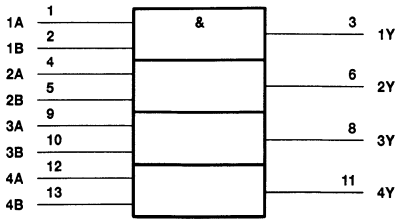
The SN54AHCT08 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT08 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHCT08		SN74AHCT08		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT08		SN74AHCT08		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		3.15		V
	I_{OH} = –8 mA		2.5			2.4		2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			2		20		20	μA
ΔI_{CC}†	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
I_{off}	V_O = 5.5 V	0 V			0.5*				5	μA
C_i	$V_I = V_{CC}$ or GND	5 V		4	10				10	pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT08				UNIT
				T_A = 25°C			MIN MAX	
				MIN	TYP	MAX		
t_{PLH}*	A or B	Y	C_L = 15 pF		5	6.9	1 8	ns
t_{PHL}*					5	6.9	1 8	
t_{PLH}	A or B	Y	C_L = 50 pF		5.5	7.9	1 9	ns
t_{PHL}					5.5	7.9	1 9	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT08				UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		5	6.9	1	8	ns
t_{PHL}					5	6.9	1	8	
t_{PLH}	A or B	Y	C_L = 50 pF		5.5	7.9	1	9	ns
t_{PHL}					5.5	7.9	1	9	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

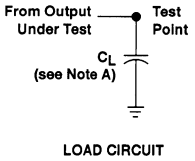
PARAMETER		SN74AHCT08			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.4	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.4	–0.8	V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

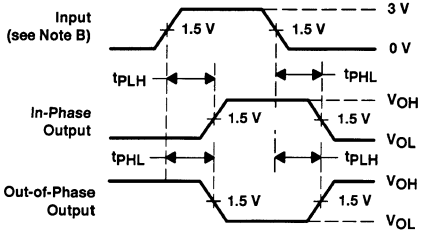
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	18	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES

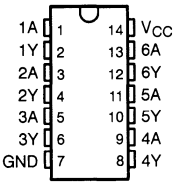
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

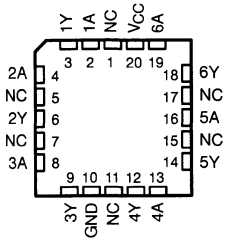
SCLS238B – OCTOBER 1995 – REVISED MARCH 1996

- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHC14 . . . J OR W PACKAGE
SN74AHC14 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC14 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AHC14 contain six independent inverters. These devices perform the Boolean function $Y = \overline{A}$.

Each circuit functions as an independent inverter, but because of the Schmitt action, the inverters have different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

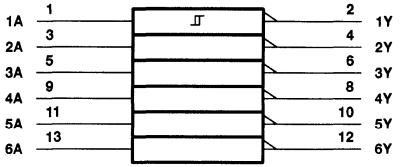
The SN54AHC14 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC14 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUT A	OUTPUT Y
H	L
L	H

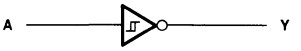
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... − 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			SN54AHC14		SN74AHC14		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC14		SN74AHC14		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{T+} Positive-going input threshold voltage		3 V			2.2		2.2		2.2	V
		4.5 V			3.15		3.15		3.15	
		5.5 V			3.85		3.85		3.85	
V_{T-} Negative-going input threshold voltage		3 V	0.9			0.9		0.9		V
		4.5 V	1.35			1.35		1.35		
		5.5 V	1.65			1.65		1.65		
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)		3 V	0.3		1.2	0.3	1.2	0.3	1.2	V
		4.5 V	0.4		1.4	0.4	1.4	0.4	1.4	
		5.5 V	0.5		1.6	0.5	1.6	0.5	1.6	
V_{OH}	I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
	I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20		20	μA
C_i	V_I = V_{CC} or GND	5 V		2	10				10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHC14					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A	Y	C_L = 15 pF		8.3	12.8	1	15	ns
t_{PHL}*					8.3	12.8	1	15	
t_{PLH}	A	Y	C_L = 50 pF		10.8	16.3	1	18.5	ns
t_{PHL}					10.8	16.3	1	18.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHC14					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		8.3	12.8	1	15	ns
t_{PHL}					8.3	12.8	1	15	
t_{PLH}	A	Y	C_L = 50 pF		10.8	16.3	1	18.5	ns
t_{PHL}					10.8	16.3	1	18.5	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHC14					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A	Y	C_L = 15 pF		5.5	8.6	1	10	ns
t_{PHL}*					5.5	8.6	1	10	
t_{PLH}	A	Y	C_L = 50 pF		7	10.6	1	12	ns
t_{PHL}					7	10.6	1	12	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHC14					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		5.5	8.6	1	10	ns
t_{PHL}					5.5	8.6	1	10	
t_{PLH}	A	Y	C_L = 50 pF		7	10.6	1	12	ns
t_{PHL}					7	10.6	1	12	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, $t_r = t_f$ = 3 ns, T_A = 25°C (see Note 4)

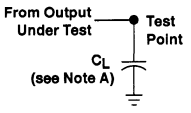
PARAMETER		SN74AHC14			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.4		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.6		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

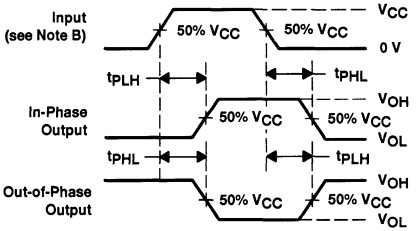
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	9	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



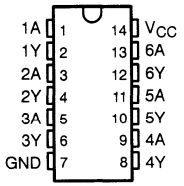
VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

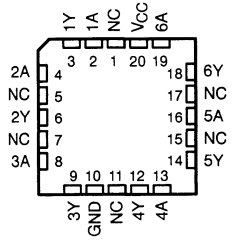
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHCT14 . . . J OR W PACKAGE
SN74AHCT14 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT14 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AHCT14 contain six independent inverters. These devices perform the Boolean function $Y = \overline{A}$.

Each circuit functions as an independent inverter, but because of the Schmitt action, the inverters have different input threshold levels for positive-going (V_{T+}) and for negative-going (V_{T-}) signals.

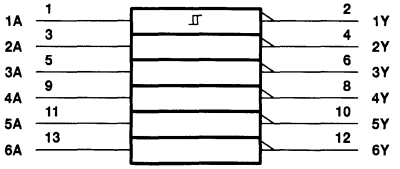
The SN54AHCT14 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT14 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

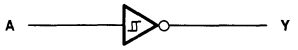
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHCT14		SN74AHCT14		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2.1		2.1		V
V_{IL}	Low-level input voltage		0.5		0.5	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT14		SN74AHCT14		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{T+} Positive-going input threshold voltage		4.5 V			2		2		2	V
		5.5 V			2		2		2	
V_{T-} Negative-going input threshold voltage		4.5 V	0.3			0.3		0.6		V
		5.5 V	0.6			0.6		0.6		
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)		4.5 V	0.4		1.4	0.4	1.4	0.4	1.4	V
		5.5 V	0.5		1.6	0.5	1.6	0.5	1.6	
V_{OH}	I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		3.15		V
	I_{OH} = –8 mA	4.5 V	2.5			2.4		2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA	4.5 V			0.36		0.44		0.44	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			2		20		20	μA
C_i	$V_I = V_{CC}$ or GND	5 V		2	10				10	pF

switching characteristics over recommended operating free-air temperature range V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT14					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A	Y	C_L = 15 pF		4	7	1	8	ns
t_{PHL}*					4	7	1	8	
t_{PLH}	A	Y	C_L = 50 pF		5.5	8	1	9	ns
t_{PHL}					5.5	8	1	9	

On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT14					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		4	7	1	8	ns
t_{PHL}					4	7	1	8	
t_{PLH}	A	Y	C_L = 50 pF		5.5	8	1	9	ns
t_{PHL}					5.5	8	1	9	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

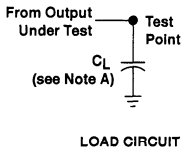
PARAMETER		SN74AHCT14			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.9		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.7		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.3		V
$V_{IH(D)}$	High-level dynamic input voltage	2.1			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.5	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

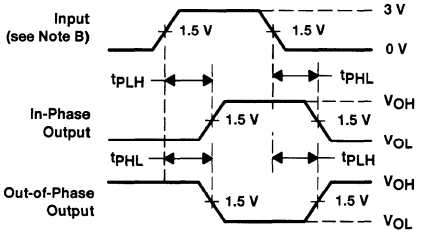
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	12	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES

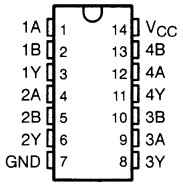
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

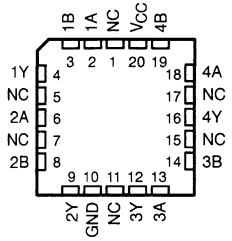
SCLS247A – OCTOBER 1995 – REVISED MARCH 1996

- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHC32 . . . J OR W PACKAGE
SN74AHC32 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC32 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AHC32 are quadruple 2-input positive-OR gates. These devices perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = A + B$ in positive logic.

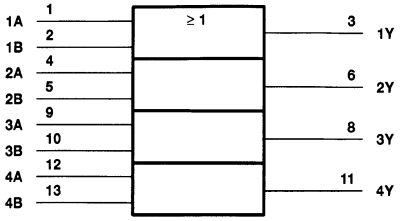
The SN54AHC32 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC32 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

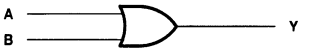
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			SN54AHC32		SN74AHC32		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC32		SN74AHC32		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
			3 V	2.9	3		2.9		2.9		
			4.5 V	4.4	4.5		4.4		4.4		
		I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
		I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
			3 V			0.1		0.1		0.1	
			4.5 V			0.1		0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	A or B inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20		20	μA
C_i		V_I = V_{CC} or GND	5 V		2	10				10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHC32					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A or B	Y	C_L = 15 pF		5.5	7.9	1	9.5	ns
t_{PHL}*					5.5	7.9	1	9.5	
t_{PLH}	A or B	Y	C_L = 50 pF		8	11.4	1	13	ns
t_{PHL}					8	11.4	1	13	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHC32					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		5.5	7.9	1	9.5	ns
t_{PHL}					5.5	7.9	1	9.5	
t_{PLH}	A or B	Y	C_L = 50 pF		8	11.4	1	13	ns
t_{PHL}					8	11.4	1	13	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHC32					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A or B	Y	C_L = 15 pF		3.8	5.5	1	6.5	ns
t_{PHL}*					3.8	5.5	1	6.5	
t_{PLH}	A or B	Y	C_L = 50 pF		5.3	7.5	1	8.5	ns
t_{PHL}					5.3	7.5	1	8.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHC32					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		3.8	5.5	1	6.5	ns
t_{PHL}					3.8	5.5	1	6.5	
t_{PLH}	A or B	Y	C_L = 50 pF		5.3	7.5	1	8.5	ns
t_{PHL}					5.3	7.5	1	8.5	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

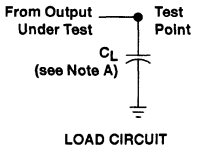
PARAMETER		SN74AHC32			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.3	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.3	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.7		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

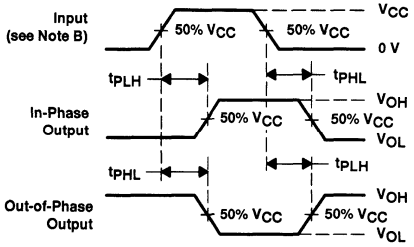
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	14	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



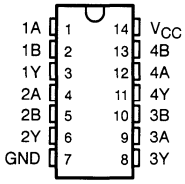
VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

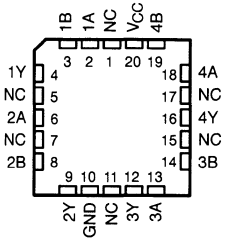
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHCT32 . . . J OR W PACKAGE
SN74AHCT32 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT32 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AHCT32 are quadruple 2-input positive-OR gates. These devices perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = A + B$ in positive logic.

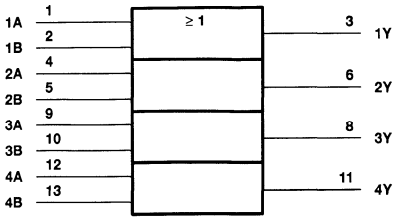
The SN54AHCT32 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT32 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DW, J, N, PW, and W packages.

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHCT32		SN74AHCT32		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT32		SN74AHCT32		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		3.15		V
	I_{OH} = –8 mA		2.5			2.4		2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			2		20		20	μA
ΔI_{CC}†	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
I_{off}	V_O = 5.5 V	0 V			0.5*				5	μA
C_i	$V_I = V_{CC}$ or GND	5 V		2	10				10	pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT32				UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A or B	Y	C_L = 15 pF		5	6.9	1	8	ns
t_{PHL}*					5	6.9	1	8	
t_{PLH}	A or B	Y	C_L = 50 pF		5.5	7.9	1	9	ns
t_{PHL}					5.5	7.9	1	9	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT32				UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		5	6.9	1	8	ns
t_{PHL}					5	6.9	1	8	
t_{PLH}	A or B	Y	C_L = 50 pF		5.5	7.9	1	9	ns
t_{PHL}					5.5	7.9	1	9	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

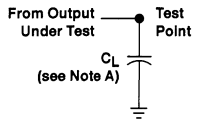
PARAMETER		SN74AHCT32			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.4	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.4	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.5		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

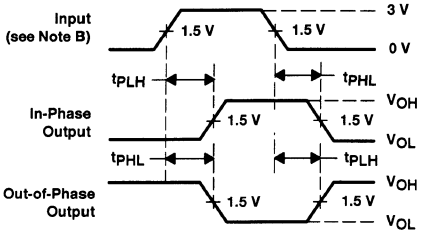
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	11.5	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



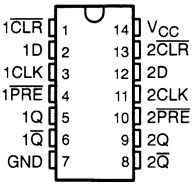
VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

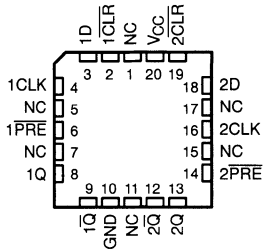
Figure 1. Load Circuit and Voltage Waveforms

- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHC74 . . . J OR W PACKAGE
SN74AHC74 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC74 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AHC74 are dual positive-edge-triggered D-type flip-flops.

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The SN54AHC74 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC74 is characterized for operation from –40°C to 85°C.

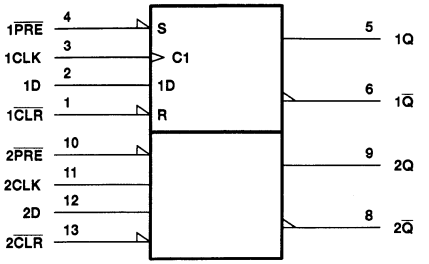
FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

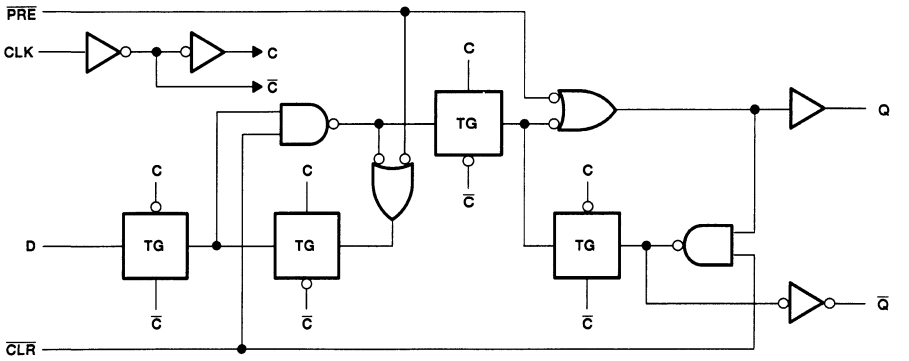
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			SN54AHC74		SN74AHC74		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC74		SN74AHC74		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
			3 V	2.9	3		2.9		2.9		
			4.5 V	4.4	4.5		4.4		4.4		
		I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
		I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
			3 V			0.1		0.1		0.1	
			4.5 V			0.1		0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	Data inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
	Control inputs					±0.1		±1		±1	
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20		20	μA
C_i		V_I = V_{CC} or GND	5 V		2	10				10	pF

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54AHC74		SN74AHC74		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	6		7		7		ns
		CLK	6		7		7		
t_{su}	Setup time before CLK↑	Data	6		7		7		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	5		5		5		
t_h	Hold time, data after CLK↑		0.5		0.5		0.5		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54AHC74		SN74AHC74		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	5		5		5		ns
		CLK	5		5		5		
t_{su}	Setup time before CLK↑	Data	5		5		5		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	3		3		3		
t_h	Hold time, data after CLK↑		0.5		0.5		0.5		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC74					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	80	125		70		MHz
			C_L = 50 pF	50	75		45		
t_{PLH}*	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	C_L = 15 pF		7.6	12.3	1	14.5	ns
t_{PHL}*					7.6	12.3	1	14.5	
t_{PLH}*	CLK	Q or $\overline{Q}$	C_L = 15 pF		6.7	11.9	1	14	ns
t_{PHL}*					6.7	11.9	1	14	
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	C_L = 50 pF		10.1	15.8	1	18	ns
t_{PHL}					10.1	15.8	1	18	
t_{PLH}	CLK	Q or $\overline{Q}$	C_L = 50 pF		9.2	15.4	1	17.5	ns
t_{PHL}					9.2	15.4	1	17.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC74					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	80	125		70		MHz
			C_L = 50 pF	50	75		45		
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	C_L = 15 pF		7.6	12.3	1	14.5	ns
t_{PHL}					7.6	12.3	1	14.5	
t_{PLH}	CLK	Q or $\overline{Q}$	C_L = 15 pF		6.7	11.9	1	14	ns
t_{PHL}					6.7	11.9	1	14	
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	C_L = 50 pF		10.1	15.8	1	18	ns
t_{PHL}					10.1	15.8	1	18	
t_{PLH}	CLK	Q or $\overline{Q}$	C_L = 50 pF		9.2	15.4	1	17.5	ns
t_{PHL}					9.2	15.4	1	17.5	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC74					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	130	170		110		MHz
			C_L = 50 pF	90	115		75		
t_{PLH}*	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	C_L = 15 pF		4.8	7.7	1	9	ns
t_{PHL}*					4.8	7.7	1	9	
t_{PLH}*	CLK	Q or $\overline{Q}$	C_L = 15 pF		4.6	7.3	1	8.5	ns
t_{PHL}*					4.6	7.3	1	8.5	
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	C_L = 50 pF		6.3	9.7	1	11	ns
t_{PHL}					6.3	9.7	1	11	
t_{PLH}	CLK	Q or Q	C_L = 50 pF		6.1	9.3	1	10.5	ns
t_{PHL}					6.1	9.3	1	10.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC74					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	130	170		110		MHz
			C_L = 50 pF	90	115		75		
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	C_L = 15 pF		4.8	7.7	1	9	ns
t_{PHL}					4.8	7.7	1	9	
t_{PLH}	CLK	Q or $\overline{Q}$	C_L = 15 pF		4.6	7.3	1	8.5	ns
t_{PHL}					4.6	7.3	1	8.5	
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	C_L = 50 pF		6.3	9.7	1	11	ns
t_{PHL}					6.3	9.7	1	11	
t_{PLH}	CLK	Q or Q	C_L = 50 pF		6.1	9.3	1	10.5	ns
t_{PHL}					6.1	9.3	1	10.5	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

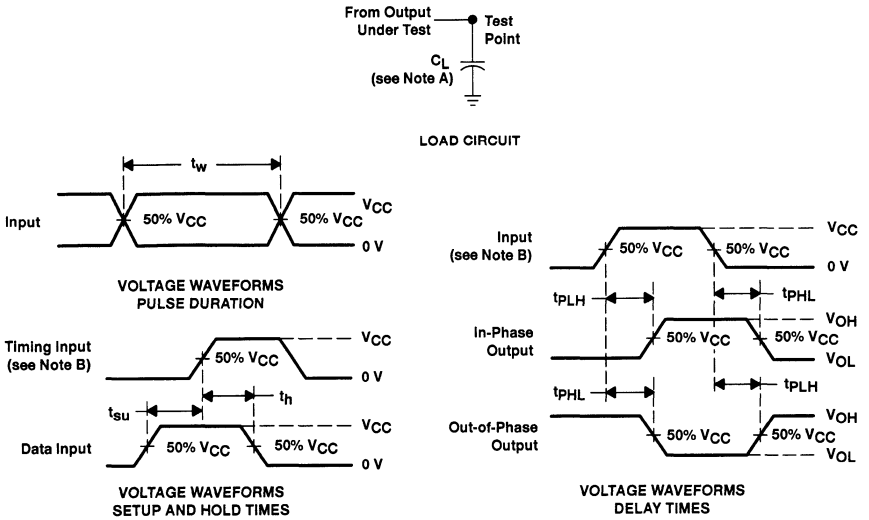
PARAMETER		SN74AHC74		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	4.7	–0.8	V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	32	pF

PARAMETER MEASUREMENT INFORMATION

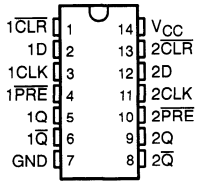


NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

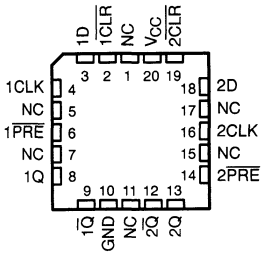
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHCT74 . . . J OR W PACKAGE
SN74AHCT74 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT74 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AHCT74 are dual positive-edge-triggered D-type flip-flops.

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The SN54AHCT74 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT74 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

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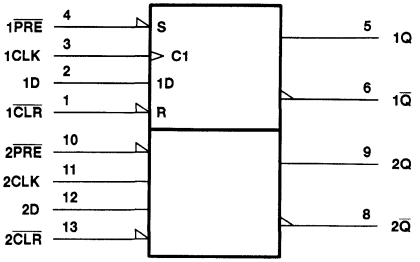
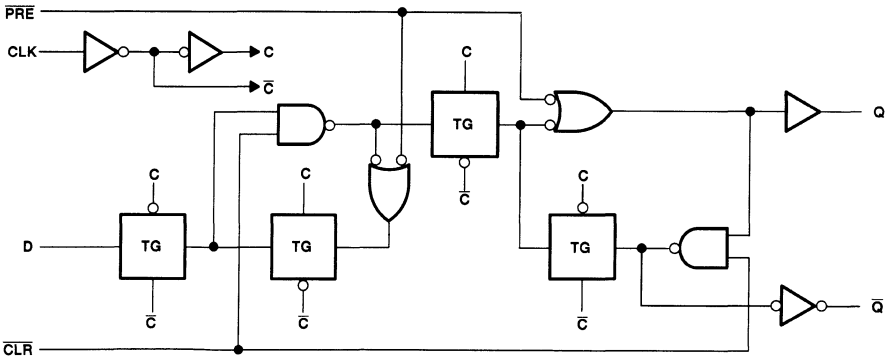
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram, each flip-flop (positive logic)



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHCT74		SN74AHCT74		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25°C$			SN54AHCT74		SN74AHCT74		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = –50\ \mu A$	4.5 V	3.15	3.65		3.15		3.15		V
	$I_{OH} = –8$ mA		2.5			2.4		2.4		
V_{OL}	$I_{OL} = 50\ \mu A$	4.5 V			0.1		0.1		0.1	V
	$I_{OL} = 8$ mA				0.36		0.5		0.44	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	µA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		20		20	µA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			1.35		1.5		1.5	mA
I_{off}	$V_O = 5.5$ V	0 V			0.5*				5	µA
C_i	$V_I = V_{CC}$ or GND	5 V		2	10				10	pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER			T_A = 25°C		SN54AHCT74		SN74AHCT74		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	5		5		5		ns
		CLK	5		5		5		
t_{su}	Setup time before CLK↑	Data	5		5		5		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	3.5		3.5		3.5		
t_h	Hold time, data after CLK↑		0		0		0		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT74					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	100	160		80		MHz
			C_L = 50 pF	80	140		65		
t_{PLH}*	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	C_L = 15 pF		7.6	10.4	1	12	ns
t_{PHL}*					7.6	10.4	1	12	
t_{PLH}*	CLK	Q or $\overline{Q}$	C_L = 15 pF		5.8	7.8	1	9	ns
t_{PHL}*					5.8	7.8	1	9	
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	C_L = 50 pF		8.1	11.4	1	13	ns
t_{PHL}					8.1	11.4	1	13	
t_{PLH}	CLK	Q or $\overline{Q}$	C_L = 50 pF		6.3	8.8	1	10	ns
t_{PHL}					6.3	8.8	1	10	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT74					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	100	160		80		MHz
			C_L = 50 pF	80	140		65		
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	C_L = 15 pF		7.6	10.4	1	12	ns
t_{PHL}					7.6	10.4	1	12	
t_{PLH}	CLK	Q or $\overline{Q}$	C_L = 15 pF		5.8	7.8	1	9	ns
t_{PHL}					5.8	7.8	1	9	
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	C_L = 50 pF		8.1	11.4	1	13	ns
t_{PHL}					8.1	11.4	1	13	
t_{PLH}	CLK	Q or $\overline{Q}$	C_L = 50 pF		6.3	8.8	1	10	ns
t_{PHL}					6.3	8.8	1	10	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

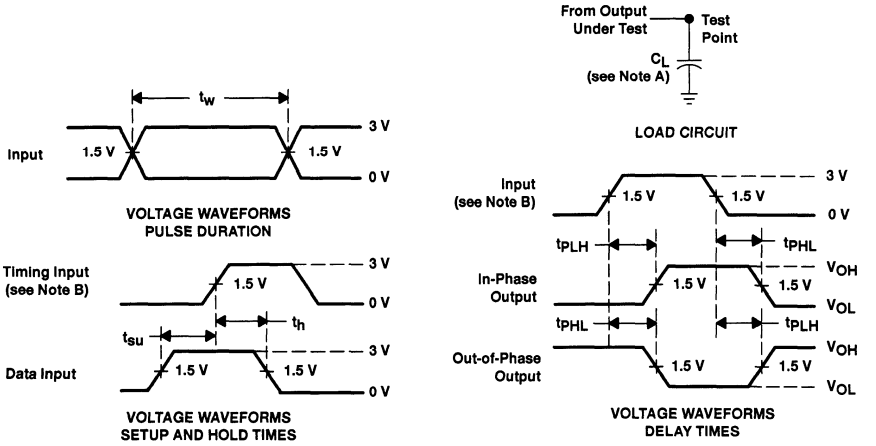
PARAMETER		SN74AHCT74 MIN	SN74AHCT74 MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4		V
$V_{IH(D)}$	High-level dynamic input voltage	2		V
$V_{IL(D)}$	Low-level dynamic input voltage		0.8	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	32	pF

PARAMETER MEASUREMENT INFORMATION



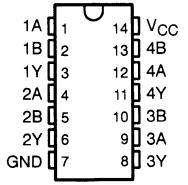
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

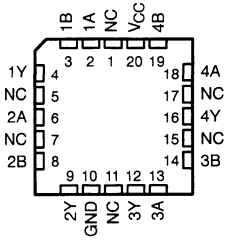
SCLS249A – OCTOBER 1995 – REVISED MARCH 1996

- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHC86 . . . J OR W PACKAGE
SN74AHC86 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC86 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AHC86 are quadruple 2-input exclusive-OR gates. These devices perform the Boolean function $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

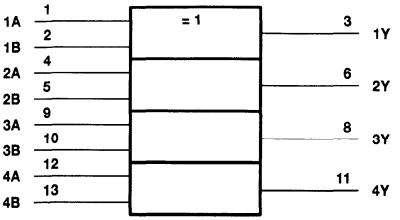
The SN54AHC86 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC86 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

EPIC is a trademark of Texas Instruments Incorporated.

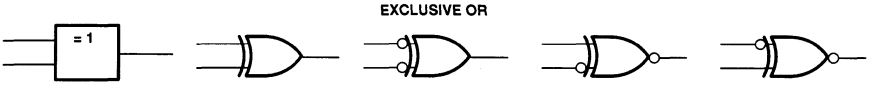
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

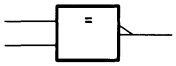
exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



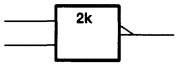
These are five equivalent exclusive-OR symbols valid for an SN74AHC86 gate in positive logic; negation may be shown at any two ports.

LOGIC-IDENTITY ELEMENT



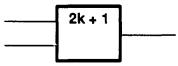
The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY ELEMENT



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			SN54AHC86		SN74AHC86		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54AHC86		SN74AHC86		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 μA		2 V	1.9	2		1.9		1.9		V
				3 V	2.9	3		2.9		2.9		
				4.5 V	4.4	4.5		4.4		4.4		
		I_{OH} = –4 mA		3 V	2.58			2.48		2.48		
		I_{OH} = –8 mA		4.5 V	3.94			3.8		3.8		
V_{OL}		I_{OL} = 50 μA		2 V			0.1		0.1		0.1	V
				3 V			0.1		0.1		0.1	
				4.5 V			0.1		0.1		0.1	
		I_{OL} = 4 mA		3 V			0.36		0.5		0.44	
		I_{OL} = 8 mA		4.5 V			0.36		0.5		0.44	
I_I	A or B inputs	$V_I = V_{CC}$ or GND		5.5 V			± 0.1		± 1		± 1	μA
I_{CC}		$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V			2		20		20	μA
C_i		$V_I = V_{CC}$ or GND		5 V		4	10				10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC86					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A or B	Y	C_L = 15 pF		7	11	1	13	ns
t_{PHL}*					7	11	1	13	
t_{PLH}	A or B	Y	C_L = 50 pF		9.5	14.5	1	16.5	ns
t_{PHL}					9.5	14.5	1	16.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC86					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		7	11	1	13	ns
t_{PHL}					7	11	1	13	
t_{PLH}	A or B	Y	C_L = 50 pF		9.5	14.5	1	16.5	ns
t_{PHL}					9.5	14.5	1	16.5	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC86				UNIT
				T_A = 25°C			MIN	MAX
				MIN	TYP	MAX		
t_{PLH}*	A or B	Y	C_L = 15 pF		4.8	6.8	1	8	ns
t_{PHL}*					4.8	6.8	1	8	
t_{PLH}	A or B	Y	C_L = 50 pF		6.3	8.8	1	10	ns
t_{PHL}					6.3	8.8	1	10	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC86				UNIT
				T_A = 25°C			MIN	MAX
				MIN	TYP	MAX		
t_{PLH}	A or B	Y	C_L = 15 pF		4.8	6.8	1	8	ns
t_{PHL}					4.8	6.8	1	8	
t_{PLH}	A or B	Y	C_L = 50 pF		6.3	8.8	1	10	ns
t_{PHL}					6.3	8.8	1	10	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

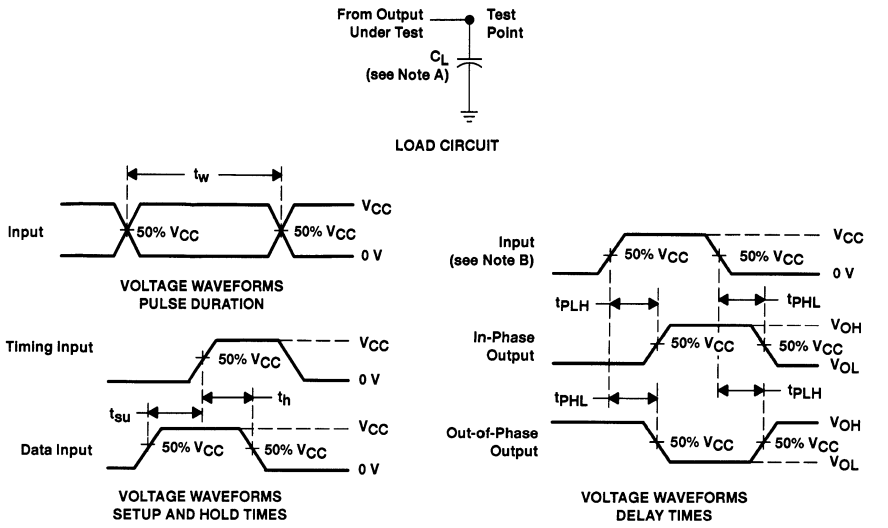
PARAMETER		SN74AHC86			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.3	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.3	–0.8	V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	18	pF

PARAMETER MEASUREMENT INFORMATION



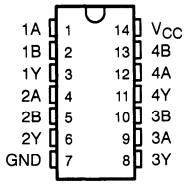
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

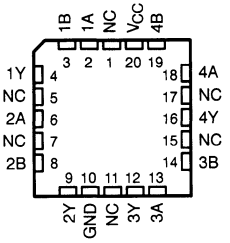
SCLS250B – OCTOBER 1995 – REVISED MARCH 1996

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHCT86 . . . J OR W PACKAGE
SN74AHCT86 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT86 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AHCT86 are quadruple 2-input exclusive-OR gates. These devices perform the Boolean function $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

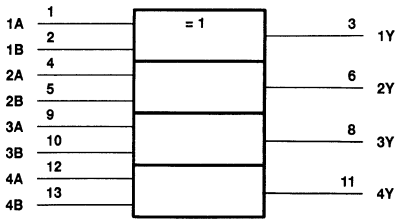
The SN54AHCT86 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT86 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

EPIC is a trademark of Texas Instruments Incorporated.

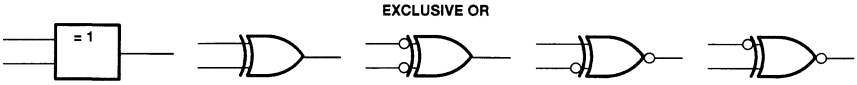
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

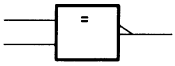
exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



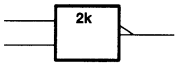
These are five equivalent exclusive-OR symbols valid for an SN74AHCT86 gate in positive logic; negation may be shown at any two ports.

LOGIC-IDENTITY ELEMENT



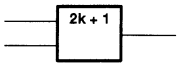
The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY ELEMENT



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHCT86		SN74AHCT86		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25°C$			SN54AHCT86		SN74AHCT86		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = –50\ \mu A$	4.5 V	3.15	3.65		3.15		3.15		V
	$I_{OH} = –8$ mA		2.5			2.4		2.4		
V_{OL}	$I_{OL} = 50\ \mu A$	4.5 V			0.1		0.1		0.1	V
	$I_{OL} = 8$ mA				0.36		0.44		0.44	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	µA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		20		20	µA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
I_{off}	$V_O = 5.5$ V	0 V			0.5*				5	µA
C_i	$V_I = V_{CC}$ or GND	5 V		4	10				10	pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT86					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A or B	Y	C_L = 15 pF		5	6.9	1	8	ns
t_{PHL}*					5	6.9	1	8	
t_{PLH}	A or B	Y	C_L = 50 pF		5.5	7.9	1	9	ns
t_{PHL}					5.5	7.9	1	9	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT86					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		5	6.9	1	8	ns
t_{PHL}					5	6.9	1	8	
t_{PLH}	A or B	Y	C_L = 50 pF		5.5	7.9	1	9	ns
t_{PHL}					5.5	7.9	1	9	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

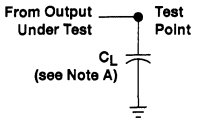
PARAMETER		SN74AHCT86			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.4	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.4	–0.8	V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

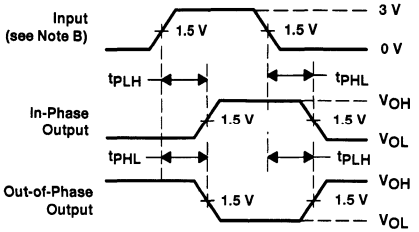
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	18	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



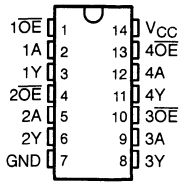
VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

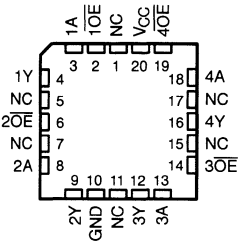
Figure 1. Load Circuit and Voltage Waveforms

- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHC125 . . . J OR W PACKAGE
SN74AHC125 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC125 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AHC125 are quadruple bus buffer gates featuring independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ($\overline{OE}$) input is high. When $\overline{OE}$ is low, the respective gate passes the data from the A input to its Y output.

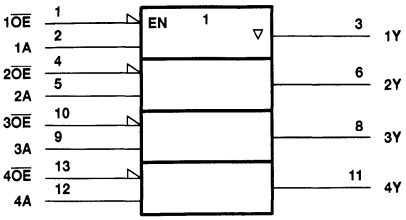
The SN54AHC125 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC125 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

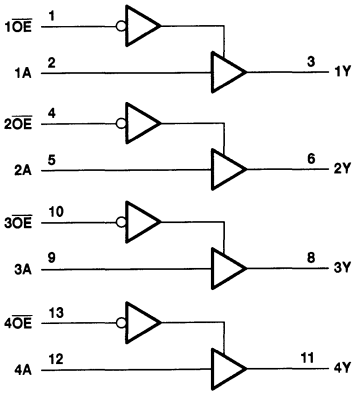
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			SN54AHC125		SN74AHC125		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	Vcc = 3.3 V ± 0.3 V		100		100	ns/V
		Vcc = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	– 40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC125		SN74AHC125		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = – 50 μA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I_{OH} = – 4 mA	3 V	2.58			2.48		2.48		
	I_{OH} = – 8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I A or $\overline{OE}$ inputs	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{OZ}	$V_I = V_{CC}$ or GND	5.5 V			± 0.25		± 2.5		± 2.5	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		40		40	μA
C_i	$V_I = V_{CC}$ or GND	5 V		4	10				10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC125					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A	Y	C_L = 15 pF		5.6	8	1	9.5	ns
t_{PHL}*					5.6	8	1	9.5	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		5.4	8	1	9.5	ns
t_{PZL}*					5.4	8	1	9.5	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		7	9.7	1	11.5	ns
t_{PLZ}*					7	9.7	1	11.5	
t_{PLH}	A	Y	C_L = 50 pF		8.1	11.5	1	13	ns
t_{PHL}					8.1	11.5	1	13	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		7.9	11.5	1	13	ns
t_{PZL}					7.9	11.5	1	13	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		9.5	13.2	1	15	ns
t_{PLZ}					9.5	13.2	1	15	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC125					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		5.6	8	1	9.5	ns
t_{PHL}					5.6	8	1	9.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF		5.4	8	1	9.5	ns
t_{PLL}					5.4	8	1	9.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF		7	9.7	1	11.5	ns
t_{PLZ}					7	9.7	1	11.5	
t_{PLH}	A	Y	C_L = 50 pF		8.1	11.5	1	13	ns
t_{PHL}					8.1	11.5	1	13	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		7.9	11.5	1	13	ns
t_{PZL}					7.9	11.5	1	13	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		9.5	13.2	1	15	ns
t_{PLZ}					9.5	13.2	1	15	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC125					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A	Y	C_L = 15 pF		3.8	5.5	1	6.5	ns
t_{PHL}*					3.8	5.5	1	6.5	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		3.6	5.1	1	6	ns
t_{PZL}*					3.6	5.1	1	6	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		4.6	6.8	1	8	ns
t_{PLZ}*					4.6	6.8	1	8	
t_{PLH}	A	Y	C_L = 50 pF		5.3	7.5	1	8.5	ns
t_{PHL}					5.3	7.5	1	8.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		5.1	7.1	1	8	ns
t_{PZL}					5.1	7.1	1	8	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		6.1	8.8	1	10	ns
t_{PLZ}					6.1	8.8	1	10	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC125					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		3.8	5.5	1	6.5	ns
t_{PHL}					3.8	5.5	1	6.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF		3.6	5.1	1	6	ns
t_{PZL}					3.6	5.1	1	6	
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF		4.6	6.8	1	8	ns
t_{PLZ}					4.6	6.8	1	8	
t_{PLH}	A	Y	C_L = 50 pF		5.3	7.5	1	8.5	ns
t_{PHL}					5.3	7.5	1	8.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		5.1	7.1	1	8	ns
t_{PZL}					5.1	7.1	1	8	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		6.1	8.8	1	10	ns
t_{PLZ}					6.1	8.8	1	10	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHC125				UNIT
			T_A = 25°C		MIN	MAX	
			MIN	MAX			
$t_{sk(o)}$	Output skew	3.3 V ± 0.3 V		1.5		1.5	ns
		5 V ± 0.5 V		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

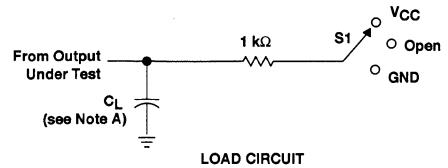
PARAMETER		SN74AHC125			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.4			V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

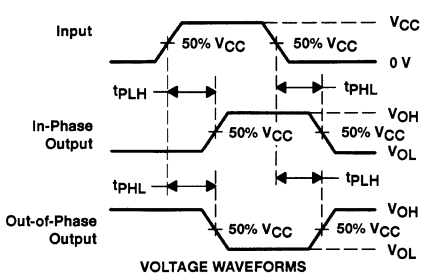
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	14	pF

PARAMETER MEASUREMENT INFORMATION

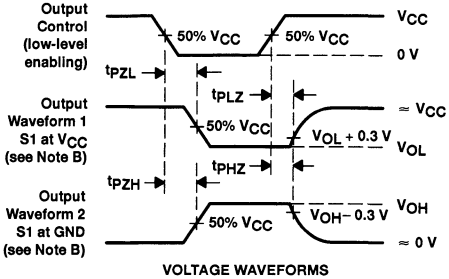


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
DELAY TIMES



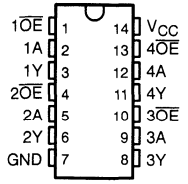
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

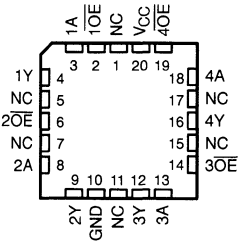
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHCT125 . . . J OR W PACKAGE
SN74AHCT125 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT125 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AHCT125 are quadruple bus buffer gates featuring independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ($\overline{OE}$) input is high. When $\overline{OE}$ is low, the respective gate passes the data from the A input to its Y output.

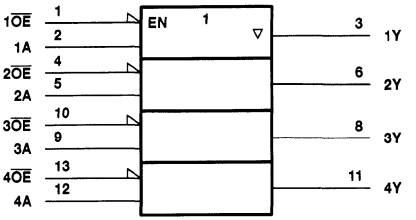
The SN54AHCT125 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT125 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

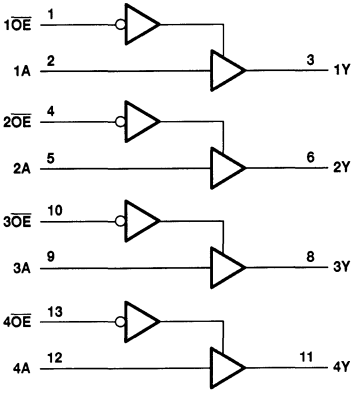
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHCT125		SN74AHCT125		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	$T_A = 25°C$			SN54AHCT125		SN74AHCT125		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		$I_{OH} = –50\ \mu A$	4.5 V	3.15	3.65		3.15		3.15		V
		$I_{OH} = –8$ mA		2.5			2.4		2.4		
V_{OL}		$I_{OL} = 50\ \mu A$	4.5 V			0.1		0.1		0.1	V
		$I_{OL} = 8$ mA				0.36		0.44		0.44	
I_I	A or $\overline{OE}$ inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	µA
I_{OZ}		$V_O = V_{CC}$ or GND	5.5 V			±0.25		±2.5		±2.5	µA
I_{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		20		20	µA
ΔI_{CC}‡		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
C_i		$V_I = V_{CC}$ or GND	5 V		4	10				10	pF
C_o		$V_O = V_{CC}$ or GND	5 V		15						pF

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT125					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A	Y	C_L = 15 pF		3.8	5.5	1	6.5	ns
t_{PHL}*					3.8	5.5	1	6.5	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		3.6	5.1	1	6	ns
t_{PZL}*					3.6	5.1	1	6	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		4.6	6.8	1	8	ns
t_{PLZ}*					4.6	6.8	1	8	
t_{PLH}	A	Y	C_L = 50 pF		5.3	7.5	1	8.5	ns
t_{PHL}					5.3	7.5	1	8.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		5.1	7.1	1	8	ns
t_{PZL}					5.1	7.1	1	8	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		6.1	8.8	1	10	ns
t_{PLZ}					6.1	8.8	1	10	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT125					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		3.8	5.5	1	6.5	ns
t_{PHL}					3.8	5.5	1	6.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF		3.6	5.1	1	6	ns
t_{PZL}					3.6	5.1	1	6	
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF		4.6	6.8	1	8	ns
t_{PLZ}					4.6	6.8	1	8	
t_{PLH}	A	Y	C_L = 50 pF		5.3	7.5	1	8.5	ns
t_{PHL}					5.3	7.5	1	8.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		5.1	7.1	1	8	ns
t_{PZL}					5.1	7.1	1	8	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		6.1	8.8	1	10	ns
t_{PLZ}					6.1	8.8	1	10	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN74AHCT125					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
$t_{sk(o)}$	A	Y	5 V ± 0.5 V			1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

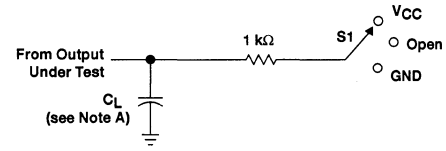
PARAMETER		SN74AHCT125		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.4		V
$V_{IH(D)}$	High-level dynamic input voltage	2		V
$V_{IL(D)}$	Low-level dynamic input voltage		0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

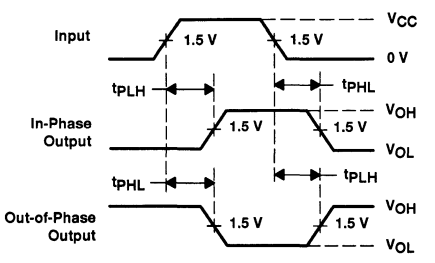
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	14	pF

PARAMETER MEASUREMENT INFORMATION

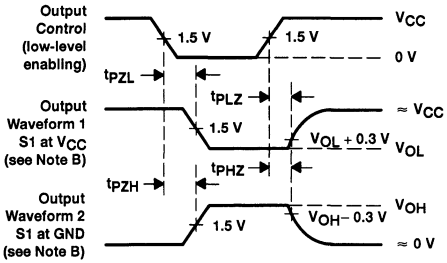


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
DELAY TIMES



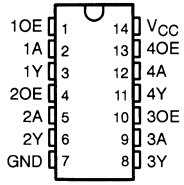
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

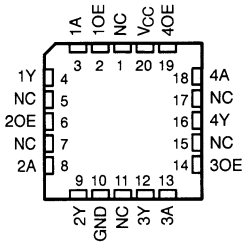
Figure 1. Load Circuit and Voltage Waveforms

- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHC126 . . . J OR W PACKAGE
SN74AHC126 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC126 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AHC126 are quadruple bus buffer gates featuring independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low. When OE is high, the respective gate passes the data from the A input to its Y output.

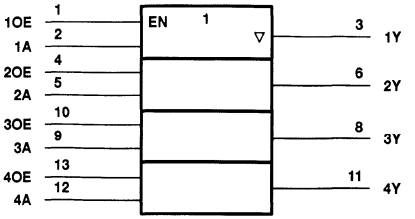
The SN54AHC126 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC126 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z

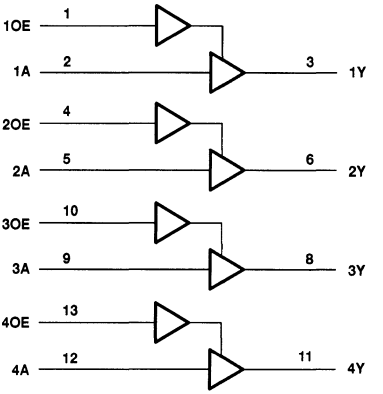
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... − 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			SN54AHC126		SN74AHC126		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		−50		−50	μA
		V_{CC} = 3.3 V ± 0.3 V		−4		−4	mA
		V_{CC} = 5 V ± 0.5 V		−8		−8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	Vcc = 3.3 V ± 0.3 V		100		100	ns/V
		Vcc = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC126		SN74AHC126		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = – 50 μA	2 V	1.9	2		1.9		1.9		V
			3 V	2.9	3		2.9		2.9		
			4.5 V	4.4	4.5		4.4		4.4		
		I_{OH} = – 4 mA	3 V	2.58			2.48		2.48		
		I_{OH} = – 8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
			3 V			0.1		0.1		0.1	
			4.5 V			0.1		0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	A or OE inputs	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{OZ}		V_I = V_{CC} or GND	5.5 V			± 0.25		± 2.5		± 2.5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
C_i		V_I = V_{CC} or GND	5 V		4	10				10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC126					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A	Y	C_L = 15 pF		5.6	8	1	9.5	ns
t_{PHL}*					5.6	8	1	9.5	
t_{PZH}*	OE	Y	C_L = 15 pF		5.4	8	1	9.5	ns
t_{PZL}*					5.4	8	1	9.5	
t_{PHZ}*	OE	Y	C_L = 15 pF		7	9.7	1	11.5	ns
t_{PLZ}*					7	9.7	1	11.5	
t_{PLH}	A	Y	C_L = 50 pF		8.1	11.5	1	13	ns
t_{PHL}					8.1	11.5	1	13	
t_{PZH}	OE	Y	C_L = 50 pF		7.9	11.5	1	13	ns
t_{PZL}					7.9	11.5	1	13	
t_{PHZ}	OE	Y	C_L = 50 pF		9.5	13.2	1	15	ns
t_{PLZ}					9.5	13.2	1	15	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC126					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		5.6	8	1	9.5	ns
t_{PHL}					5.6	8	1	9.5	
t_{PZH}	OE	Y	C_L = 15 pF		5.4	8	1	9.5	ns
t_{PZL}					5.4	8	1	9.5	
t_{PHZ}	OE	Y	C_L = 15 pF		7	9.7	1	11.5	ns
t_{PLZ}					7	9.7	1	11.5	
t_{PLH}	A	Y	C_L = 50 pF		8.1	11.5	1	13	ns
t_{PHL}					8.1	11.5	1	13	
t_{PZH}	OE	Y	C_L = 50 pF		7.9	11.5	1	13	ns
t_{PZL}					7.9	11.5	1	13	
t_{PHZ}	OE	Y	C_L = 50 pF		9.5	13.2	1	15	ns
t_{PLZ}					9.5	13.2	1	15	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC126					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A	Y	C_L = 15 pF		3.8	5.5	1	6.5	ns
t_{PHL}*					3.8	5.5	1	6.5	
t_{PZH}*	OE	Y	C_L = 15 pF		3.6	5.1	1	6	ns
t_{PZL}*					3.6	5.1	1	6	
t_{PHZ}*	OE	Y	C_L = 15 pF		4.6	6.8	1	8	ns
t_{PLZ}*					4.6	6.8	1	8	
t_{PLH}	A	Y	C_L = 50 pF		5.3	7.5	1	8.5	ns
t_{PHL}					5.3	7.5	1	8.5	
t_{PZH}	OE	Y	C_L = 50 pF		5.1	7.1	1	8	ns
t_{PZL}					5.1	7.1	1	8	
t_{PHZ}	OE	Y	C_L = 50 pF		6.1	8.8	1	10	ns
t_{PLZ}					6.1	8.8	1	10	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC126					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		3.8	5.5	1	6.5	ns
t_{PHL}					3.8	5.5	1	6.5	
t_{PZH}	OE	Y	C_L = 15 pF		3.6	5.1	1	6	ns
t_{PZL}					3.6	5.1	1	6	
t_{PHZ}	OE	Y	C_L = 15 pF		4.6	6.8	1	8	ns
t_{PLZ}					4.6	6.8	1	8	
t_{PLH}	A	Y	C_L = 50 pF		5.3	7.5	1	8.5	ns
t_{PHL}					5.3	7.5	1	8.5	
t_{PZH}	OE	Y	C_L = 50 pF		5.1	7.1	1	8	ns
t_{PZL}					5.1	7.1	1	8	
t_{PHZ}	OE	Y	C_L = 50 pF		6.1	8.8	1	10	ns
t_{PLZ}					6.1	8.8	1	10	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHC126				UNIT
			T_A = 25°C		MIN	MAX	
			MIN	MAX			
$t_{sk(o)}$	Output skew	3.3 V ± 0.3 V		1.5		1.5	ns
		5 V ± 0.5 V		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

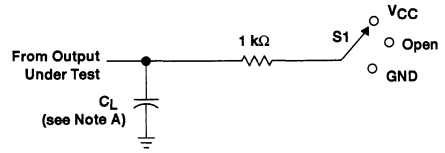
PARAMETER		SN74AHC126			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.4			V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

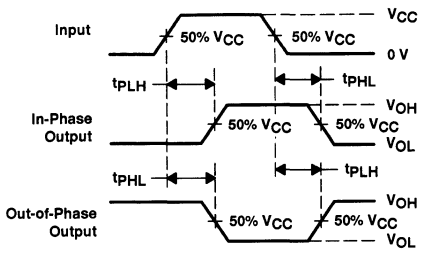
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	14	pF

PARAMETER MEASUREMENT INFORMATION

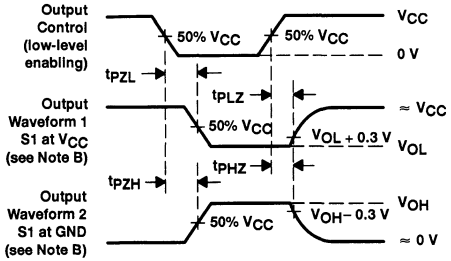


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
DELAY TIMES



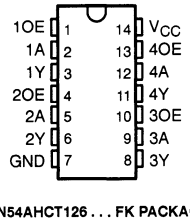
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

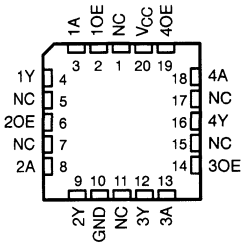
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHCT126 . . . J OR W PACKAGE
SN74AHCT126 . . . D, DB, N OR PW PACKAGE
(TOP VIEW)



SN54AHCT126 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AHCT126 are quadruple bus buffer gates featuring independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low. When OE is high, the respective gate passes the data from the A input to its Y output.

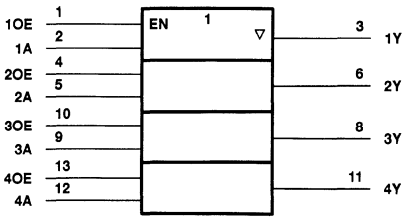
The SN54AHCT126 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT126 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z

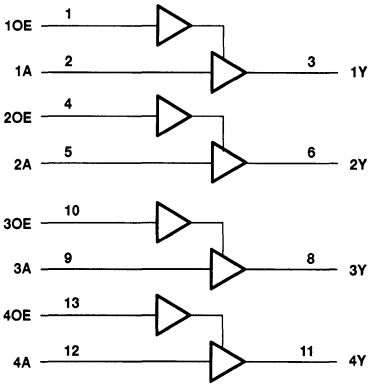
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHCT126		SN74AHCT126		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT126		SN74AHCT126		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		3.15		V
		I_{OH} = –8 mA		2.5			2.4		2.4		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		I_{OL} = 8 mA				0.36		0.44		0.44	
I_I	A or OE inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}		$V_O = V_{CC}$ or GND	5.5 V			±0.25		±2.5		±2.5	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			2		20		20	μA
ΔI_{CC}‡		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
C_i		$V_I = V_{CC}$ or GND	5 V		4	10				10	pF
C_o		$V_O = V_{CC}$ or GND	5 V		15						pF

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT126					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A	Y	C_L = 15 pF		3.8	5.5	1	6.5	ns
t_{PHL}*					3.8	5.5	1	6.5	
t_{PZH}*	OE	Y	C_L = 15 pF		3.6	5.1	1	6	ns
t_{PZL}*					3.6	5.1	1	6	
t_{PHZ}*	OE	Y	C_L = 15 pF		4.6	6.8	1	8	ns
t_{PLZ}*					4.6	6.8	1	8	
t_{PLH}	A	Y	C_L = 50 pF		5.3	7.5	1	8.5	ns
t_{PHL}					5.3	7.5	1	8.5	
t_{PZH}	OE	Y	C_L = 50 pF		5.1	7.1	1	8	ns
t_{PZL}					5.1	7.1	1	8	
t_{PHZ}	OE	Y	C_L = 50 pF		6.1	8.8	1	10	ns
t_{PLZ}					6.1	8.8	1	10	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT126					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		3.8	5.5	1	6.5	ns
t_{PHL}					3.8	5.5	1	6.5	
t_{PZH}	OE	Y	C_L = 15 pF		3.6	5.1	1	6	ns
t_{PZL}					3.6	5.1	1	6	
t_{PHZ}	OE	Y	C_L = 15 pF		4.6	6.8	1	8	ns
t_{PLZ}					4.6	6.8	1	8	
t_{PLH}	A	Y	C_L = 50 pF		5.3	7.5	1	8.5	ns
t_{PHL}					5.3	7.5	1	8.5	
t_{PZH}	OE	Y	C_L = 50 pF		5.1	7.1	1	8	ns
t_{PZL}					5.1	7.1	1	8	
t_{PHZ}	OE	Y	C_L = 50 pF		6.1	8.8	1	10	ns
t_{PLZ}					6.1	8.8	1	10	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN74AHCT126					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
$t_{sk(o)}$	A	Y	5 V ± 0.5 V			1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

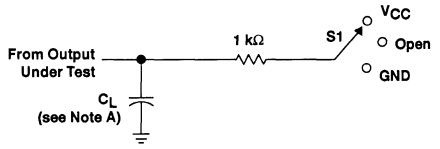
PARAMETER		SN74AHCT126 MIN	SN74AHCT126 MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.4		V
$V_{IH(D)}$	High-level dynamic input voltage	2		V
$V_{IL(D)}$	Low-level dynamic input voltage		0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

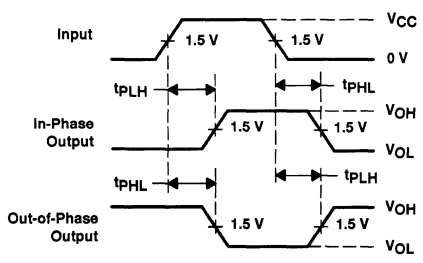
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	14	pF

PARAMETER MEASUREMENT INFORMATION

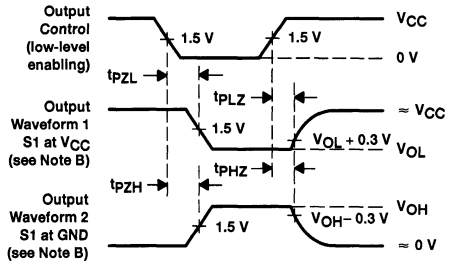


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

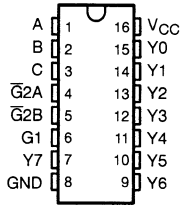
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

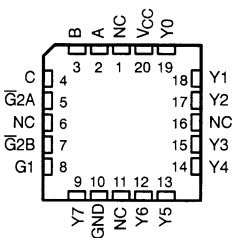
SCLS258C – DECEMBER 1995 – REVISED JULY 1996

- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporate Three Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHC138 . . . J OR W PACKAGE
SN74AHC138 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC138 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AHC138 decoders/demultiplexers are designed for high-performance memory-decoding or data-routing applications requiring very short propagation-delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN54AHC138 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC138 is characterized for operation from –40°C to 85°C.

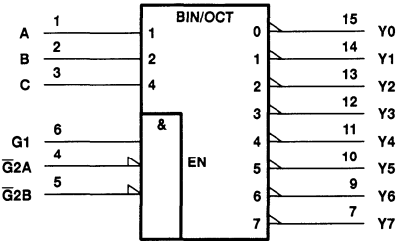
PRODUCT PREVIEW

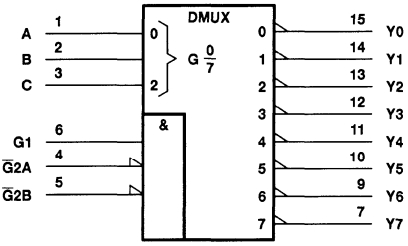
EPIC is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

logic symbols (alternatives)†

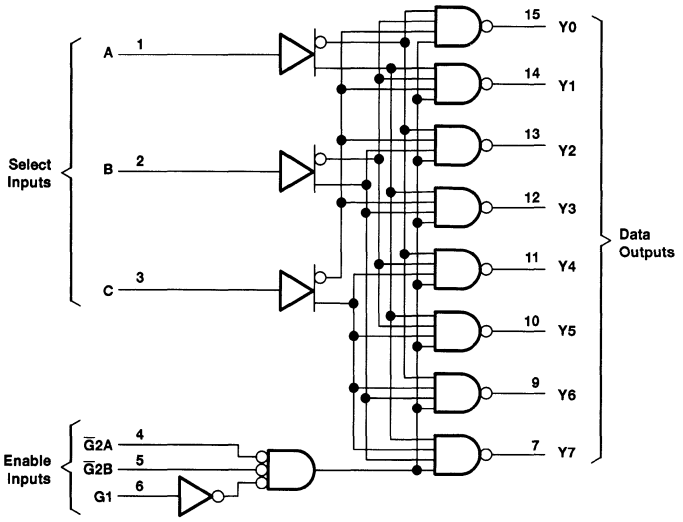




† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.3 W
DB package ..... 0.55 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

			SN54AHC138		SN74AHC138		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	Vcc = 3.3 V ± 0.3 V		100		100	ns/V
		Vcc = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC138		SN74AHC138		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = – 50 μA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I_{OH} = – 4 mA	3 V	2.58			2.48		2.48		
	I_{OH} = – 8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
C_i	V_I = V_{CC} or GND	5 V		4	10				10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHC138					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A, B, C	Any Y	C_L = 15 pF		8.2	11.4	1	13	ns
t_{PHL}*					8.2	11.4	1	13	
t_{PLH}*	G1	Any Y	C_L = 15 pF		8.1	12.8	1	15	ns
t_{PHL}*					8.1	12.8	1	15	
t_{PLH}*	$\overline{G}$2A, $\overline{G}$2B	Any Y	C_L = 15 pF		8.2	11.4	1	13.5	ns
t_{PHL}*					8.2	11.4	1	13.5	
t_{PLH}	A, B, C	Any Y	C_L = 50 pF		10	15.8	1	18	ns
t_{PHL}					10	15.8	1	18	
t_{PLH}	G1	Any Y	C_L = 50 pF		10.6	16.3	1	18.5	ns
t_{PHL}					10.6	16.3	1	18.5	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Any Y	C_L = 50 pF		10.7	14.9	1	17	ns
t_{PHL}					10.7	14.9	1	17	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHC138					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A, B, C	Any Y	C_L = 15 pF		8.2	11.4	1	13	ns
t_{PHL}					8.2	11.4	1	13	
t_{PLH}	G1	Any Y	C_L = 15 pF		8.1	12.8	1	15	ns
t_{PHL}					8.1	12.8	1	15	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Any Y	C_L = 15 pF		8.2	11.4	1	13.5	ns
t_{PHL}					8.2	11.4	1	13.5	
t_{PLH}	A, B, C	Any Y	C_L = 50 pF		10	15.8	1	18	ns
t_{PHL}					10	15.8	1	18	
t_{PLH}	G1	Any Y	C_L = 50 pF		10.6	16.3	1	18.5	ns
t_{PHL}					10.6	16.3	1	18.5	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Any Y	C_L = 50 pF		10.7	14.9	1	17	ns
t_{PHL}					10.7	14.9	1	17	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHC138					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A, B, C	Any Y	C_L = 15 pF		5.7	8.1	1	9.5	ns
t_{PHL}*					5.7	8.1	1	9.5	
t_{PLH}*	G1	Any Y	C_L = 15 pF		5.6	8.1	1	9.5	ns
t_{PHL}*					5.6	8.1	1	9.5	
t_{PLH}*	$\overline{G}$2A, $\overline{G}$2B	Any Y	C_L = 15 pF		5.8	8.1	1	9.5	ns
t_{PHL}*					5.8	8.1	1	9.5	
t_{PLH}	A, B, C	Any Y	C_L = 50 pF		7.2	10.1	1	11.5	ns
t_{PHL}					7.2	10.1	1	11.5	
t_{PLH}	G1	Any Y	C_L = 50 pF		7.1	10.1	1	11.5	ns
t_{PHL}					7.1	10.1	1	11.5	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Any Y	C_L = 50 pF		7.3	10.1	1	11.5	ns
t_{PHL}					7.3	10.1	1	11.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

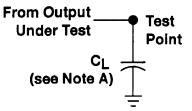
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHC138					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A, B, C	Any Y	C_L = 15 pF		5.7	8.1	1	9.5	ns
t_{PHL}					5.7	8.1	1	9.5	
t_{PLH}	G1	Any Y	C_L = 15 pF		5.6	8.1	1	9.5	ns
t_{PHL}					5.6	8.1	1	9.5	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Any Y	C_L = 15 pF		5.8	8.1	1	9.5	ns
t_{PHL}					5.8	8.1	1	9.5	
t_{PLH}	A, B, C	Any Y	C_L = 50 pF		7.2	10.1	1	11.5	ns
t_{PHL}					7.2	10.1	1	11.5	
t_{PLH}	G1	Any Y	C_L = 50 pF		7.1	10.1	1	11.5	ns
t_{PHL}					7.1	10.1	1	11.5	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Any Y	C_L = 50 pF		7.3	10.1	1	11.5	ns
t_{PHL}					7.3	10.1	1	11.5	

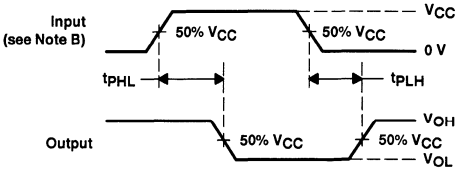
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load,	f = 1 MHz	34	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

APPLICATION INFORMATION

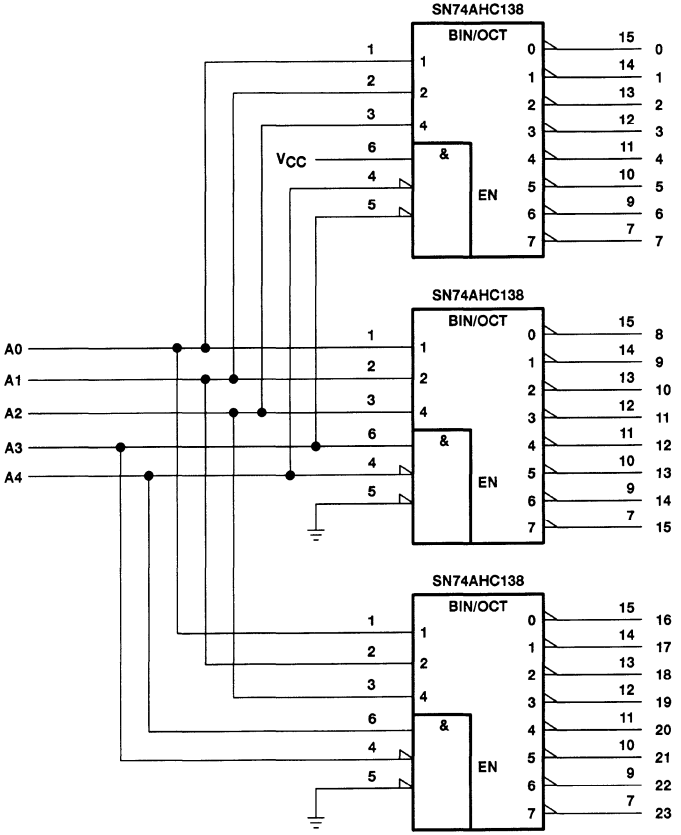


Figure 2. 24-Bit Decoding Scheme

APPLICATION INFORMATION

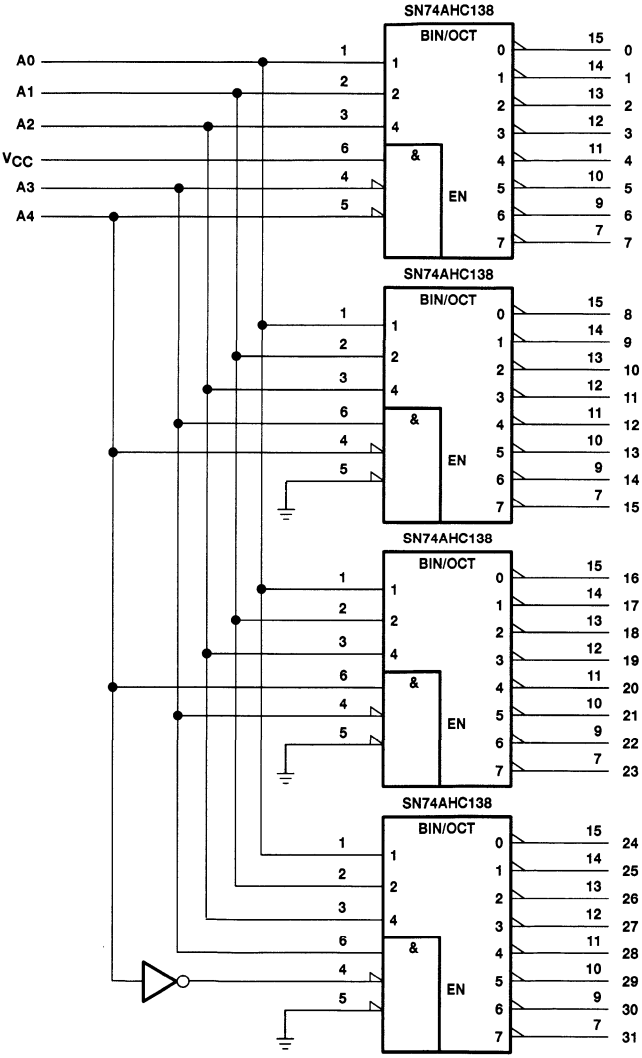
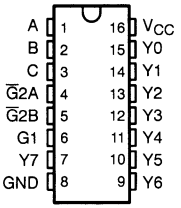


Figure 3. 32-Bit Decoding Scheme

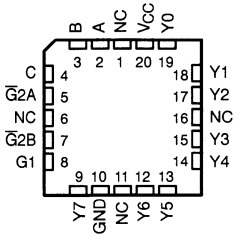
SCLS266B – DECEMBER 1995 – REVISED JULY 1996

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporate Three Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHCT138 . . . J OR W PACKAGE
SN74AHCT138 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT138 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AHCT138 3-line to 8-line decoders/demultiplexers are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN54AHCT138 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT138 is characterized for operation from –40°C to 85°C.

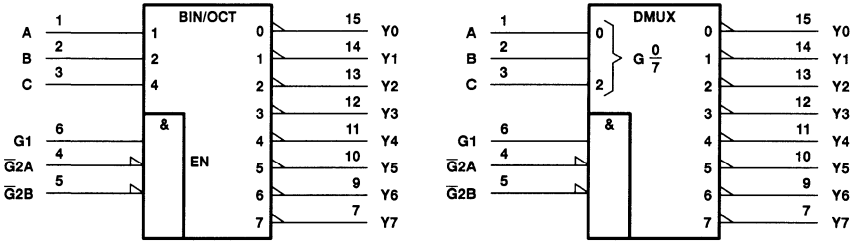
PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

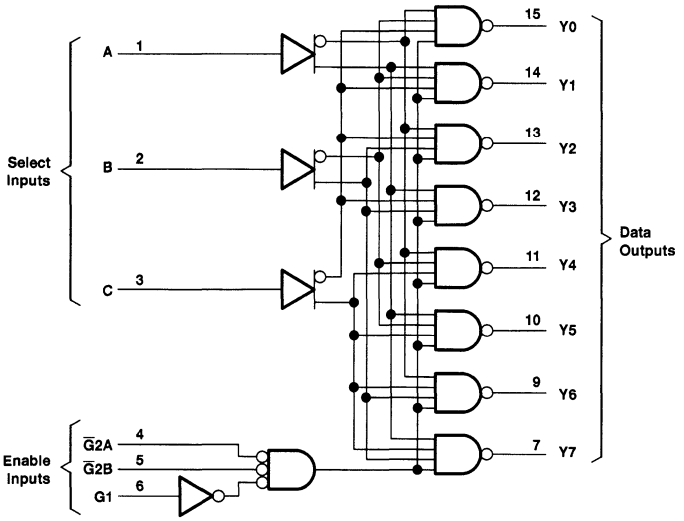
logic symbols (alternatives)†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.3 W
DB package ..... 0.55 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

		SN54AHCT138		SN74AHCT138		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT138		SN74AHCT138		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		3.15		V
	I_{OH} = –8 mA		2.5			2.4		2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		40		40	μA
ΔI_{CC}†	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
I_{off}	V_O = 5.5 V	0 V			0.5*				5	μA
C_i	$V_I = V_{CC}$ or GND	5 V		4	10				10	pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHCT138					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A, B, C	Any Y	C_L = 15 pF		7.6	10.4	1	12	ns
t_{PHL}*					7.6	10.4	1	12	
t_{PLH}*	G1	Any Y	C_L = 15 pF		6.6	9.1	1	10.5	ns
t_{PHL}*					6.6	9.1	1	10.5	
t_{PLH}*	$\overline{G}$2A, $\overline{G}$2B	Any Y	C_L = 15 pF		7	9.6	1	11	ns
t_{PHL}*					7	9.6	1	11	
t_{PLH}	A, B, C	Any Y	C_L = 50 pF		8.1	11.4	1	13	ns
t_{PHL}					8.1	11.4	1	13	
t_{PLH}	G1	Any Y	C_L = 50 pF		7.1	10.1	1	11.5	ns
t_{PHL}					7.1	10.1	1	11.5	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Any Y	C_L = 50 pF		7.5	10.6	1	12	ns
t_{PHL}					7.5	10.6	1	12	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

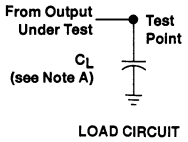
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHCT138					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A, B, C	Any Y	C_L = 15 pF		7.6	10.4	1	12	ns
t_{PHL}					7.6	10.4	1	12	
t_{PLH}	G1	Any Y	C_L = 15 pF		6.6	9.1	1	10.5	ns
t_{PHL}					6.6	9.1	1	10.5	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Any Y	C_L = 15 pF		7	9.6	1	11	ns
t_{PHL}					7	9.6	1	11	
t_{PLH}	A, B, C	Any Y	C_L = 50 pF		8.1	11.4	1	13	ns
t_{PHL}					8.1	11.4	1	13	
t_{PLH}	G1	Any Y	C_L = 50 pF		7.1	10.1	1	11.5	ns
t_{PHL}					7.1	10.1	1	11.5	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Any Y	C_L = 50 pF		7.5	10.6	1	12	ns
t_{PHL}					7.5	10.6	1	12	

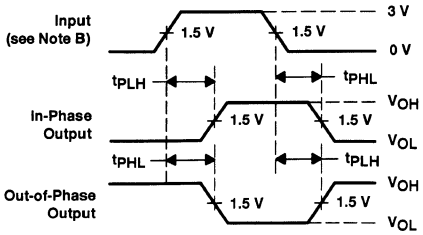
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load,	f = 1 MHz	49	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

APPLICATION INFORMATION

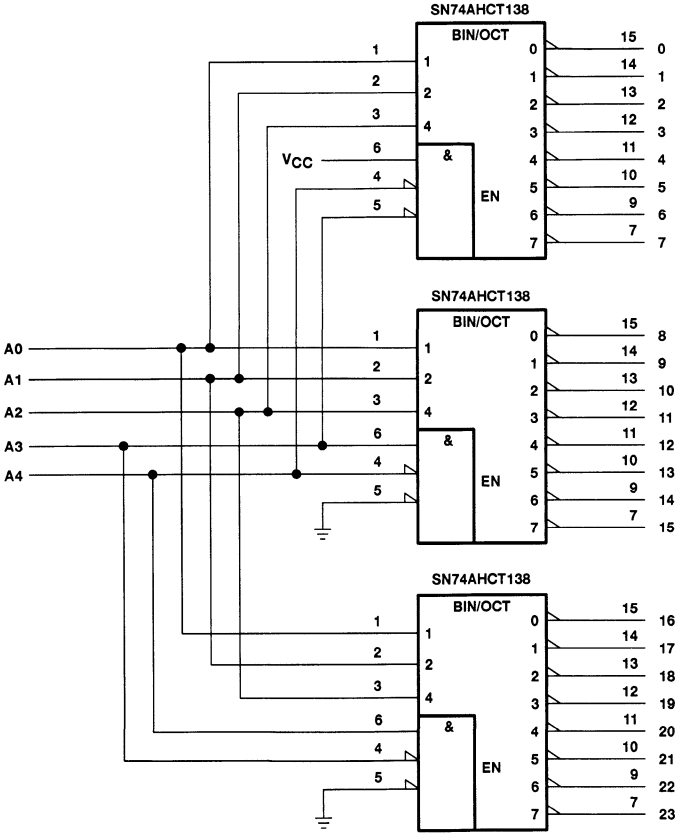


Figure 2. 24-Bit Decoding Scheme

APPLICATION INFORMATION

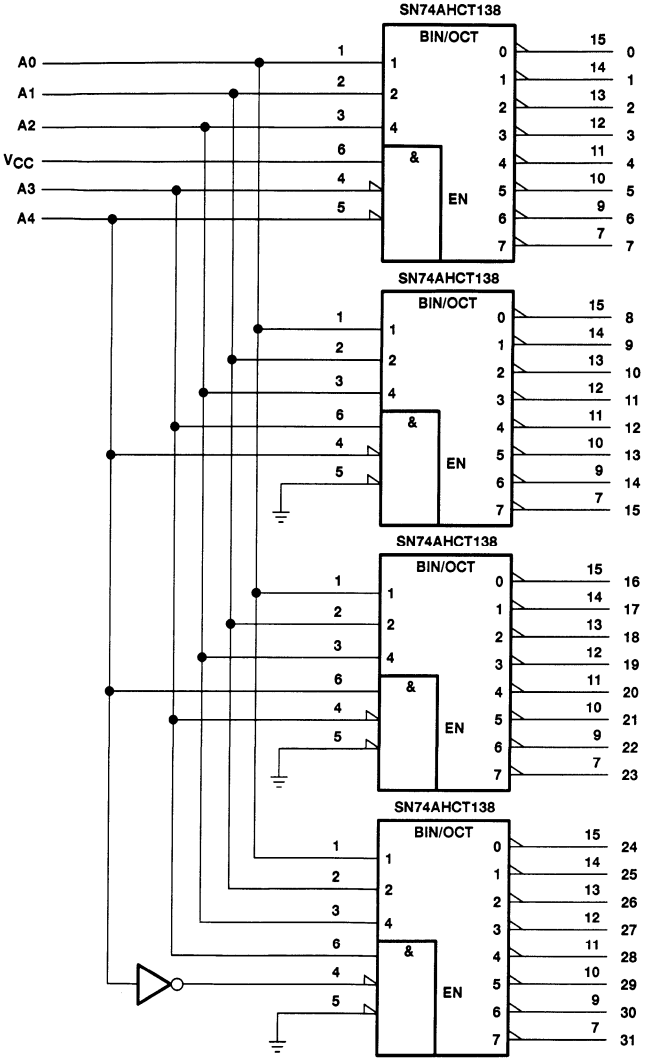
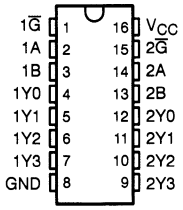


Figure 3. 32-Bit Decoding Scheme

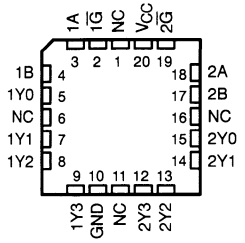
SCLS259C – DECEMBER 1995 – REVISED JUNE 1996

- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporate Two Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHC139 . . . J OR W PACKAGE
SN74AHC139 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC139 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AHC139 are dual 2-line to 4-line decoders/demultiplexers designed for 2-V to 5.5-V V_{CC} operation. These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

The active-low enable ($\overline{G}$) input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

The SN54AHC139 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC139 is characterized for operation from –40°C to 85°C.

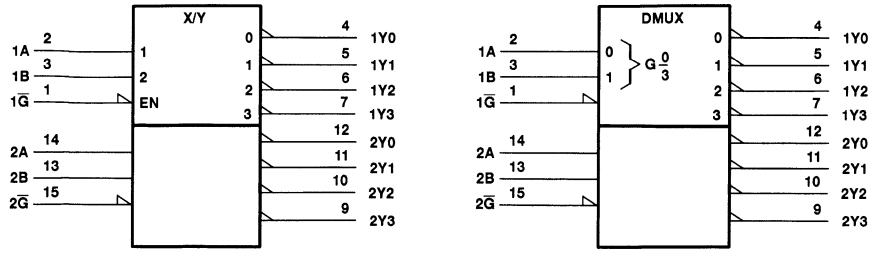
FUNCTION TABLE

INPUTS			OUTPUTS			
$\overline{G}$	SELECT					
	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

PRODUCT PREVIEW

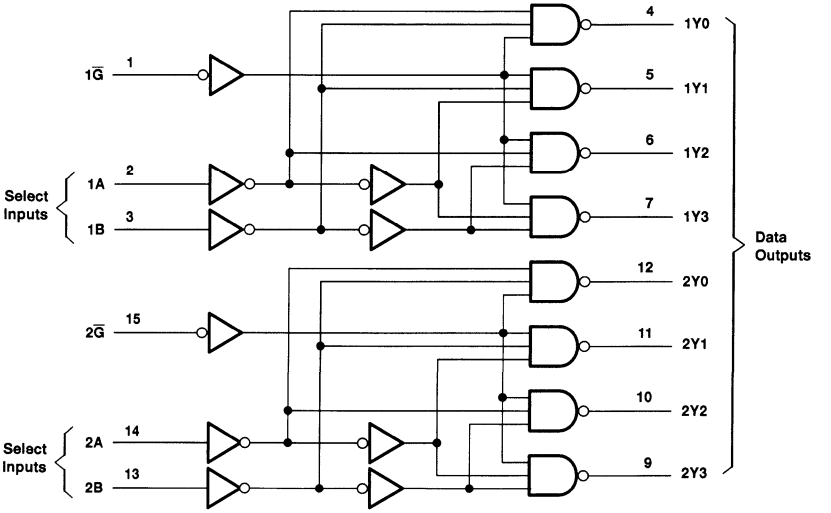
EPIC is a trademark of Texas Instruments Incorporated.

logic symbols (alternatives)†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... –20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.3 W
DB package ..... 0.55 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			SN54AHC139		SN74AHC139		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC139		SN74AHC139		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
	I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		40		40	μA
C_i	$V_I = V_{CC}$ or GND	5 V		4	10				10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHC139					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A or B	Y	C_L = 15 pF		7.2	11	1	13	ns
t_{PHL}*					7.2	11	1	13	
t_{PLH}*	$\overline{G}$	Y	C_L = 15 pF		6.4	9.2	1	11	ns
t_{PHL}*					6.4	9.2	1	11	
t_{PLH}	A or B	Y	C_L = 50 pF		9.7	14.5	1	16.5	ns
t_{PHL}					9.7	14.5	1	16.5	
t_{PLH}	$\overline{G}$	Y	C_L = 50 pF		8.9	12.7	1	14.5	ns
t_{PHL}					8.9	12.7	1	14.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHC139					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		7.2	11	1	13	ns
t_{PHL}					7.2	11	1	13	
t_{PLH}	$\overline{G}$	Y	C_L = 15 pF		6.4	9.2	1	11	ns
t_{PHL}					6.4	9.2	1	11	
t_{PLH}	A or B	Y	C_L = 50 pF		9.7	14.5	1	16.5	ns
t_{PHL}					9.7	14.5	1	16.5	
t_{PLH}	$\overline{G}$	Y	C_L = 50 pF		8.9	12.7	1	14.5	ns
t_{PHL}					8.9	12.7	1	14.5	

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHC139					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A or B	Y	C_L = 15 pF		5	7.2	1	8.5	ns
t_{PHL}*					5	7.2	1	8.5	
t_{PLH}*	$\overline{G}$	Y	C_L = 15 pF		4.4	6.3	1	7.5	ns
t_{PHL}*					4.4	6.3	1	7.5	
t_{PLH}	A or B	Y	C_L = 50 pF		6.5	9.2	1	10.5	ns
t_{PHL}					6.5	9.2	1	10.5	
t_{PLH}	$\overline{G}$	Y	C_L = 50 pF		5.9	8.3	1	9.5	ns
t_{PHL}					5.9	8.3	1	9.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

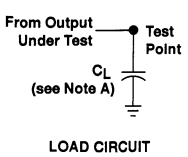
PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHC139					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		5	7.2	1	8.5	ns
t_{PHL}					5	7.2	1	8.5	
t_{PLH}	$\overline{G}$	Y	C_L = 15 pF		4.4	6.3	1	7.5	ns
t_{PHL}					4.4	6.3	1	7.5	
t_{PLH}	A or B	Y	C_L = 50 pF		6.5	9.2	1	10.5	ns
t_{PHL}					6.5	9.2	1	10.5	
t_{PLH}	$\overline{G}$	Y	C_L = 50 pF		5.9	8.3	1	9.5	ns
t_{PHL}					5.9	8.3	1	9.5	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

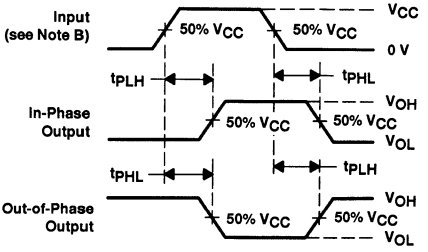
PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load,	f = 1 MHz	26	pF

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

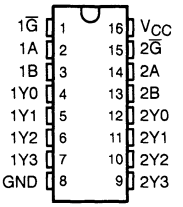
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

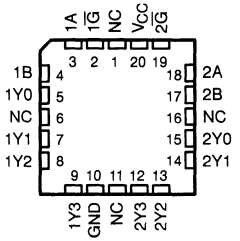
SCLS267B – DECEMBER 1995 – REVISED JUNE 1996

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporate Two Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHCT139 . . . J OR W PACKAGE
SN74AHCT139 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT139 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AHCT139 are dual 2-line to 4-line decoders/demultiplexers designed for 4.5-V to 5.5-V V_{CC} operation. These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

The active-low enable ($\overline{G}$) input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

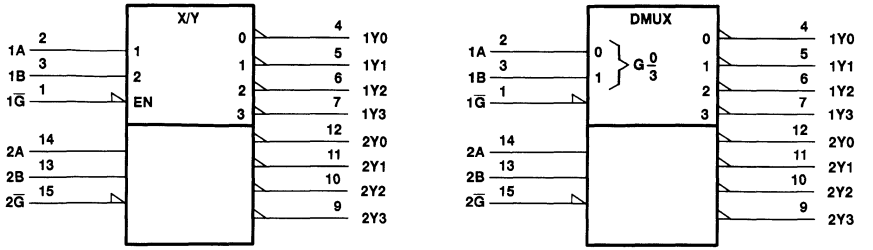
The SN54AHCT139 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT139 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUTS			
$\overline{G}$	SELECT					
	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

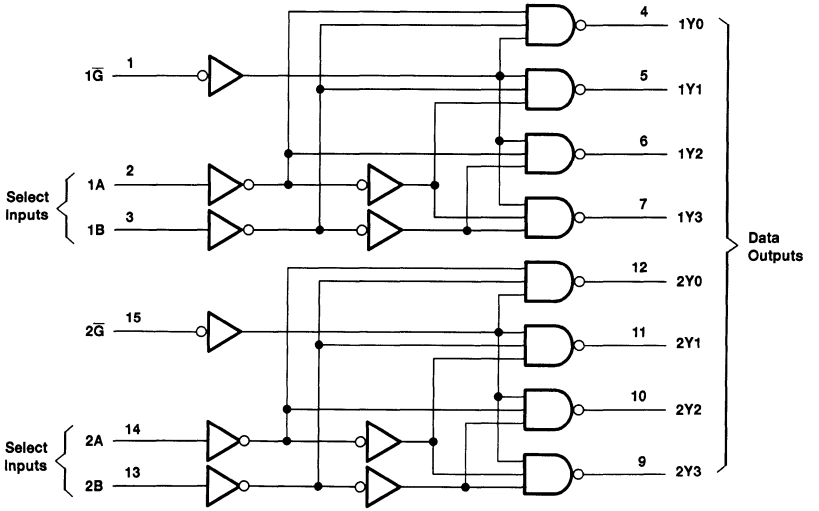
EPIC is a trademark of Texas Instruments Incorporated.

logic symbols (alternatives)†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
DB package ..... 0.55 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHCT139		SN74AHCT139		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25°C$			SN54AHCT139		SN74AHCT139		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = –50\ \mu A$	4.5 V	3.15	3.65		3.15		3.15		V
	$I_{OH} = –8$ mA		2.5			2.4		2.4		
V_{OL}	$I_{OL} = 50\ \mu A$	4.5 V			0.1		0.1		0.1	V
	$I_{OL} = 8$ mA				0.36		0.44		0.44	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	µA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		20		20	µA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4.5						pF

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT139					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A or B	Y	C_L = 15 pF				1		ns
t_{PHL}*							1		
t_{PLH}*	$\overline{G}$	Y	C_L = 15 pF				1		ns
t_{PHL}*							1		
t_{PLH}	A or B	Y	C_L = 50 pF				1		ns
t_{PHL}							1		
t_{PLH}	$\overline{G}$	Y	C_L = 50 pF				1		ns
t_{PHL}							1		

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

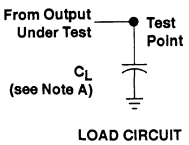
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT139					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF				1		ns
t_{PHL}							1		
t_{PLH}	$\overline{G}$	Y	C_L = 15 pF				1		ns
t_{PHL}							1		
t_{PLH}	A or B	Y	C_L = 50 pF				1		ns
t_{PHL}							1		
t_{PLH}	$\overline{G}$	Y	C_L = 50 pF				1		ns
t_{PHL}							1		

PRODUCT PREVIEW

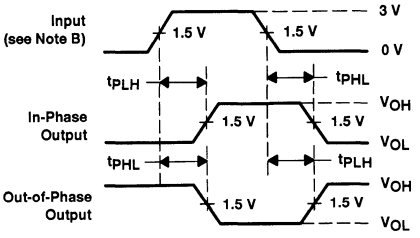
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	26	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCLS345 – MAY 1996

- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

These quadruple 2-line to 1-line data selectors/multiplexers are designed for 2-V to 5.5-V V_{CC} operation.

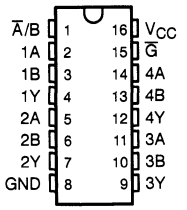
The 'AHC157 feature a common strobe ($\overline{G}$) input. When the strobe is high, all outputs are low. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The devices provide true data.

The SN54AHC157 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC157 is characterized for operation from –40°C to 85°C.

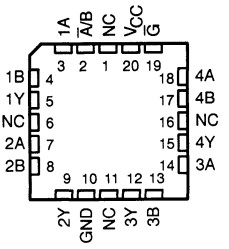
FUNCTION TABLE

INPUTS				OUTPUT
$\overline{G}$	$\overline{A}$/B	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

SN54AHC157 . . . J OR W PACKAGE
SN74AHC157 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC157 . . . FK PACKAGE
(TOP VIEW)

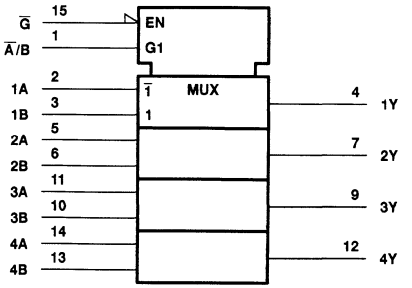


NC – No internal connection

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

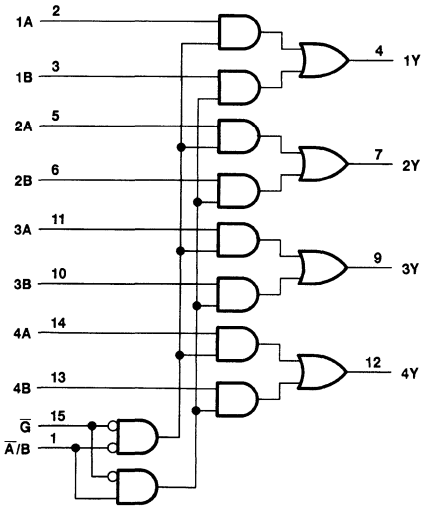
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... −20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.3 W
DB package ..... 0.55 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			SN54AHC157		SN74AHC157		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		−50		−50	μA
		V_{CC} = 3.3 V ± 0.3 V		−4		−4	mA
		V_{CC} = 5 V ± 0.5 V		−8		−8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC157		SN74AHC157		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
			3 V	2.9	3		2.9		2.9		
			4.5 V	4.4	4.5		4.4		4.4		
		I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
		I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
			3 V			0.1		0.1		0.1	
			4.5 V			0.1		0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	A or B inputs	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		40		40	μA
C_i		$V_I = V_{CC}$ or GND	5 V		4	10				10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC157					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A or B	Y	C_L = 15 pF		6.2	9.7	1	11.5	ns
t_{PHL}*					6.2	9.7	1	11.5	
t_{PLH}*	$\overline{A}$/B	Y	C_L = 15 pF		8.4	13.2	1	15.5	ns
t_{PHL}*					8.4	13.2	1	15.5	
t_{PLH}*	$\overline{G}$	Y	C_L = 15 pF		8.7	13.6	1	16	ns
t_{PHL}*					8.7	13.6	1	16	
t_{PLH}	A or B	Y	C_L = 50 pF		8.7	13.2	1	15	ns
t_{PHL}					8.7	13.2	1	15	
t_{PLH}	$\overline{A}$/B	Y	C_L = 50 pF		10.9	16.7	1	19	ns
t_{PHL}					10.9	16.7	1	19	
t_{PLH}	$\overline{G}$	Y	C_L = 50 pF		11.2	17.1	1	19.5	ns
t_{PHL}					11.2	17.1	1	19.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC157					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		6.2	9.7	1	11.5	ns
t_{PHL}					6.2	9.7	1	11.5	
t_{PLH}	$\overline{A}$/B	Y	C_L = 15 pF		8.4	13.2	1	15.5	ns
t_{PHL}					8.4	13.2	1	15.5	
t_{PLH}	$\overline{G}$	Y	C_L = 15 pF		8.7	13.6	1	16	ns
t_{PHL}					8.7	13.6	1	16	
t_{PLH}	A or B	Y	C_L = 50 pF		8.7	13.2	1	15	ns
t_{PHL}					8.7	13.2	1	15	
t_{PLH}	$\overline{A}$/B	Y	C_L = 50 pF		10.9	16.7	1	19	ns
t_{PLH}					10.9	16.7	1	19	
t_{PLH}	$\overline{G}$	Y	C_L = 50 pF		11.2	17.1	1	19.5	ns
t_{PHL}					11.2	17.1	1	19.5	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC157					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A or B	Y	C_L = 15 pF		4.1	6.4	1	7.5	ns
t_{PHL}*					4.1	6.4	1	7.5	
t_{PLH}*	$\overline{A}$/B	Y	C_L = 15 pF		5.3	8.1	1	9.5	ns
t_{PHL}*					5.3	8.1	1	9.5	
t_{PLH}*	$\overline{G}$	Y	C_L = 15 pF		5.6	8.6	1	10	ns
t_{PHL}*					5.6	8.6	1	10	
t_{PLH}	A or B	Y	C_L = 50 pF		5.6	8.4	1	9.5	ns
t_{PHL}					5.6	8.4	1	9.5	
t_{PLH}	$\overline{A}$/B	Y	C_L = 50 pF		6.8	10.1	1	11.5	ns
t_{PLH}					6.8	10.1	1	11.5	
t_{PLH}	$\overline{G}$	Y	C_L = 50 pF		7.1	10.6	1	12	ns
t_{PHL}					7.1	10.6	1	12	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC157					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		4.1	6.4	1	7.5	ns
t_{PHL}					4.1	6.4	1	7.5	
t_{PLH}	$\overline{A}$/B	Y	C_L = 15 pF		5.3	8.1	1	9.5	ns
t_{PHL}					5.3	8.1	1	9.5	
t_{PLH}	$\overline{G}$	Y	C_L = 15 pF		5.6	8.6	1	10	ns
t_{PHL}					5.6	8.6	1	10	
t_{PLH}	A or B	Y	C_L = 50 pF		5.6	8.4	1	9.5	ns
t_{PHL}					5.6	8.4	1	9.5	
t_{PLH}	$\overline{A}$/B	Y	C_L = 50 pF		6.8	10.1	1	11.5	ns
t_{PLH}					6.8	10.1	1	11.5	
t_{PLH}	$\overline{G}$	Y	C_L = 50 pF		7.1	10.6	1	12	ns
t_{PHL}					7.1	10.6	1	12	

noise characteristics V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

PARAMETER		SN74AHC157		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	–0.8		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}			V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

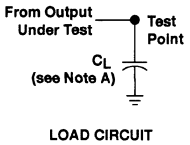
NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

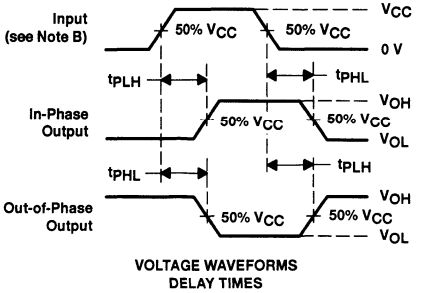
PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load,	f = 1 MHz	20	pF

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

SCLS347 – MAY 1996

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

These quadruple 2-line to 1-line data selectors/multiplexers are designed for 4.5-V to 5.5-V V_{CC} operation.

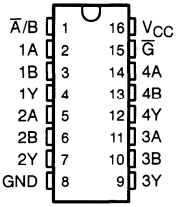
The 'AHCT157 feature a common strobe ($\overline{G}$) input. When the strobe is high, all outputs are low. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The devices provide true data.

The SN54AHCT157 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT157 is characterized for operation from –40°C to 85°C.

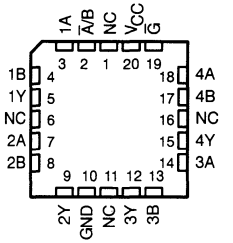
FUNCTION TABLE

INPUTS				OUTPUT
$\overline{G}$	$\overline{A}$/B	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

SN54AHCT157 . . . J OR W PACKAGE
SN74AHCT157 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT157 . . . FK PACKAGE
(TOP VIEW)

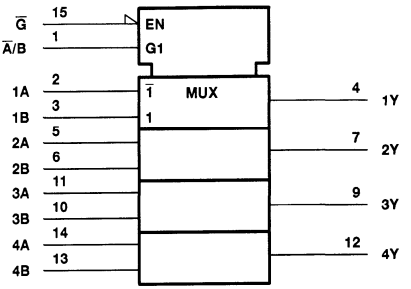


NC – No internal connection

PRODUCT PREVIEW

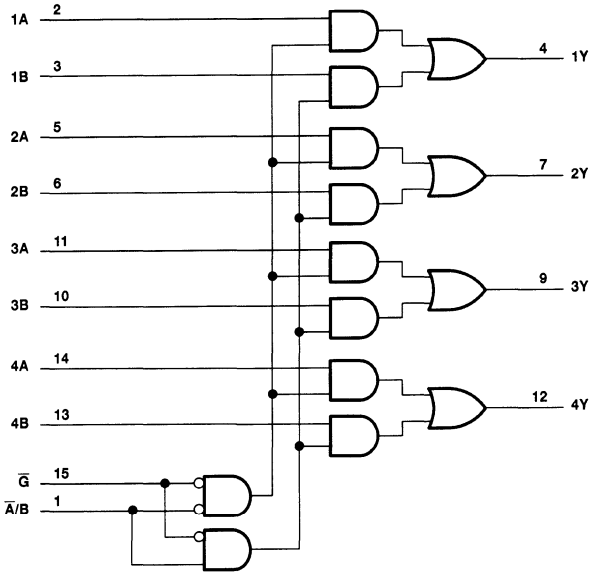
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.3 W
DB package ..... 0.55 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHCT157		SN74AHCT157		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall time		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT157		SN74AHCT157		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		3.15		V
	I_{OH} = –8 mA		2.5			2.4		2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20		20	μA
ΔI_{CC}†	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
C_i	V_I = V_{CC} or GND	5 V		4.5						pF

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT157					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A or B	Y	C_L = 15 pF		4.1	6.4	1	7.5	ns
t_{PHL}*					4.1	6.4	1	7.5	
t_{PLH}*	$\overline{A}$/B	Y	C_L = 15 pF		5.3	8.1	1	9.5	ns
t_{PHL}*					5.3	8.1	1	9.5	
t_{PLH}*	$\overline{G}$	Y	C_L = 15 pF		5.6	8.6	1	10	ns
t_{PHL}*					5.6	8.6	1	10	
t_{PLH}	A or B	Y	C_L = 50 pF		5.6	8.4	1	9.5	ns
t_{PHL}					5.6	8.4	1	9.5	
t_{PLH}	$\overline{A}$/B	Y	C_L = 50 pF		6.8	10.1	1	11.5	ns
t_{PLH}					6.8	10.1	1	11.5	
t_{PLH}	$\overline{G}$	Y	C_L = 50 pF		7.1	10.6	1	12	ns
t_{PHL}					7.1	10.6	1	12	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT157					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		4.1	6.4	1	7.5	ns
t_{PHL}					4.1	6.4	1	7.5	
t_{PLH}	$\overline{A}$/B	Y	C_L = 15 pF		5.3	8.1	1	9.5	ns
t_{PHL}					5.3	8.1	1	9.5	
t_{PLH}	$\overline{G}$	Y	C_L = 15 pF		5.6	8.6	1	10	ns
t_{PHL}					5.6	8.6	1	10	
t_{PLH}	A or B	Y	C_L = 50 pF		5.6	8.4	1	9.5	ns
t_{PHL}					5.6	8.4	1	9.5	
t_{PLH}	$\overline{A}$/B	Y	C_L = 50 pF		6.8	10.1	1	11.5	ns
t_{PLH}					6.8	10.1	1	11.5	
t_{PLH}	$\overline{G}$	Y	C_L = 50 pF		7.1	10.6	1	12	ns
t_{PHL}					7.1	10.6	1	12	

noise characteristics V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

PARAMETER		SN74AHCT157		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	–0.8		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}			V
$V_{IH(D)}$	High-level dynamic input voltage	2		V
$V_{IL(D)}$	Low-level dynamic input voltage		0.8	V

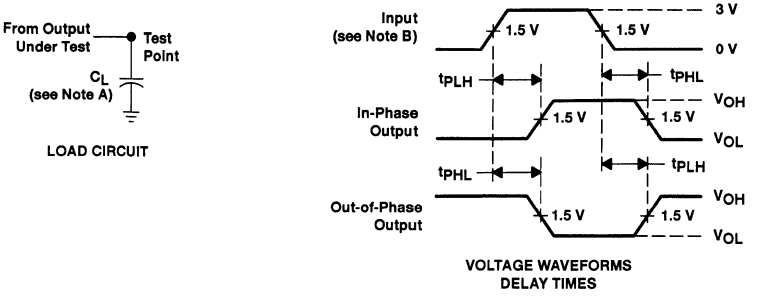
NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load,	f = 1 MHz	26	pF

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

SCLS346 – MAY 1996

- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

These quadruple 2-line to 1-line data selectors/multiplexers are designed for 2-V to 5.5-V V_{CC} operation.

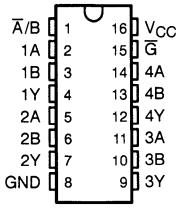
The 'AHC158 feature a common strobe ($\overline{G}$) input. When the strobe is high, all outputs are high. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. These devices provide inverted data.

The SN54AHC158 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC158 is characterized for operation from –40°C to 85°C.

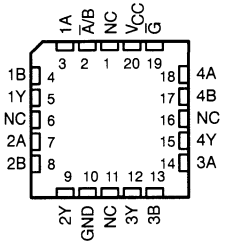
FUNCTION TABLE

INPUTS				OUTPUT
$\overline{G}$	$\overline{A}$/B	A	B	Y
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

SN54AHC158 . . . J OR W PACKAGE
SN74AHC158 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC158 . . . FK PACKAGE
(TOP VIEW)

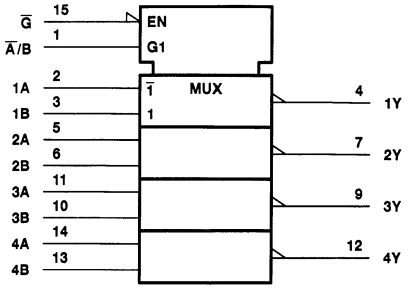


NC – No internal connection

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

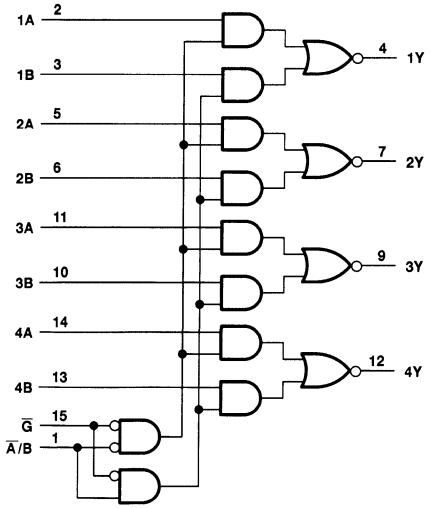
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... −20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.3 W
DB package ..... 0.55 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			SN54AHC158		SN74AHC158		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		−50		−50	μA
		V_{CC} = 3.3 V ± 0.3 V		−4		−4	mA
		V_{CC} = 5 V ± 0.5 V		−8		−8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54AHC158		SN74AHC158		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 μA		2 V	1.9	2		1.9		1.9		V
				3 V	2.9	3		2.9		2.9		
				4.5 V	4.4	4.5		4.4		4.4		
		I_{OH} = –4 mA		3 V	2.58			2.48		2.48		
		I_{OH} = –8 mA		4.5 V	3.94			3.8		3.8		
V_{OL}		I_{OL} = 50 μA		2 V			0.1		0.1		0.1	V
				3 V			0.1		0.1		0.1	
				4.5 V			0.1		0.1		0.1	
		I_{OL} = 4 mA		3 V			0.36		0.5		0.44	
		I_{OL} = 8 mA		4.5 V			0.36		0.5		0.44	
I_I	A or B inputs	$V_I = V_{CC}$ or GND		5.5 V			± 0.1		± 1		± 1	μA
I_{CC}		$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V			4		40		40	μA
C_i		$V_I = V_{CC}$ or GND		5 V		4	10				10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC158					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A or B	Y	C_L = 15 pF		6.2	9.7	1	11.5	ns
t_{PHL}*					6.2	9.7	1	11.5	
t_{PLH}*	$\overline{A}$/B	Y	C_L = 15 pF		8.4	13.2	1	15.5	ns
t_{PHL}*					8.4	13.2	1	15.5	
t_{PLH}*	$\overline{G}$	Y	C_L = 15 pF		8.7	13.6	1	16	ns
t_{PHL}*					8.7	13.6	1	16	
t_{PLH}	A or B	Y	C_L = 50 pF		8.7	13.2	1	15	ns
t_{PHL}					8.7	13.2	1	15	
t_{PLH}	$\overline{A}$/B	Y	C_L = 50 pF		10.9	16.7	1	19	ns
t_{PHL}					10.9	16.7	1	19	
t_{PLH}	$\overline{G}$	Y	C_L = 50 pF		11.2	17.1	1	19.5	ns
t_{PHL}					11.2	17.1	1	19.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC158					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		6.2	9.7	1	11.5	ns
t_{PHL}					6.2	9.7	1	11.5	
t_{PLH}	$\overline{A}$/B	Y	C_L = 15 pF		8.4	13.2	1	15.5	ns
t_{PHL}					8.4	13.2	1	15.5	
t_{PLH}	$\overline{G}$	Y	C_L = 15 pF		8.7	13.6	1	16	ns
t_{PHL}					8.7	13.6	1	16	
t_{PLH}	A or B	Y	C_L = 50 pF		8.7	13.2	1	15	ns
t_{PHL}					8.7	13.2	1	15	
t_{PLH}	$\overline{A}$/B	Y	C_L = 50 pF		10.9	16.7	1	19	ns
t_{PLH}					10.9	16.7	1	19	
t_{PLH}	$\overline{G}$	Y	C_L = 50 pF		11.2	17.1	1	19.5	ns
t_{PHL}					11.2	17.1	1	19.5	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC158					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A or B	Y	C_L = 15 pF		4.1	6.4	1	7.5	ns
t_{PHL}*					4.1	6.4	1	7.5	
t_{PLH}*	$\overline{A}$/B	Y	C_L = 15 pF		5.3	8.1	1	9.5	ns
t_{PHL}*					5.3	8.1	1	9.5	
t_{PLH}*	$\overline{G}$	Y	C_L = 15 pF		5.6	8.6	1	10	ns
t_{PHL}*					5.6	8.6	1	10	
t_{PLH}	A or B	Y	C_L = 50 pF		5.6	8.4	1	9.5	ns
t_{PHL}					5.6	8.4	1	9.5	
t_{PLH}	$\overline{A}$/B	Y	C_L = 50 pF		6.8	10.1	1	11.5	ns
t_{PLH}					6.8	10.1	1	11.5	
t_{PLH}	$\overline{G}$	Y	C_L = 50 pF		7.1	10.6	1	12	ns
t_{PHL}					7.1	10.6	1	12	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC158					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		4.1	6.4	1	7.5	ns
t_{PHL}					4.1	6.4	1	7.5	
t_{PLH}	$\overline{A}$/B	Y	C_L = 15 pF		5.3	8.1	1	9.5	ns
t_{PHL}					5.3	8.1	1	9.5	
t_{PLH}	$\overline{G}$	Y	C_L = 15 pF		5.6	8.6	1	10	ns
t_{PHL}					5.6	8.6	1	10	
t_{PLH}	A or B	Y	C_L = 50 pF		5.6	8.4	1	9.5	ns
t_{PHL}					5.6	8.4	1	9.5	
t_{PLH}	$\overline{A}$/B	Y	C_L = 50 pF		6.8	10.1	1	11.5	ns
t_{PLH}					6.8	10.1	1	11.5	
t_{PLH}	$\overline{G}$	Y	C_L = 50 pF		7.1	10.6	1	12	ns
t_{PHL}					7.1	10.6	1	12	

noise characteristics V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

PARAMETER		SN74AHC158			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	–0.8			V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

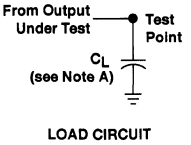
NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

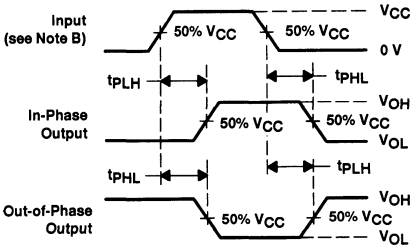
PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load,	f = 1 MHz	20	pF

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

SCLS348 – MAY 1996

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

These quadruple 2-line to 1-line data selectors/multiplexers are designed for 4.5-V to 5.5-V V_{CC} operation.

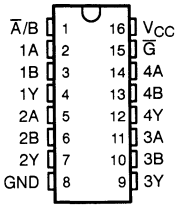
The 'AHCT158 feature a common strobe ($\overline{G}$) input. When the strobe is high, all outputs are high. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The devices provide inverted data.

The SN54AHCT158 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT158 is characterized for operation from –40°C to 85°C.

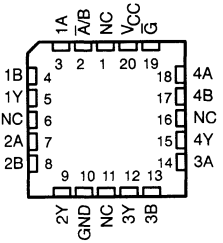
FUNCTION TABLE

INPUTS				OUTPUT
$\overline{G}$	$\overline{A}$/B	A	B	Y
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

SN54AHCT158 . . . J OR W PACKAGE
SN74AHCT158 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT158 . . . FK PACKAGE
(TOP VIEW)

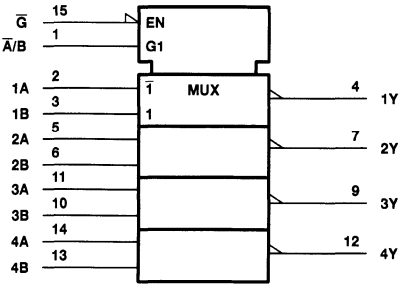


NC – No internal connection

PRODUCT PREVIEW

EPIC is a trademark of Texas Instruments Incorporated.

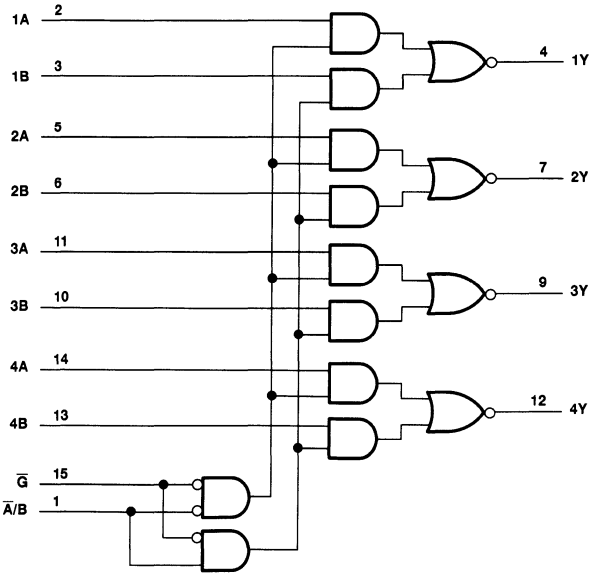
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
DB package ..... 0.55 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHCT158		SN74AHCT158		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall time		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT158		SN74AHCT158		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		3.15		V
	I_{OH} = –8 mA		2.5			2.4		2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20		20	μA
ΔI_{CC}†	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
C_i	V_I = V_{CC} or GND	5 V		4.5						pF

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT158					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A or B	Y	C_L = 15 pF		4.1	6.4	1	7.5	ns
t_{PHL}*					4.1	6.4	1	7.5	
t_{PLH}*	$\overline{A}$/B	Y	C_L = 15 pF		5.3	8.1	1	9.5	ns
t_{PHL}*					5.3	8.1	1	9.5	
t_{PLH}*	$\overline{G}$	Y	C_L = 15 pF		5.6	8.6	1	10	ns
t_{PHL}*					5.6	8.6	1	10	
t_{PLH}	A or B	Y	C_L = 50 pF		5.6	8.4	1	9.5	ns
t_{PHL}					5.6	8.4	1	9.5	
t_{PLH}	$\overline{A}$/B	Y	C_L = 50 pF		6.8	10.1	1	11.5	ns
t_{PLH}					6.8	10.1	1	11.5	
t_{PLH}	$\overline{G}$	Y	C_L = 50 pF		7.1	10.6	1	12	ns
t_{PHL}					7.1	10.6	1	12	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT158					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		4.1	6.4	1	7.5	ns
t_{PHL}					4.1	6.4	1	7.5	
t_{PLH}	$\overline{A}$/B	Y	C_L = 15 pF		5.3	8.1	1	9.5	ns
t_{PHL}					5.3	8.1	1	9.5	
t_{PLH}	$\overline{G}$	Y	C_L = 15 pF		5.6	8.6	1	10	ns
t_{PHL}					5.6	8.6	1	10	
t_{PLH}	A or B	Y	C_L = 50 pF		5.6	8.4	1	9.5	ns
t_{PHL}					5.6	8.4	1	9.5	
t_{PLH}	$\overline{A}$/B	Y	C_L = 50 pF		6.8	10.1	1	11.5	ns
t_{PLH}					6.8	10.1	1	11.5	
t_{PLH}	$\overline{G}$	Y	C_L = 50 pF		7.1	10.6	1	12	ns
t_{PHL}					7.1	10.6	1	12	

noise characteristics V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

PARAMETER		SN74AHCT158		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	–0.8		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}			V
$V_{IH(D)}$	High-level dynamic input voltage	2		V
$V_{IL(D)}$	Low-level dynamic input voltage		0.8	V

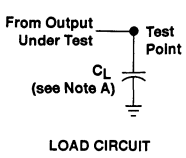
NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

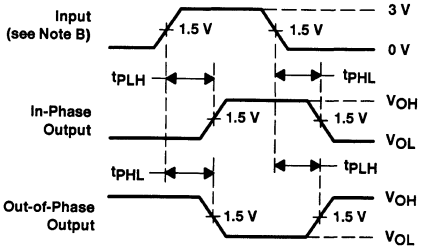
PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load,	f = 1 MHz	26	pF

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES

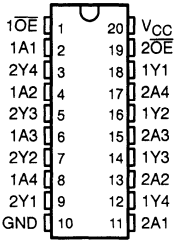
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

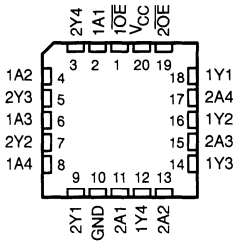
PRODUCT PREVIEW

- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHC240 . . . J OR W PACKAGE
SN74AHC240 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC240 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers/drivers are designed specifically to improve the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The 'AHC240 are organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

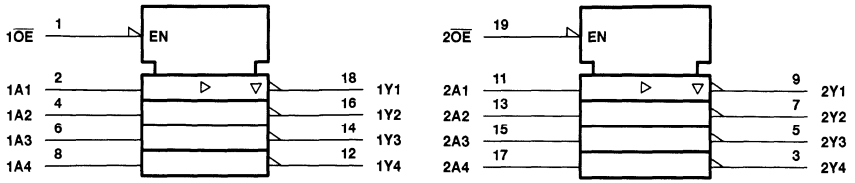
The SN54AHC240 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC240 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

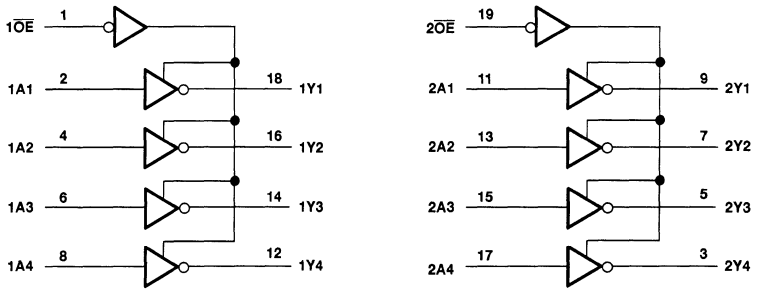
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			SN54AHC240		SN74AHC240		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC240		SN74AHC240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
			3 V	2.9	3		2.9		2.9		
			4.5 V	4.4	4.5		4.4		4.4		
		I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
		I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
			3 V			0.1		0.1		0.1	
			4.5 V			0.1		0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	Data inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
	Control inputs					±0.1		±1		±1	
I_{OZ}†		V_O = V_{CC} or GND, V_I ($\overline{OE}$) = V_{IL} or V_{IH}	5.5 V			±0.25		±2.5		±2.5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
C_i		V_I = V_{CC} or GND	5 V		2.5	10				10	pF
C_o		V_O = V_{CC} or GND	5 V		3.5						pF

† The parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHC240					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A	Y	C_L = 15 pF		5.3	7.5	1	9	ns
t_{PHL}*					5.3	7.5	1	9	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		6.6	10.6	1	12.5	ns
t_{PZL}*					6.6	10.6	1	12.5	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		7.8	11.5	1	12.5	ns
t_{PLZ}*					7.8	11.5	1	12.5	
t_{PLH}	A	Y	C_L = 50 pF		7.8	11	1	12.5	ns
t_{PHL}					7.8	11	1	12.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		9.1	14.1	1	16	ns
t_{PZL}					9.1	14.1	1	16	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		10.3	14	1	16	ns
t_{PLZ}					10.3	14	1	16	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHC240					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		5.3	7.5	1	9	ns
t_{PHL}					5.3	7.5	1	9	
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF		6.6	10.6	1	12.5	ns
t_{PZL}					6.6	10.6	1	12.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF		7.8	11.5	1	12.5	ns
t_{PLZ}					7.8	11.5	1	12.5	
t_{PLH}	A	Y	C_L = 50 pF		7.8	11	1	12.5	ns
t_{PHL}					7.8	11	1	12.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		9.1	14.1	1	16	ns
t_{PZL}					9.1	14.1	1	16	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		10.3	14	1	16	ns
t_{PLZ}					10.3	14	1	16	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHC240					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A	Y	C_L = 15 pF		3.6	5.5	1	6.5	ns
t_{PHL}*					3.6	5.5	1	6.5	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		4.7	7.3	1	8.5	ns
t_{PZL}*					4.7	7.3	1	8.5	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		5.2	7.2	1	8.5	ns
t_{PLZ}*					5.2	7.2	1	8.5	
t_{PLH}	A	Y	C_L = 50 pF		5.1	7.5	1	8.5	ns
t_{PHL}					5.1	7.5	1	8.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		6.2	9.3	1	10.5	ns
t_{PZL}					6.2	9.3	1	10.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		6.7	9.2	1	10.5	ns
t_{PLZ}					6.7	9.2	1	10.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHC240					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		3.6	5.5	1	6.5	ns
t_{PHL}					3.6	5.5	1	6.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF		4.7	7.3	1	8.5	ns
t_{PZL}					4.7	7.3	1	8.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF		5.2	7.2	1	8.5	ns
t_{PLZ}					5.2	7.2	1	8.5	
t_{PLH}	A	Y	C_L = 50 pF		5.1	7.5	1	8.5	ns
t_{PHL}					5.1	7.5	1	8.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		6.2	9.3	1	10.5	ns
t_{PZL}					6.2	9.3	1	10.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		6.7	9.2	1	10.5	ns
t_{PLZ}					6.7	9.2	1	10.5	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHC240				UNIT
			T_A = 25°C		MIN	MAX	
			MIN	MAX			
$t_{sk(o)}$	Output skew	3.3 V ± 0.3 V		1.5		1.5	ns
		5 V ± 0.5 V		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

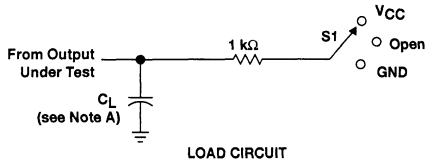
PARAMETER		SN74AHC240			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.6		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.6		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.6		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

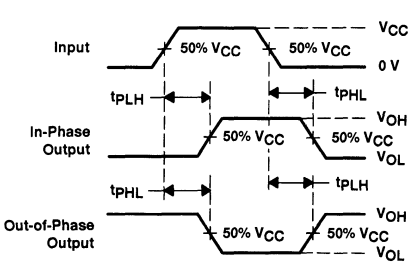
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	10	pF

PARAMETER MEASUREMENT INFORMATION

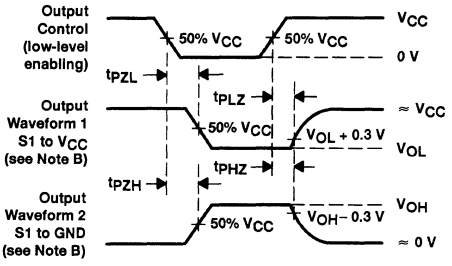


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
DELAY TIMES



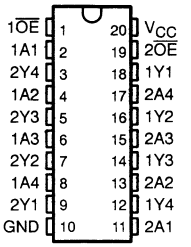
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

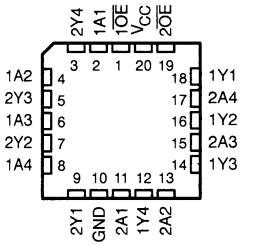
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs**

SN54AHCT240 . . . J OR W PACKAGE
SN74AHCT240 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT240 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers/drivers are designed specifically to improve the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The 'AHCT240 are organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

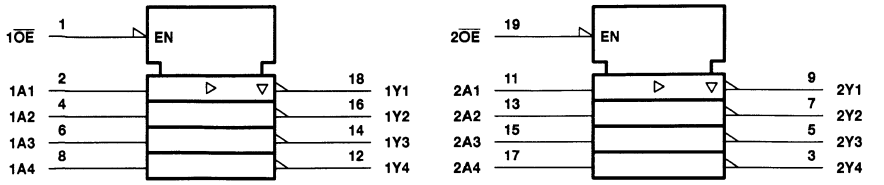
The SN54AHCT240 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT240 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer/driver)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

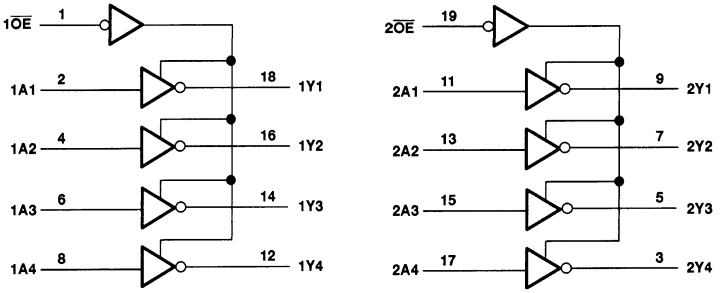
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHCT240		SN74AHCT240		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT240		SN74AHCT240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		3.15		V
	I_{OH} = –8 mA		2.5			2.4		2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V		.001	0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.25		±2.5		±2.5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		40		40	μA
ΔI_{CC}†	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
I_{off}	V_O = 5.5 V	0 V			0.5*				5	μA
C_i	$V_I = V_{CC}$ or GND	5 V		2.5	10				10	pF
C_o	$V_O = V_{CC}$ or GND	5 V		3						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT240					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A	Y	C_L = 15 pF		5.4	7.4	1	8.5	ns
t_{PHL}*					5.4	7.4	1	8.5	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		7.7	10.4	1	12	ns
t_{PZL}*					7.7	10.4	1	12	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		8.3	10.4	1	12	ns
t_{PLZ}*					8.3	10.4	1	12	
t_{PLH}	A	Y	C_L = 50 pF		5.9	8.4	1	9.5	ns
t_{PHL}					5.9	8.4	1	9.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		8.2	11.4	1	13	ns
t_{PZL}					8.2	11.4	1	13	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		8.8	11.4	1	13	ns
t_{PLZ}					8.8	11.4	1	13	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT240					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		5.4	7.4	1	8.5	ns
t_{PHL}					5.4	7.4	1	8.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF		7.7	10.4	1	12	ns
t_{PZL}					7.7	10.4	1	12	
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF		8.3	10.4	1	12	ns
t_{PLZ}					8.3	10.4	1	12	
t_{PLH}	A	Y	C_L = 50 pF		5.9	8.4	1	9.5	ns
t_{PHL}					5.9	8.4	1	9.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		8.2	11.4	1	13	ns
t_{PZL}					8.2	11.4	1	13	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		8.8	11.4	1	13	ns
t_{PLZ}					8.8	11.4	1	13	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHCT240				UNIT
			T_A = 25°C		MIN	MAX	
			MIN	MAX			
$t_{sk(o)}$	Output skew	5 V ± 0.5 V		1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

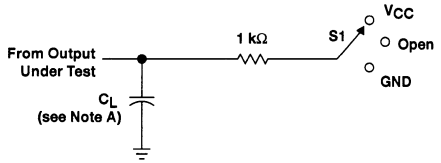
PARAMETER		SN74AHCT240			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.6		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.6		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.1		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

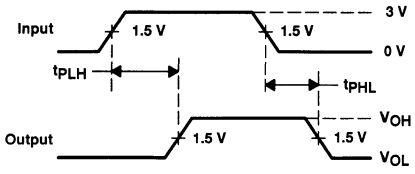
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	10	pF

PARAMETER MEASUREMENT INFORMATION

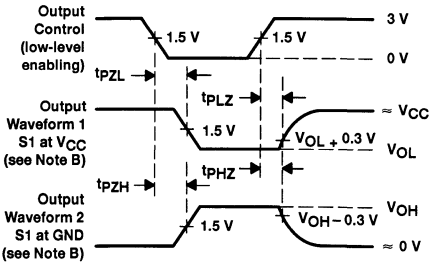


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
DELAY TIMES



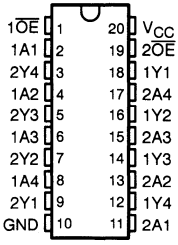
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

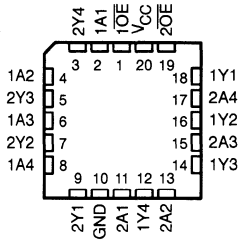
Figure 1. Load Circuit and Voltage Waveforms

- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHC244 . . . J OR W PACKAGE
SN74AHC244 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC244 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers/drivers are designed specifically to improve the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The 'AHC244 are organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

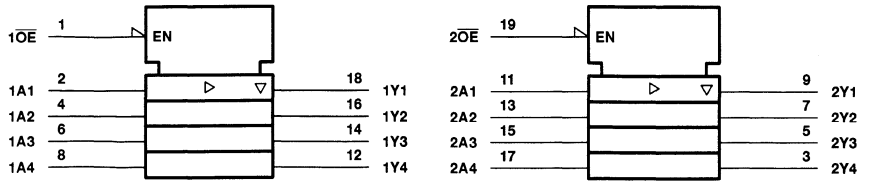
The SN54AHC244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC244 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

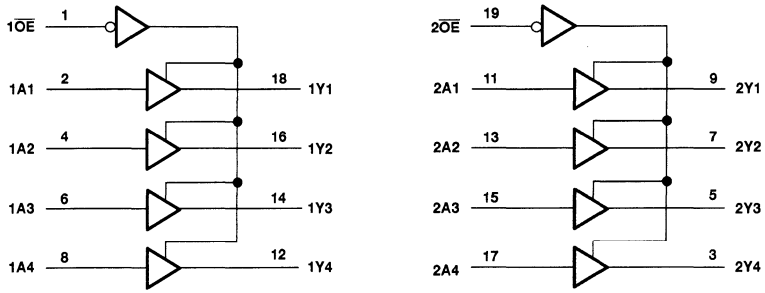
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			SN54AHC244		SN74AHC244		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC244		SN74AHC244		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
			3 V	2.9	3		2.9		2.9		
			4.5 V	4.4	4.5		4.4		4.4		
		I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
		I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
			3 V			0.1		0.1		0.1	
			4.5 V			0.1		0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	Data inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
	Control inputs					±0.1		±1		±1	
I_{OZ}		V_O = V_{CC} or GND, V_I ($\overline{OE}$) = V_{IL} or V_{IH}	5.5 V			±0.25		±2.5		±2.5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
C_i		V_I = V_{CC} or GND	5 V		2	10				10	pF
C_o		V_O = V_{CC} or GND	5 V		3.5						pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHC244					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A	Y	C_L = 15 pF		5.8	8.4	1	10	ns
t_{PHL}*					5.8	8.4	1	10	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		6.6	10.6	1	12.5	ns
t_{PZL}*					6.6	10.6	1	12.5	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		5	9.7	1	11	ns
t_{PLZ}*					5	9.7	1	11	
t_{PLH}	A	Y	C_L = 50 pF		8.3	11.9	1	13.5	ns
t_{PHL}					8.3	11.9	1	13.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		9.1	14.1	1	16	ns
t_{PZL}					9.1	14.1	1	16	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		10.3	14	1	16	ns
t_{PLZ}					10.3	14	1	16	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHC244					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		5.8	8.4	1	10	ns
t_{PHL}					5.8	8.4	1	10	
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF		6.6	10.6	1	12.5	ns
t_{PZL}					6.6	10.6	1	12.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF		5	9.7	1	11	ns
t_{PLZ}					5	9.7	1	11	
t_{PLH}	A	Y	C_L = 50 pF		8.3	11.9	1	13.5	ns
t_{PHL}					8.3	11.9	1	13.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		9.1	14.1	1	16	ns
t_{PZL}					9.1	14.1	1	16	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		10.3	14	1	16	ns
t_{PLZ}					10.3	14	1	16	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHC244					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A	Y	C_L = 15 pF		3.9	5.5	1	6.5	ns
t_{PHL}*					3.9	5.5	1	6.5	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		4.7	7.3	1	8.5	ns
t_{PZL}*					4.7	7.3	1	8.5	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		5	7.2	1	8.5	ns
t_{PLZ}*					5	7.2	1	8.5	
t_{PLH}	A	Y	C_L = 50 pF		5.4	7.5	1	8.5	ns
t_{PHL}					5.4	7.5	1	8.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		6.2	9.3	1	10.5	ns
t_{PZL}					6.2	9.3	1	10.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		6.7	9.2	1	10.5	ns
t_{PLZ}					6.7	9.2	1	10.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHC244					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		3.9	5.5	1	6.5	ns
t_{PHL}					3.9	5.5	1	6.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF		4.7	7.3	1	8.5	ns
t_{PZL}					4.7	7.3	1	8.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF		5	7.2	1	8.5	ns
t_{PLZ}					5	7.2	1	8.5	
t_{PLH}	A	Y	C_L = 50 pF		5.4	7.5	1	8.5	ns
t_{PHL}					5.4	7.5	1	8.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		6.2	9.3	1	10.5	ns
t_{PZL}					6.2	9.3	1	10.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		6.7	9.2	1	10.5	ns
t_{PLZ}					6.7	9.2	1	10.5	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHC244				UNIT
			T_A = 25°C		MIN	MAX	
			MIN	MAX			
$t_{sk(o)}$	Output skew	3.3 V ± 0.3 V		1.5		1.5	ns
		5 V ± 0.5 V		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

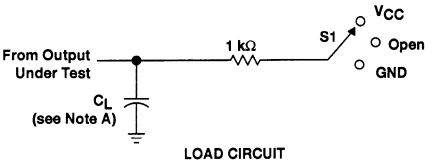
PARAMETER		SN74AHC244			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.2		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.8		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for plastic surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

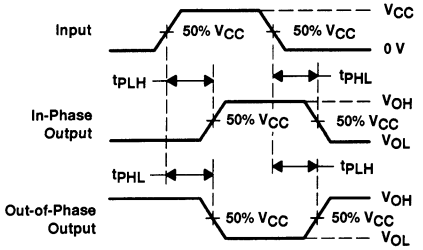
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	8.6	pF

PARAMETER MEASUREMENT INFORMATION

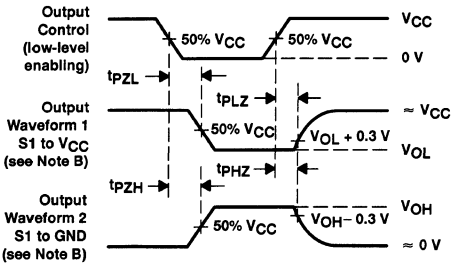


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
DELAY TIMES



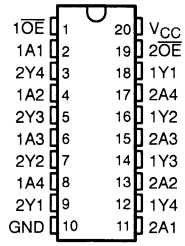
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

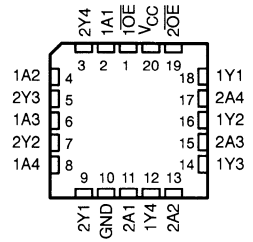
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHCT244 . . . J OR W PACKAGE
SN74AHCT244 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT244 . . . FK PACKAGE
(TOP VIEW)



description

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The 'AHCT244 are organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The SN54AHCT244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT244 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer/driver)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

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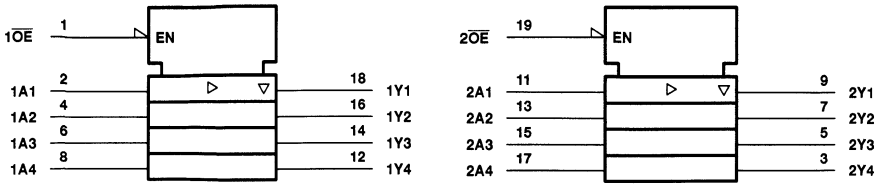
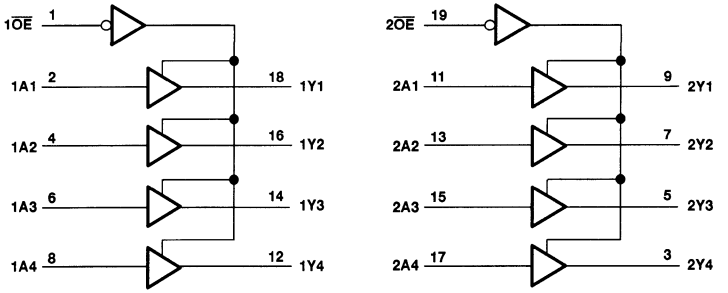
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHCT244		SN74AHCT244		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT244		SN74AHCT244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		3.15		V
	I_{OH} = –8 mA		2.5			2.4		2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.25		±2.5		±2.5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		40		40	μA
ΔI_{CC}†	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
I_{off}	V_O = 5.5 V	0 V			0.5*				5	μA
C_i	$V_I = V_{CC}$ or GND	5 V		2.5	10				10	pF
C_o	$V_O = V_{CC}$ or GND	5 V		3						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT244					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A	Y	C_L = 15 pF		5.4	7.4	1	8.5	ns
t_{PHL}*					5.4	7.4	1	8.5	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		7.7	10.4	1	12	ns
t_{PZL}*					7.7	10.4	1	12	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		5	9.4	1	10	ns
t_{PLZ}*					5	9.4	1	10	
t_{PLH}	A	Y	C_L = 50 pF		5.9	8.4	1	9.5	ns
t_{PHL}					5.9	8.4	1	9.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		8.2	11.4	1	13	ns
t_{PZL}					8.2	11.4	1	13	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		8.8	11.4	1	13	ns
t_{PLZ}					8.8	11.4	1	13	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT244					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		5.4	7.4	1	8.5	ns
t_{PHL}					5.4	7.4	1	8.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF		7.7	10.4	1	12	ns
t_{PZL}					7.7	10.4	1	12	
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF		5	9.4	1	10	ns
t_{PLZ}					5	9.4	1	10	
t_{PLH}	A	Y	C_L = 50 pF		5.9	8.4	1	9.5	ns
t_{PHL}					5.9	8.4	1	9.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		8.2	11.4	1	13	ns
t_{PZL}					8.2	11.4	1	13	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		8.8	11.4	1	13	ns
t_{PLZ}					8.8	11.4	1	13	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHCT244				UNIT
			T_A = 25°C		MIN	MAX	
			MIN	MAX			
$t_{sk(o)}$	Output skew	5 V ± 0.5 V		1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

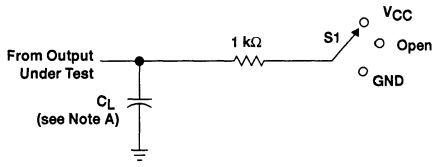
PARAMETER		SN74AHCT244			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.7		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.7		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.1		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

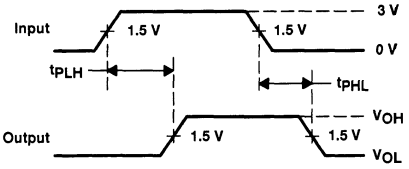
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	8.2	pF

PARAMETER MEASUREMENT INFORMATION

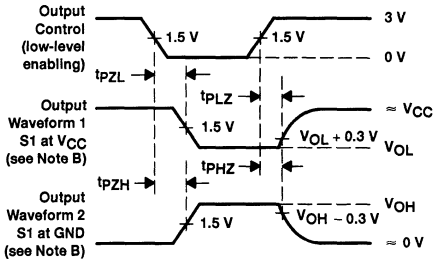


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
DELAY TIMES



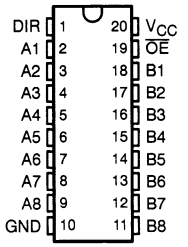
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

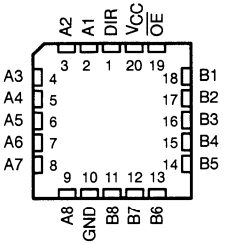
Figure 1. Load Circuit and Voltage Waveforms

- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHC245 . . . J OR W PACKAGE
SN74AHC245 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC245 . . . FK PACKAGE
(TOP VIEW)



description

The 'AHC245 octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

These allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

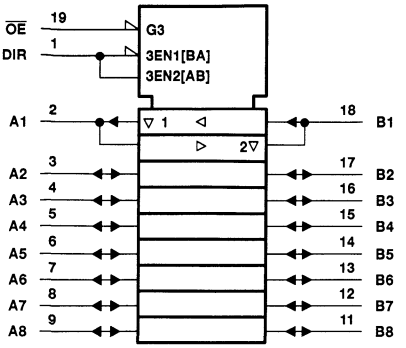
The SN54AHC245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS		OUTPUT
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

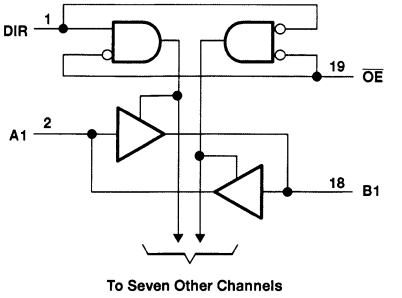
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			SN54AHC245		SN74AHC245		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage	$\overline{OE}$ or DIR	0	5.5	0	5.5	V
V_{IO}	Output voltage	A or B	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC245		SN74AHC245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
			3 V	2.9	3		2.9		2.9		
			4.5 V	4.4	4.5		4.4		4.4		
		I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
		I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
			3 V			0.1		0.1		0.1	
			4.5 V			0.1		0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	A or B inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
	$\overline{OE}$ or DIR					±0.1		±1		±1	
I_{OZ}†		V_O = V_{CC} or GND, V_I (OE) = V_{IL} or V_{IH}	5.5 V			±0.25		±2.5		±2.5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
C_i	$\overline{OE}$ or DIR inputs	V_I = V_{CC} or GND	5 V		2.5	10				10	pF
C_{io}	A or B inputs	V_I = V_{CC} or GND	5 V		4						pF

† The parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHC245					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A or B	B or A	C_L = 15 pF		5.8	8.4	1	10	ns
t_{PHL}*					5.8	8.4	1	10	
t_{PZH}*	$\overline{OE}$	A or B	C_L = 15 pF		8.5	13.2	1	15.5	ns
t_{PZL}*					8.5	13.2	1	15.5	
t_{PHZ}*	$\overline{OE}$	A or B	C_L = 15 pF		8.9	12.5	1	15.5	ns
t_{PLZ}*					8.9	12.5	1	15.5	
t_{PLH}	A or B	B or A	C_L = 50 pF		8.3	11.9	1	13.5	ns
t_{PHL}					8.3	11.9	1	13.5	
t_{PZH}	$\overline{OE}$	A or B	C_L = 50 pF		11	16.7	1	19	ns
t_{PZL}					11	16.7	1	19	
t_{PHZ}	$\overline{OE}$	A or B	C_L = 50 pF		11.5	15.8	1	18	ns
t_{PLZ}					11.5	15.8	1	18	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHC245					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	B or A	C_L = 15 pF		5.8	8.4	1	10	ns
t_{PHL}					5.8	8.4	1	10	
t_{PZH}	$\overline{OE}$	A or B	C_L = 15 pF		8.5	13.2	1	15.5	ns
t_{PZL}					8.5	13.2	1	15.5	
t_{PHZ}	$\overline{OE}$	A or B	C_L = 15 pF		8.9	12.5	1	15.5	ns
t_{PLZ}					8.9	12.5	1	15.5	
t_{PLH}	A or B	B or A	C_L = 50 pF		8.3	11.9	1	13.5	ns
t_{PHL}					8.3	11.9	1	13.5	
t_{PZH}	$\overline{OE}$	A or B	C_L = 50 pF		11	16.7	1	19	ns
t_{PZL}					11	16.7	1	19	
t_{PHZ}	$\overline{OE}$	A or B	C_L = 50 pF		11.5	15.8	1	18	ns
t_{PLZ}					11.5	15.8	1	18	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHC245					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A or B	B or A	C_L = 15 pF		4	5.5	1	6.5	ns
t_{PHL}*					4	5.5	1	6.5	
t_{PZH}*	$\overline{OE}$	A or B	C_L = 15 pF		5.8	8.5	1	10	ns
t_{PZL}*					5.8	8.5	1	10	
t_{PHZ}*	$\overline{OE}$	A or B	C_L = 15 pF		5.6	7.8	1	9.2	ns
t_{PLZ}*					5.6	7.8	1	9.2	
t_{PLH}	A or B	B or A	C_L = 50 pF		5.5	7.5	1	8.5	ns
t_{PHL}					5.5	7.5	1	8.5	
t_{PZH}	$\overline{OE}$	A or B	C_L = 50 pF		7.3	10.6	1	12	ns
t_{PZL}					7.3	10.6	1	12	
t_{PHZ}	$\overline{OE}$	A or B	C_L = 50 pF		7	9.7	1	11	ns
t_{PLZ}					7	9.7	1	11	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHC245					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	B or A	C_L = 15 pF		4	5.5	1	6.5	ns
t_{PHL}					4	5.5	1	6.5	
t_{PZH}	$\overline{OE}$	A or B	C_L = 15 pF		5.8	8.5	1	10	ns
t_{PZL}					5.8	8.5	1	10	
t_{PHZ}	$\overline{OE}$	A or B	C_L = 15 pF		5.6	7.8	1	9.2	ns
t_{PLZ}					5.6	7.8	1	9.2	
t_{PLH}	A or B	B or A	C_L = 50 pF		5.5	7.5	1	8.5	ns
t_{PHL}					5.5	7.5	1	8.5	
t_{PZH}	$\overline{OE}$	A or B	C_L = 50 pF		7.3	10.6	1	12	ns
t_{PZL}					7.3	10.6	1	12	
t_{PHZ}	$\overline{OE}$	A or B	C_L = 50 pF		7	9.7	1	11	ns
t_{PLZ}					7	9.7	1	11	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHC245				UNIT
			T_A = 25°C		MIN	MAX	
			MIN	MAX			
$t_{sk(o)}$	Output skew	3.3 V ± 0.3 V		1.5		1.5	ns
		5 V ± 0.5 V		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

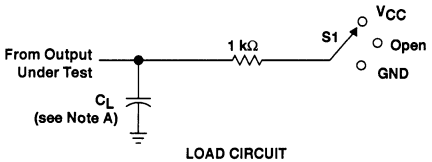
PARAMETER		SN74AHC245			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.9		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.9		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.3		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

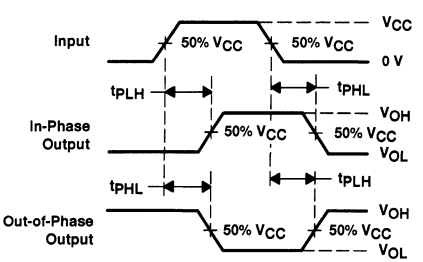
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	No load, f = 1 MHz	14	pF

PARAMETER MEASUREMENT INFORMATION

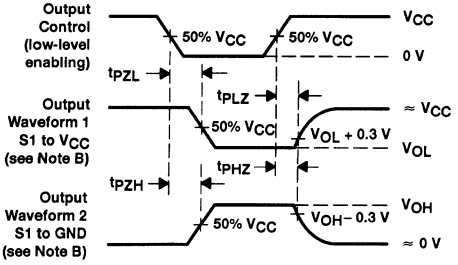


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
DELAY TIMES



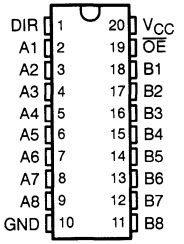
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

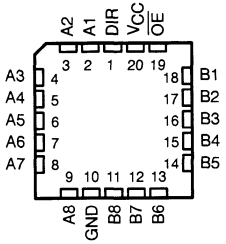
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHCT245 . . . J OR W PACKAGE
SN74AHCT245 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT245 . . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

The 'AHCT245 allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

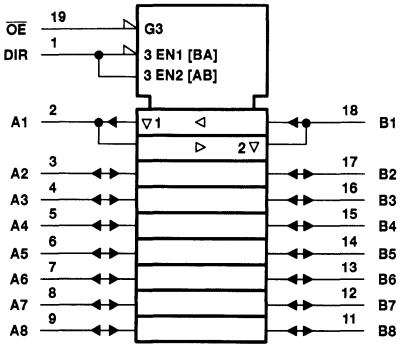
The SN54AHCT245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

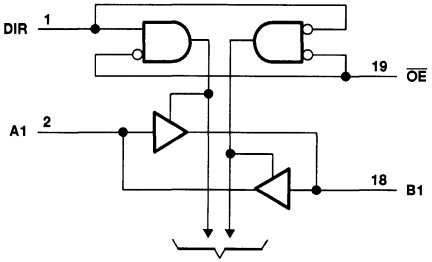
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHCT245		SN74AHCT245		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT245		SN74AHCT245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		3.15		V
		I_{OH} = –8 mA		2.5			2.4		2.4		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		I_{OL} = 8 mA				0.36		0.44		0.44	
I_{OZ}	A or B inputs†	V_O = V_{CC} or GND	5.5 V			±0.25		±2.5		±2.5	μA
I_I	$\overline{OE}$ or DIR	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
ΔI_{CC}‡		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
I_{off}		V_O = 5.5 V	0 V			0.5*				5	μA
C_i	$\overline{OE}$ or DIR	V_I = V_{CC} or GND	5 V		2.5	10				10	pF
C_{io}	A or B inputs	V_I = V_{CC} or GND	5 V		4						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† For I/O ports, the parameter I_{OZ} includes the input leakage current.
‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT245					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A or B	B or A	C_L = 15 pF		4.5	7.7	1	8.5	ns
t_{PHL}*					4.5	7.7	1	8.5	
t_{PZH}*	$\overline{OE}$	A or B	C_L = 15 pF		8.9	13.8	1	15	ns
t_{PZL}*					8.9	13.8	1	15	
t_{PHZ}*	$\overline{OE}$	A or B	C_L = 15 pF		9.2	14.4	1	15.5	ns
t_{PLZ}*					9.2	14.4	1	15.5	
t_{PLH}	A or B	B or A	C_L = 50 pF		5.3	8.7	1	9.5	ns
t_{PHL}					5.3	8.7	1	9.5	
t_{PZH}	$\overline{OE}$	A or B	C_L = 50 pF		9.7	14.8	1	16	ns
t_{PZL}					9.7	14.8	1	16	
t_{PHZ}	$\overline{OE}$	A or B	C_L = 50 pF		10	15.4	1	16.5	ns
t_{PLZ}					10	15.4	1	16.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT245					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	B or A	C_L = 15 pF		4.5	7.7	1	8.5	ns
t_{PHL}					4.5	7.7	1	8.5	
t_{PZH}	$\overline{OE}$	A or B	C_L = 15 pF		8.9	13.8	1	15	ns
t_{PZL}					8.9	13.8	1	15	
t_{PHZ}	$\overline{OE}$	A or B	C_L = 15 pF		9.2	14.4	1	15.5	ns
t_{PLZ}					9.2	14.4	1	15.5	
t_{PLH}	A or B	B or A	C_L = 50 pF		5.3	8.7	1	9.5	ns
t_{PHL}					5.3	8.7	1	9.5	
t_{PZH}	$\overline{OE}$	A or B	C_L = 50 pF		9.7	14.8	1	16	ns
t_{PZL}					9.7	14.8	1	16	
t_{PHZ}	$\overline{OE}$	A or B	C_L = 50 pF		10	15.4	1	16.5	ns
t_{PLZ}					10	15.4	1	16.5	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHCT245				UNIT
			T_A = 25°C		MIN	MAX	
			MIN	MAX			
$t_{sk(o)}$	Output skew	5 V ± 0.5 V		1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

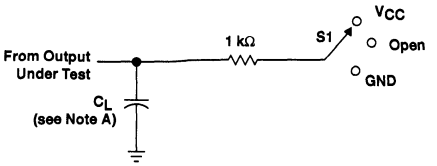
PARAMETER		SN74AHCT245			UNIT
		MIN	TYP	MAX	
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

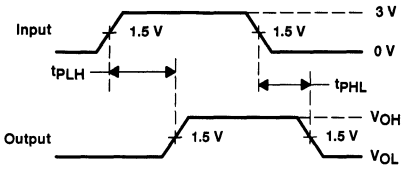
PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	No load,	f = 1 MHz	13	pF

PARAMETER MEASUREMENT INFORMATION

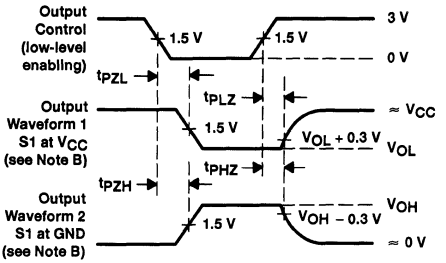


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

These quadruple 2-line to 1-line data selectors/multiplexers are designed for 2-V to 5.5-V V_{CC} operation.

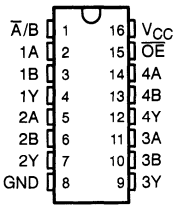
The 'AHC257 are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable ($\overline{OE}$) input is at a high logic level.

The SN54AHC257 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC257 is characterized for operation from –40°C to 85°C.

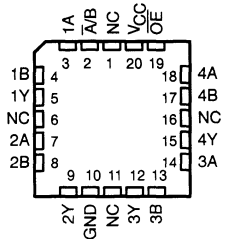
FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	$\overline{A}$/B	A	B	Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

SN54AHC257 . . . J OR W PACKAGE
SN74AHC257 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC257 . . . FK PACKAGE
(TOP VIEW)

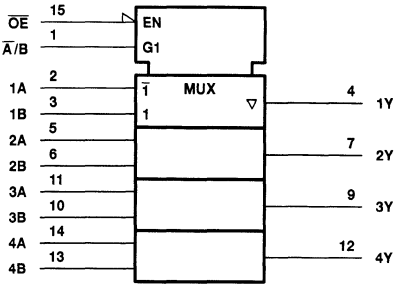


NC – No internal connection

PRODUCT PREVIEW

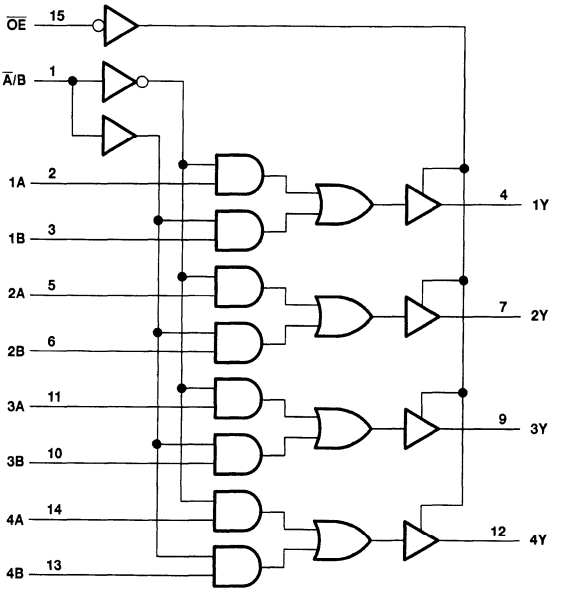
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... −20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.3 W
DB package ..... 0.55 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			SN54AHC257		SN74AHC257		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		−50		−50	μA
		V_{CC} = 3.3 V ± 0.3 V		−4		−4	mA
		V_{CC} = 5 V ± 0.5 V		−8		−8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC257		SN74AHC257		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
	I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
I_{OZ}	V_I = V_{CC} or GND	5.5 V			± 0.25		± 2.5		± 2.5	μA
C_i	V_I = V_{CC} or GND	5 V		4	10				10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC257					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A or B	Y	C_L = 15 pF						ns
t_{PHL}*									
t_{PLH}*	$\overline{A}$/B	Y	C_L = 15 pF						ns
t_{PHL}*									
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF						ns
t_{PZL}*									
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF						ns
t_{PLZ}*									
t_{PLH}	A or B	Y	C_L = 50 pF						ns
t_{PHL}									
t_{PLH}	$\overline{A}$/B	Y	C_L = 50 pF						ns
t_{PHL}									
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF						ns
t_{PZL}									
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF						ns
t_{PLZ}									

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC257 T_A = 25°C MIN	SN74AHC257 T_A = 25°C TYP	SN74AHC257 T_A = 25°C MAX	SN74AHC257 MIN	SN74AHC257 MAX	UNIT
t_{PLH}	A or B	Y	C_L = 15 pF						ns
t_{PHL}									
t_{PLH}	$\overline{A}$/B	Y	C_L = 15 pF						ns
t_{PHL}									
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF						ns
t_{PZL}									
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF						ns
t_{PLZ}									
t_{PLH}	A or B	Y	C_L = 50 pF						ns
t_{PHL}									
t_{PLH}	$\overline{A}$/B	Y	C_L = 50 pF						ns
t_{PHL}									
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF						ns
t_{PZL}									
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF						ns
t_{PLZ}									

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC257 T_A = 25°C MIN	SN54AHC257 T_A = 25°C TYP	SN54AHC257 T_A = 25°C MAX	SN54AHC257 MIN	SN54AHC257 MAX	UNIT
t_{PLH}*	A or B	Y	C_L = 15 pF						ns
t_{PHL}*									
t_{PLH}*	$\overline{A}$/B	Y	C_L = 15 pF						ns
t_{PHL}*									
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF						ns
t_{PZL}*									
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF						ns
t_{PLZ}*									
t_{PLH}	A or B	Y	C_L = 50 pF						ns
t_{PHL}									
t_{PLH}	$\overline{A}$/B	Y	C_L = 50 pF						ns
t_{PHL}									
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF						ns
t_{PZL}									
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF						ns
t_{PLZ}									

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC257					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF						ns
t_{PHL}									
t_{PLH}	$\overline{A}$/B	Y	C_L = 15 pF						ns
t_{PHL}									
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF						ns
t_{PZL}									
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF						ns
t_{PLZ}									
t_{PLH}	A or B	Y	C_L = 50 pF						ns
t_{PHL}									
t_{PLH}	$\overline{A}$/B	Y	C_L = 50 pF						ns
t_{PHL}									
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF						ns
t_{PZL}									
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF						ns
t_{PLZ}									

noise characteristics V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

PARAMETER		SN74AHC257			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	–0.8			V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

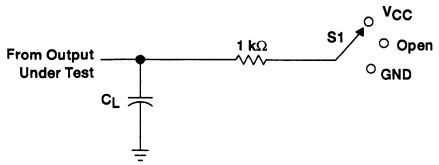
NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	12	pF

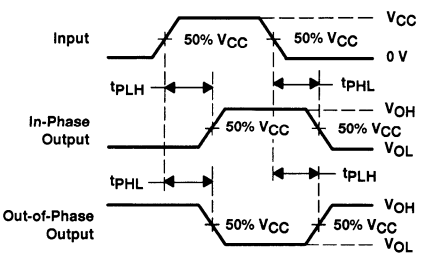
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

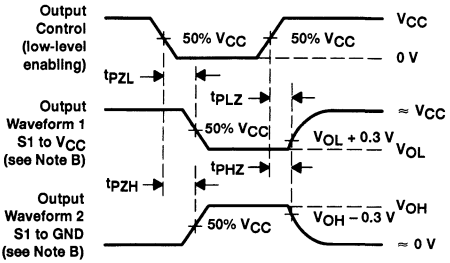


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

These quadruple 2-line to 1-line data selectors/multiplexers are designed for 4.5-V to 5.5-V V_{CC} operation.

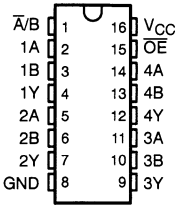
The 'AHCT257 are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable ($\overline{OE}$) input is at the high logic level.

The SN54AHCT257 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT257 is characterized for operation from –40°C to 85°C.

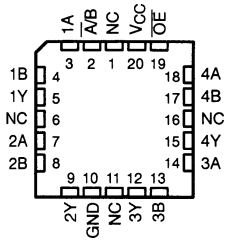
FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	$\overline{A}$/B	A	B	Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

SN54AHCT257 . . . J OR W PACKAGE
SN74AHCT257 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT257 . . . FK PACKAGE
(TOP VIEW)

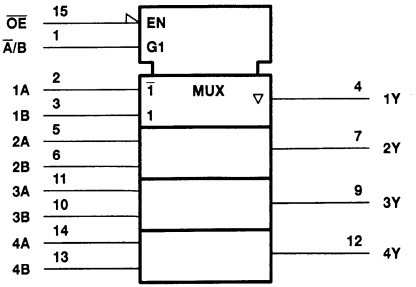


NC – No internal connection

PRODUCT PREVIEW

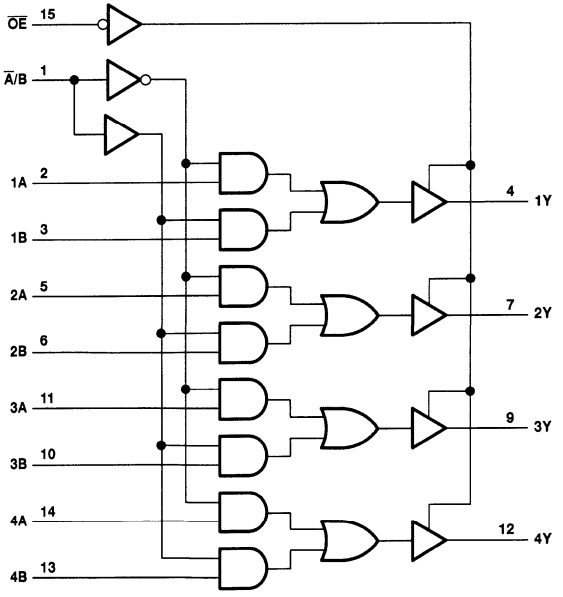
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
DB package ..... 0.55 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHCT257		SN74AHCT257		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall time		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT257		SN74AHCT257		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		3.15		V
	I_{OH} = –8 mA		2.5			2.4		2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
ΔI_{CC}†	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
I_{off}	V_O = 5.5 V	0 V			0.5				5	μA
I_{OZ}	V_I = V_{CC} or GND	5.5 V			±0.25		±2.5		±2.5	μA
C_i	V_I = V_{CC} or GND	5 V		2	10				10	pF

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT257				UNIT
				T_A = 25°C			MIN MAX	
				MIN	TYP	MAX		
t_{PLH}*	A or B	Y	C_L = 15 pF					ns
t_{PHL}*								
t_{PLH}*	$\overline{A}$/B	Y	C_L = 15 pF					ns
t_{PHL}*								
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF					ns
t_{PZL}*								
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF					ns
t_{PLZ}*								
t_{PLH}	A or B	Y	C_L = 50 pF					ns
t_{PHL}								
t_{PLH}	$\overline{A}$/B	Y	C_L = 50 pF					ns
t_{PLH}								
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF					ns
t_{PZL}								
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF					ns
t_{PLZ}								

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT257					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF						ns
t_{PHL}									
t_{PLH}	$\overline{A}$/B	Y	C_L = 15 pF						ns
t_{PHL}									
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF						ns
t_{PZL}									
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF						ns
t_{PLZ}									
t_{PLH}	A or B	Y	C_L = 50 pF						ns
t_{PHL}									
t_{PLH}	$\overline{A}$/B	Y	C_L = 50 pF						ns
t_{PLH}									
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF						ns
t_{PZL}									
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF						ns
t_{PLZ}									

noise characteristics V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

PARAMETER		SN74AHCT257		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	–0.8		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}			V
$V_{IH(D)}$	High-level dynamic input voltage	2		V
$V_{IL(D)}$	Low-level dynamic input voltage		0.8	V

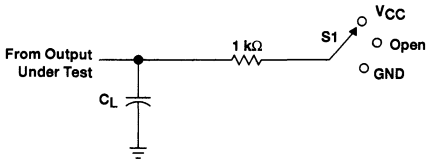
NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz		pF

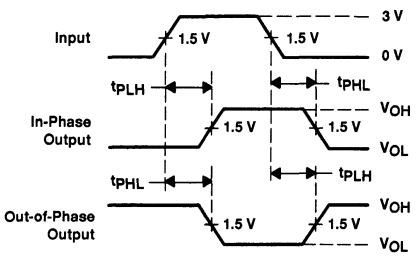
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

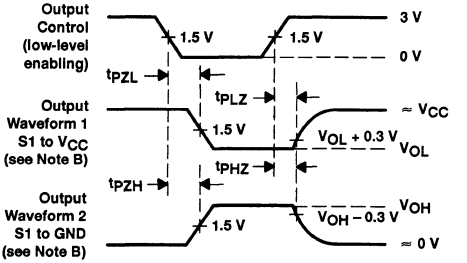


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

These quadruple 2-line to 1-line data selectors/multiplexers are designed for 2-V to 5.5-V V_{CC} operation.

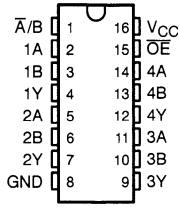
The 'AHC258 are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output enable ($\overline{OE}$) input is at a high logic level.

The SN54AHC258 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC258 is characterized for operation from –40°C to 85°C.

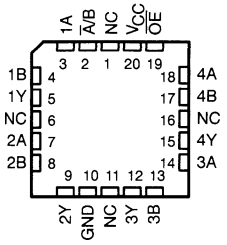
FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	$\overline{A}$/B	A	B	Y
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

SN54AHC258 . . . J OR W PACKAGE
SN74AHC258 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC258 . . . FK PACKAGE
(TOP VIEW)

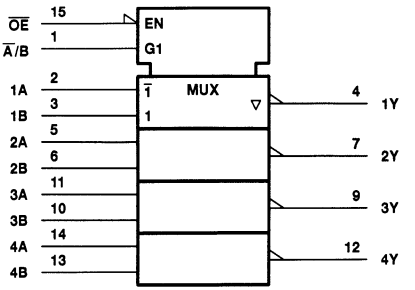


NC – No internal connection

PRODUCT PREVIEW

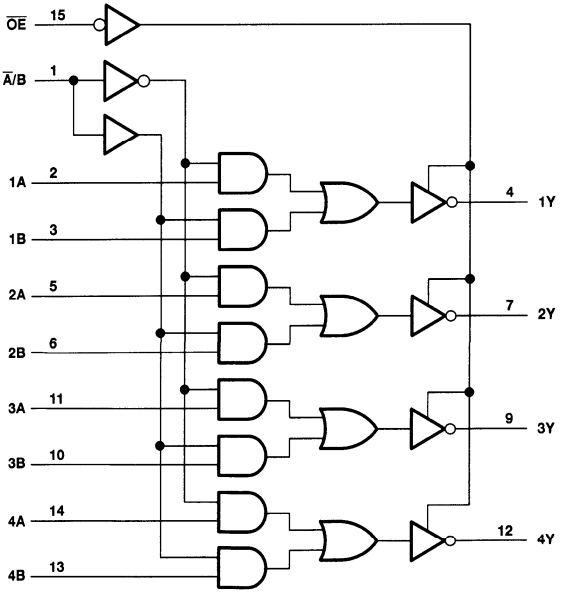
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... −20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.3 W
DB package ..... 0.55 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			SN54AHC258		SN74AHC258		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		−50		−50	μA
		V_{CC} = 3.3 V ± 0.3 V		−4		−4	mA
		V_{CC} = 5 V ± 0.5 V		−8		−8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC258		SN74AHC258		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
	I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
I_{OZ}	V_I = V_{CC} or GND	5.5 V			± 0.25		± 2.5		± 2.5	μA
C_i	V_I = V_{CC} or GND	5 V		4	10				10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC258					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A or B	Y	C_L = 15 pF						ns
t_{PHL}*									
t_{PLH}*	$\overline{A}$/B	Y	C_L = 15 pF						ns
t_{PHL}*									
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF						ns
t_{PZL}*									
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF						ns
t_{PLZ}*									
t_{PLH}	A or B	Y	C_L = 50 pF						ns
t_{PHL}									
t_{PLH}	$\overline{A}$/B	Y	C_L = 50 pF						ns
t_{PHL}									
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF						ns
t_{PZL}									
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF						ns
t_{PLZ}									

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC258					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF						ns
t_{PHL}									
t_{PLH}	$\overline{A}$/B	Y	C_L = 15 pF						ns
t_{PHL}									
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF						ns
t_{PZL}									
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF						ns
t_{PLZ}									
t_{PLH}	A or B	Y	C_L = 50 pF						ns
t_{PHL}									
t_{PLH}	$\overline{A}$/B	Y	C_L = 50 pF						ns
t_{PHL}									
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF						ns
t_{PZL}									
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF						ns
t_{PLZ}									

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC258					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A or B	Y	C_L = 15 pF						ns
t_{PHL}*									
t_{PLH}*	$\overline{A}$/B	Y	C_L = 15 pF						ns
t_{PHL}*									
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF						ns
t_{PZL}*									
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF						ns
t_{PLZ}*									
t_{PLH}	A or B	Y	C_L = 50 pF						ns
t_{PHL}									
t_{PLH}	$\overline{A}$/B	Y	C_L = 50 pF						ns
t_{PHL}									
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF						ns
t_{PZL}									
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF						ns
t_{PLZ}									

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC258				UNIT
				T_A = 25°C			MIN MAX	
				MIN	TYP	MAX		
t_{PLH}	A or B	Y	C_L = 15 pF					ns
t_{PHL}								
t_{PLH}	$\overline{A}$/B	Y	C_L = 15 pF					ns
t_{PHL}								
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF					ns
t_{PZL}								
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF					ns
t_{PLZ}								
t_{PLH}	A or B	Y	C_L = 50 pF					ns
t_{PHL}								
t_{PLH}	$\overline{A}$/B	Y	C_L = 50 pF					ns
t_{PHL}								
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF					ns
t_{PZL}								
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF					ns
t_{PLZ}								

noise characteristics V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

PARAMETER		SN74AHC258			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	–0.8			V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

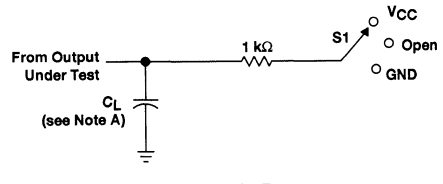
NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	12	pF

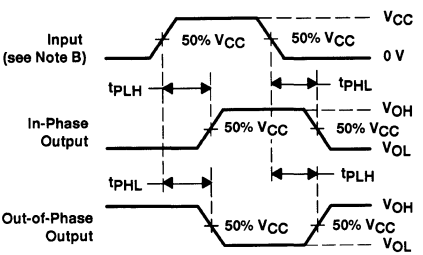
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

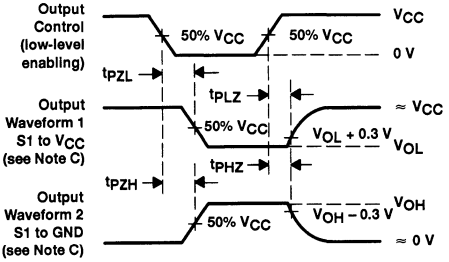


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

These quadruple 2-line to 1-line data selectors/multiplexers are designed for 4.5-V to 5.5-V V_{CC} operation.

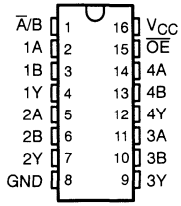
The 'AHCT258 are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable ($\overline{OE}$) input is at the high logic level.

The SN54AHCT258 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT258 is characterized for operation from –40°C to 85°C.

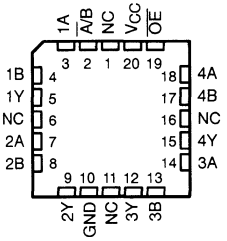
FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	$\overline{A}$/B	A	B	Y
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

SN54AHCT258 . . . J OR W PACKAGE
SN74AHCT258 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT258 . . . FK PACKAGE
(TOP VIEW)

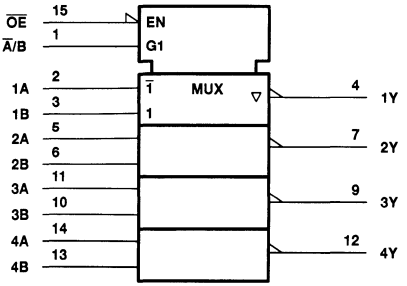


NC – No internal connection

PRODUCT PREVIEW

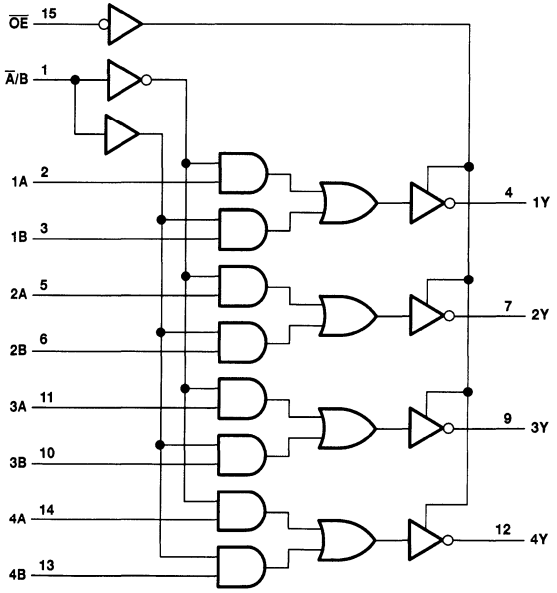
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.3 W
DB package ..... 0.55 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHCT258		SN74AHCT258		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall time		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT258		SN74AHCT258		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		3.15		V
	I_{OH} = –8 mA		2.5			2.4		2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
ΔI_{CC}†	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
I_{off}	V_O = 5.5 V	0 V			0.5				5	μA
I_{OZ}	V_I = V_{CC} or GND	5.5 V			±0.25		±2.5		±2.5	μA
C_i	V_I = V_{CC} or GND	5 V		2	10				10	pF

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT258				UNIT
				T_A = 25°C			MIN MAX	
				MIN	TYP	MAX		
t_{PLH}*	A or B	Y	C_L = 15 pF					ns
t_{PHL}*								
t_{PLH}*	$\overline{A}$/B	Y	C_L = 15 pF					ns
t_{PHL}*								
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF					ns
t_{PZL}*								
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF					ns
t_{PLZ}*								
t_{PLH}	A or B	Y	C_L = 50 pF					ns
t_{PHL}								
t_{PLH}	$\overline{A}$/B	Y	C_L = 50 pF					ns
t_{PLH}								
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF					ns
t_{PZL}								
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF					ns
t_{PLZ}								

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT258 T_A = 25°C MIN	TYP	MAX	SN74AHCT258 MIN	MAX	UNIT
t_{PLH}	A or B	Y	C_L = 15 pF						ns
t_{PHL}									
t_{PLH}	$\overline{A}$/B	Y	C_L = 15 pF						ns
t_{PHL}									
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF						ns
t_{PZL}									
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF						ns
t_{PLZ}									
t_{PLH}	A or B	Y	C_L = 50 pF						ns
t_{PHL}									
t_{PLH}	$\overline{A}$/B	Y	C_L = 50 pF						ns
t_{PLH}									
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF						ns
t_{PZL}									
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF						ns
t_{PLZ}									

noise characteristics V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

PARAMETER		SN74AHCT258 MIN	SN74AHCT258 MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	–0.8		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}			V
$V_{IH(D)}$	High-level dynamic input voltage	2		V
$V_{IL(D)}$	Low-level dynamic input voltage		0.8	V

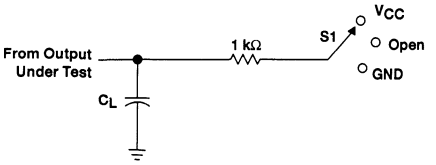
NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz		pF

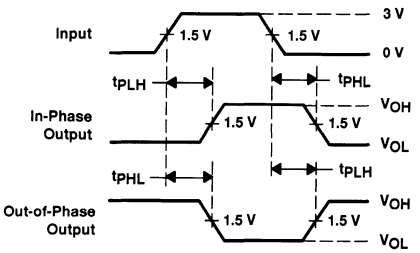
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

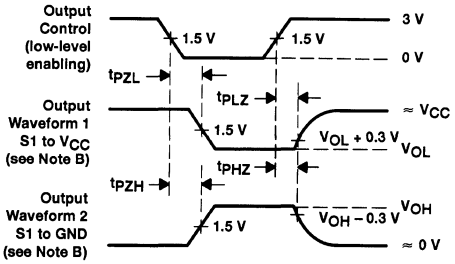


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES



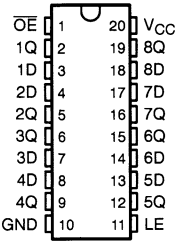
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

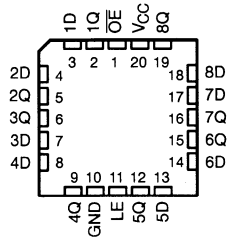
Figure 1. Load Circuit and Voltage Waveforms

- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHC373 . . . J OR W PACKAGE
SN74AHC373 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC373 . . . FK PACKAGE
(TOP VIEW)



description

The 'AHC373 are octal transparent D-type latches.

When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

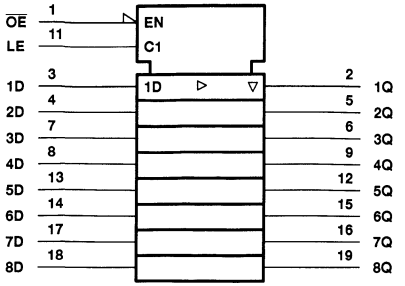
The SN54AHC373 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC373 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

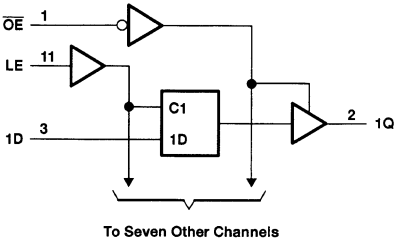
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... −20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			SN54AHC373		SN74AHC373		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		– 50		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		– 4		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC373		SN74AHC373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = – 50 μA	2 V	1.9			1.9		1.9		V
		3 V	2.9			2.9		2.9		
		4.5 V	4.4			4.4		4.4		
	I_{OH} = – 4 mA	3 V	2.58			2.48		2.48		
	I_{OH} = – 8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{OZ}	V_I = V_{IH} or V_{IL}, V_O = V_{CC} or GND	5.5 V			± 0.25		± 2.5		± 2.5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
C_i	V_I = V_{CC} or GND	5 V		4	10				10	pF
C_o	V_O = V_{CC} or GND	5 V		6						pF

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54AHC373		SN74AHC373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, $\overline{LE}$ high	5		5		5		ns
t_{su}	Setup time, data before $\overline{LE}\downarrow$	4		4		4		ns
t_h	Hold time, data after $\overline{LE}\downarrow$	1		1		1		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54AHC373		SN74AHC373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, $\overline{LE}$ high	5		5		5		ns
t_{su}	Setup time, data before $\overline{LE}\downarrow$	4		4		4		ns
t_h	Hold time, data after $\overline{LE}\downarrow$	1		1		1		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHC373					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	D	Q	C_L = 15 pF		7.3	11.4	1	13.5	ns
t_{PHL}*					7.3	11.4	1	13.5	
t_{PLH}*	LE	Q	C_L = 15 pF		7	11	1	13	ns
t_{PHL}*					7	11	1	13	
t_{PZH}*	$\overline{OE}$	Q	C_L = 15 pF		7.3	11.4	1	13.5	ns
t_{PZL}*					7.3	11.4	1	13.5	
t_{PHZ}*	$\overline{OE}$	Q	C_L = 15 pF		7	10	1	12	ns
t_{PLZ}*					7	10	1	12	
t_{PLH}	D	Q	C_L = 50 pF		9.8	14.9	1	17	ns
t_{PHL}					9.8	14.9	1	17	
t_{PLH}	LE	Q	C_L = 50 pF		9.5	14.5	1	16.5	ns
t_{PHL}					9.5	14.5	1	16.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		9.8	14.9	1	17	ns
t_{PZL}					9.8	14.9	1	17	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		9.5	13.2	1	15	ns
t_{PLZ}					9.5	13.2	1	15	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHC373					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	D	Q	C_L = 15 pF		7.3	11.4	1	13.5	ns
t_{PHL}					7.3	11.4	1	13.5	
t_{PLH}	LE	Q	C_L = 15 pF		7	11	1	13	ns
t_{PHL}					7	11	1	13	
t_{PZH}	$\overline{OE}$	Q	C_L = 15 pF		7.3	11.4	1	13.5	ns
t_{PZL}					7.3	11.4	1	13.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 15 pF		7	10	1	12	ns
t_{PLZ}					7	10	1	12	
t_{PLH}	D	Q	C_L = 50 pF		9.8	14.9	1	17	ns
t_{PHL}					9.8	14.9	1	17	
t_{PLH}	LE	Q	C_L = 50 pF		9.5	14.5	1	16.5	ns
t_{PHL}					9.5	14.5	1	16.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		9.8	14.9	1	17	ns
t_{PZL}					9.8	14.9	1	17	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		9.5	13.2	1	15	ns
t_{PLZ}					9.5	13.2	1	15	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHC373					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	D	Q	C_L = 15 pF		5	7.2	1	8.5	ns
t_{PHL}*					5	7.2	1	8.5	
t_{PLH}*	LE	Q	C_L = 15 pF		4.9	7.2	1	8.5	ns
t_{PHL}*					4.9	7.2	1	8.5	
t_{PZH}*	$\overline{OE}$	Q	C_L = 15 pF		5.5	8.1	1	9.5	ns
t_{PZL}*					5.5	8.1	1	9.5	
t_{PHZ}*	$\overline{OE}$	Q	C_L = 15 pF		5	7.2	1	8.5	ns
t_{PLZ}*					5	7.2	1	8.5	
t_{PLH}	D	Q	C_L = 50 pF		6.5	9.2	1	10.5	ns
t_{PHL}					6.5	9.2	1	10.5	
t_{PLH}	LE	Q	C_L = 50 pF		6.4	9.2	1	10.5	ns
t_{PHL}					6.4	9.2	1	10.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		7	10.1	1	11.5	ns
t_{PZL}					7	10.1	1	11.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		6.5	9.2	1	10.5	ns
t_{PLZ}					6.5	9.2	1	10.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHC373					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	D	Q	C_L = 15 pF		5	7.2	1	8.5	ns
t_{PHL}					5	7.2	1	8.5	
t_{PLH}	LE	Q	C_L = 15 pF		4.9	7.2	1	8.5	ns
t_{PHL}					4.9	7.2	1	8.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 15 pF		5.5	8.1	1	9.5	ns
t_{PZL}					5.5	8.1	1	9.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 15 pF		5	7.2	1	8.5	ns
t_{PLZ}					5	7.2	1	8.5	
t_{PLH}	D	Q	C_L = 50 pF		6.5	9.2	1	10.5	ns
t_{PHL}					6.5	9.2	1	10.5	
t_{PLH}	LE	Q	C_L = 50 pF		6.4	9.2	1	10.5	ns
t_{PHL}					6.4	9.2	1	10.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		7	10.1	1	11.5	ns
t_{PZL}					7	10.1	1	11.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		6.5	9.2	1	10.5	ns
t_{PLZ}					6.5	9.2	1	10.5	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHC373				UNIT
			T_A = 25°C		MIN	MAX	
			MIN	MAX			
$t_{sk(o)}$	Output skew	3.3 V ± 0.3 V		1.5		1.5	ns
		5 V ± 0.5 V		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

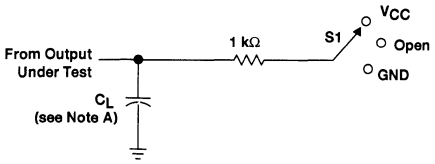
PARAMETER		SN74AHC373			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.1			V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

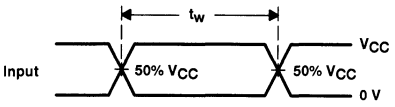
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	18	pF

PARAMETER MEASUREMENT INFORMATION

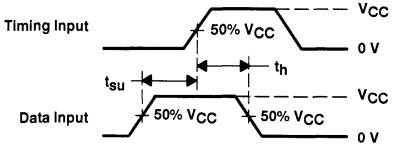


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

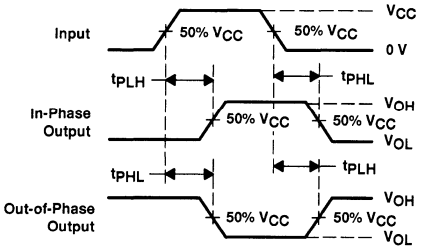
LOAD CIRCUIT



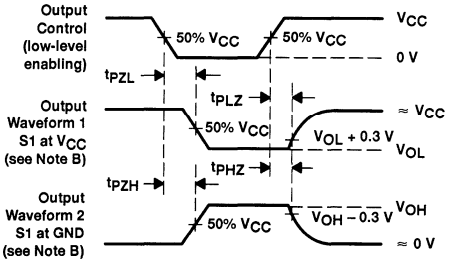
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
DELAY TIMES



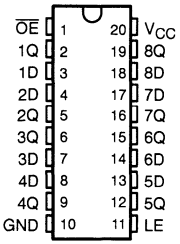
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

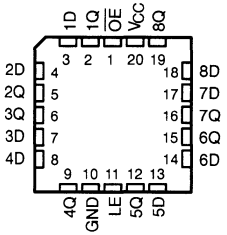
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHCT373 . . . J OR W PACKAGE
SN74AHCT373 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT373 . . . FK PACKAGE
(TOP VIEW)



description

The 'AHCT373 are octal-transparent D-type latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

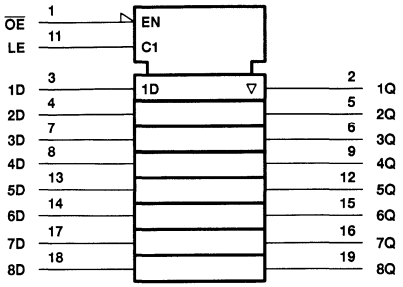
The SN54AHCT373 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT373 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

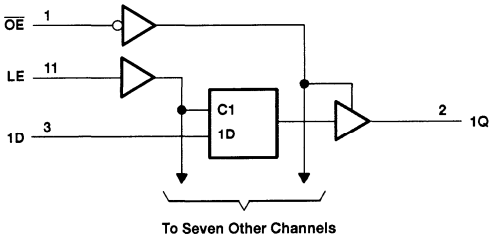
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at T_A = 55°C (in still air)(see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHCT373		SN74AHCT373		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT373		SN74AHCT373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		3.15		V
	I_{OH} = –8 mA		2.5			2.4		2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.25		±2.5		±2.5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		40		40	μA
ΔI_{CC}†	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
I_{off}	V_O = 5.5 V	0 V			0.5*				5	μA
C_i	$V_I = V_{CC}$ or GND	5 V		4						pF
C_o	$V_O = V_{CC}$ or GND	5 V		9						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54AHCT373		SN74AHCT373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, $\overline{LE}$ high	6.5		6.5		6.5		ns
t_{su}	Setup time, data before $\overline{LE}\downarrow$	1.5		1.5		1.5		ns
t_h	Hold time, data after $\overline{LE}\downarrow$	3.5		3.5		3.5		ns

switching characteristics over recommended free-air temperature operating range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHCT373					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	D	Q	C_L = 15 pF		5.1	8.5	1	9.5	ns
t_{PHL}*					5.1	8.5	1	9.5	
t_{PLH}*	LE	Q	C_L = 15 pF		7.7	12.3	1	13.5	ns
t_{PHL}*					7.7	12.3	1	13.5	
t_{PZH}*	$\overline{OE}$	Q	C_L = 15 pF		6.3	10.9	1	12.5	ns
t_{PZL}*					6.3	10.9	1	12.5	
t_{PHZ}*	$\overline{OE}$	Q	C_L = 15 pF		6	10.2	1	11	ns
t_{PLZ}*					6	10.2	1	11	
t_{PLH}	D	Q	C_L = 50 pF		5.9	9.5	1	10.5	ns
t_{PHL}					5.9	9.5	1	10.5	
t_{PLH}	LE	Q	C_L = 50 pF		8.5	13.3	1	14.5	ns
t_{PHL}					8.5	13.3	1	14.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		7.1	11.9	1	13.5	ns
t_{PZL}					7.1	11.9	1	13.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		6.8	11.2	1	12	ns
t_{PLZ}					6.8	11.2	1	12	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended free-air temperature operating range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHCT373					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	D	Q	C_L = 15 pF		5.1	8.5	1	9.5	ns
t_{PHL}					5.1	8.5	1	9.5	
t_{PLH}	LE	Q	C_L = 15 pF		7.7	12.3	1	13.5	ns
t_{PHL}					7.7	12.3	1	13.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 15 pF		6.3	10.9	1	12.5	ns
t_{PZL}					6.3	10.9	1	12.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 15 pF		6	10.2	1	11	ns
t_{PLZ}					6	10.2	1	11	
t_{PLH}	D	Q	C_L = 50 pF		5.9	9.5	1	10.5	ns
t_{PHL}					5.9	9.5	1	10.5	
t_{PLH}	LE	Q	C_L = 50 pF		8.5	13.3	1	14.5	ns
t_{PHL}					8.5	13.3	1	14.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		7.1	11.9	1	13.5	ns
t_{PZL}					7.1	11.9	1	13.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		6.8	11.2	1	12	ns
t_{PLZ}					6.8	11.2	1	12	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHCT373				UNIT
			T_A = 25°C		MIN	MAX	
			MIN	MAX			
$t_{sk(o)}$	Output skew	5 V ± 0.5 V		1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

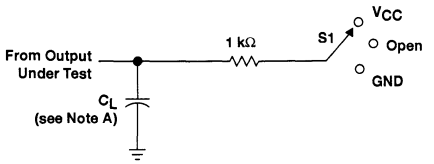
PARAMETER		SN74AHCT373			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	1.2	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.8	–1.2	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.1			V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

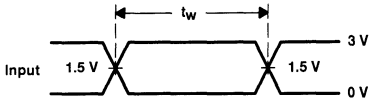
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	17	pF

PARAMETER MEASUREMENT INFORMATION

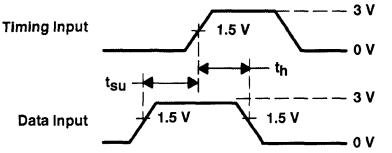


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

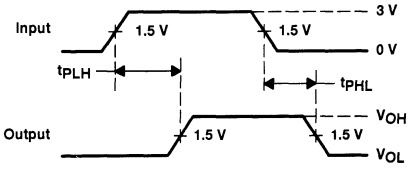
LOAD CIRCUIT



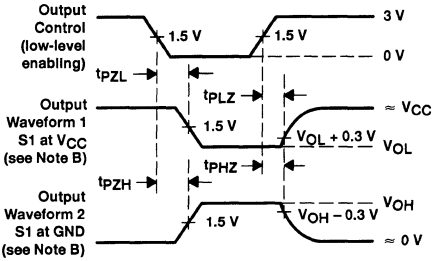
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
DELAY TIMES



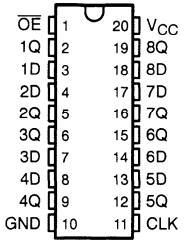
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

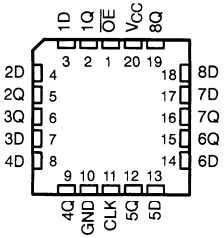
Figure 1. Load Circuit and Voltage Waveforms

- **Operating Range 2-V to 5.5-V V_{CC}**
- **3-State Outputs Drive Bus Lines Directly**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHC374 . . . J OR W PACKAGE
SN74AHC374 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC374 . . . FK PACKAGE
(TOP VIEW)



description

The 'AHC374 are octal edge-triggered D-type flip-flops that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

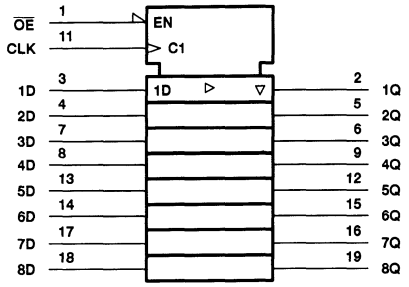
The SN54AHC374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC374 is characterized for operation from –40°C to 85°C.

EPIC is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE
(each flip-flop)

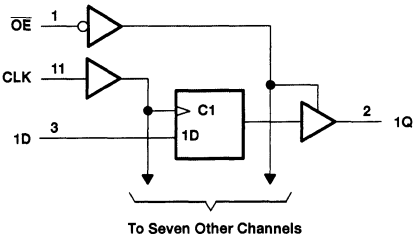
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			SN54AHC374		SN74AHC374		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC374		SN74AHC374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
	I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.25		±2.5		±2.5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
C_i	V_I = V_{CC} or GND	5 V		4	10				10	pF
C_o	V_O = V_{CC} or GND	5 V		6						pF

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54AHC374		SN74AHC374		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, CLK high or low	5		5.5		5.5		ns
t_{su}	Setup time, data before CLK↑	4.5		4		4		ns
t_h	Hold time, data after CLK↑	2		2		2		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54AHC374		SN74AHC374		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, CLK high or low	5		5		5		ns
t_{su}	Setup time, data before CLK↑	3		3		3		ns
t_h	Hold time, data after CLK↑	2		2		2		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHC374					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	80	130		70		MHz
			C_L = 50 pF	55	85		50		
t_{PLH}*	CLK	Q	C_L = 15 pF		8.1	12.7	1	15	ns
t_{PHL}*					8.1	12.7	1	15	
t_{PZH}*	$\overline{OE}$	Q	C_L = 15 pF		7.1	11	1	13	ns
t_{PZL}*					7.1	11	1	13	
t_{PHZ}*	$\overline{OE}$	Q	C_L = 15 pF		7.5	10.5	1	12.5	ns
t_{PLZ}*					7.5	10.5	1	12.5	
t_{PLH}	CLK	Q	C_L = 50 pF		10.6	16.2	1	18.5	ns
t_{PHL}					10.6	16.2	1	18.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		9.6	14.5	1	16.5	ns
t_{PZL}					9.6	14.5	1	16.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		10.2	14	1	16	ns
t_{PLZ}					10.2	14	1	16	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHC374					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	80	130		70		MHz
			C_L = 50 pF	55	85		50		
t_{PLH}	CLK	Q	C_L = 15 pF		8.1	12.7	1	15	ns
t_{PHL}					8.1	12.7	1	15	
t_{PZH}	$\overline{OE}$	Q	C_L = 15 pF		7.1	11	1	13	ns
t_{PZL}					7.1	11	1	13	
t_{PHZ}	$\overline{OE}$	Q	C_L = 15 pF		7.5	10.5	1	12.5	ns
t_{PLZ}					7.5	10.5	1	12.5	
t_{PLH}	CLK	Q	C_L = 50 pF		10.6	16.2	1	18.5	ns
t_{PHL}					10.6	16.2	1	18.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		9.6	14.5	1	16.5	ns
t_{PZL}					9.6	14.5	1	16.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		10.2	14	1	16	ns
t_{PLZ}					10.2	14	1	16	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHC374					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	130	185		110		MHz
			C_L = 50 pF	85	120		75		
t_{PLH}*	CLK	Q	C_L = 15 pF		5.4	8.1	1	9.5	ns
t_{PHL}*					5.4	8.1	1	9.5	
t_{PZH}*	$\overline{OE}$	Q	C_L = 15 pF		5.1	7.6	1	9	ns
t_{PZL}*					5.1	7.6	1	9	
t_{PHZ}*	$\overline{OE}$	Q	C_L = 15 pF		4.6	6.8	1	8	ns
t_{PLZ}*					4.6	6.8	1	8	
t_{PLH}	CLK	Q	C_L = 50 pF		6.9	10.1	1	11.5	ns
t_{PHL}					6.9	10.1	1	11.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		6.6	9.6	1	11	ns
t_{PZL}					6.6	9.6	1	11	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		6.1	8.8	1	10	ns
t_{PLZ}					6.1	8.8	1	10	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHC374					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	130	185		110		MHz
			C_L = 50 pF	85	120		75		
t_{PLH}	CLK	Q	C_L = 15 pF		5.4	8.1	1	9.5	ns
t_{PHL}					5.4	8.1	1	9.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 15 pF		5.1	7.6	1	9	ns
t_{PZL}					5.1	7.6	1	9	
t_{PHZ}	$\overline{OE}$	Q	C_L = 15 pF		4.6	6.8	1	8	ns
t_{PLZ}					4.6	6.8	1	8	
t_{PLH}	CLK	Q	C_L = 50 pF		6.9	10.1	1	11.5	ns
t_{PHL}					6.9	10.1	1	11.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		6.6	9.6	1	11	ns
t_{PZL}					6.6	9.6	1	11	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		6.1	8.8	1	10	ns
t_{PLZ}					6.1	8.8	1	10	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHC374				UNIT
			T_A = 25°C		MIN	MAX	
			MIN	MAX			
$t_{sk(o)}$	Output skew	3.3 V ± 0.3 V		1.5		1.5	ns
		5 V ± 0.5 V		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

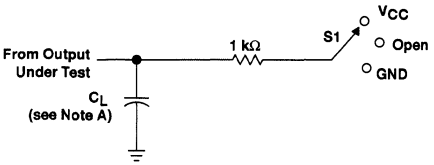
PARAMETER		SN74AHC374			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5	1	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.5	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4			V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

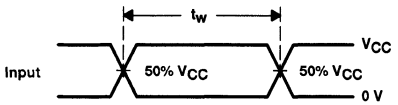
PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	32	pF

PARAMETER MEASUREMENT INFORMATION

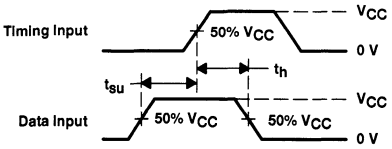


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

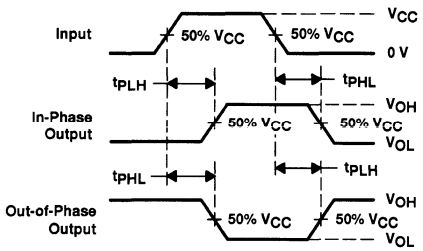
LOAD CIRCUIT



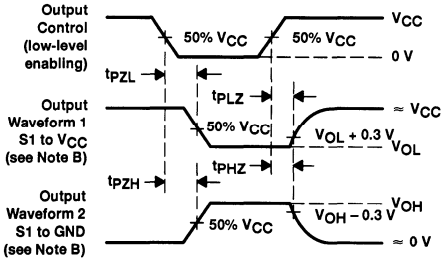
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
DELAY TIMES



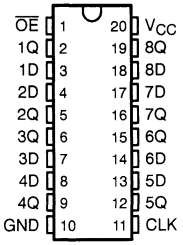
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

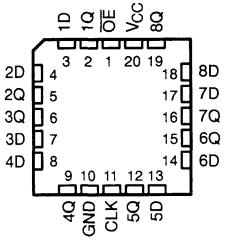
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHCT374 . . . J OR W PACKAGE
SN74AHCT374 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT374 . . . FK PACKAGE
(TOP VIEW)



description

The 'AHCT374 are octal edge-triggered D-type flip-flops that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AHCT374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT374 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

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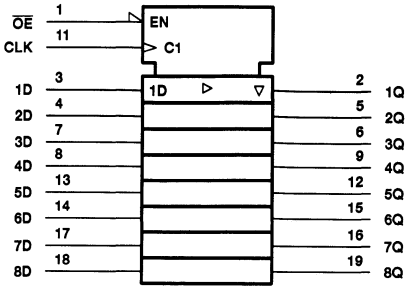
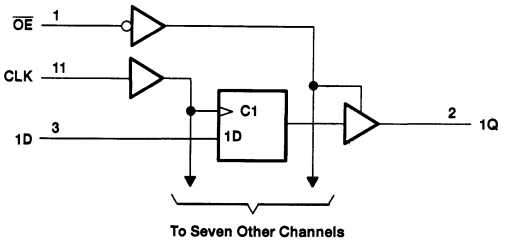
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at $T_A = 55°C$ (in still air)(see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHCT374		SN74AHCT374		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT374		SN74AHCT374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		3.15		V
	I_{OH} = –8 mA		2.5			2.4		2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_{OZ}	$V_O = V_{CC}$ or GND, $V_I = V_{IH}$ or V_{IL}	5.5 V			±0.25		±2.5		±2.5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		40		40	μA
ΔI_{CC}†	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
I_{off}	V_O = 5.5 V	0 V			0.5*				5	μA
C_i	$V_I = V_{CC}$ or GND	5 V		4	10				10	pF
C_o	$V_O = V_{CC}$ or GND	5 V		9						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54AHCT374		SN74AHCT374		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, CLK high or low	6.5		6.5		6.5		ns
t_{su}	Setup time, data before CLK↑	2.5		2.5		2.5		ns
t_h	Hold time, data after CLK↑	2.5		2.5		2.5		ns

switching characteristics over recommended free-air temperature operating range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT374					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	90	140		80		MHz
			C_L = 50 pF	85	130		75		
t_{PLH}*	CLK	Q	C_L = 15 pF		5.6	9.4	1	10.5	ns
t_{PHL}*					5.6	9.4	1	10.5	
t_{PZH}*	$\overline{OE}$	Q	C_L = 15 pF		6.5	10.2	1	11.5	ns
t_{PZL}*					6.5	10.2	1	11.5	
t_{PHZ}*	$\overline{OE}$	Q	C_L = 15 pF		6.2	10.2	1	11	ns
t_{PLZ}*					6.2	10.2	1	11	
t_{PLH}	CLK	Q	C_L = 50 pF		6.4	10.4	1	11.5	ns
t_{PHL}					6.4	10.4	1	11.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		7.3	11.2	1	12.5	ns
t_{PZL}					7.3	11.2	1	12.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		7	11.2	1	12	ns
t_{PLZ}					7	11.2	1	12	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended free-air temperature operating range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT374					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	90	140		80		MHz
			C_L = 50 pF	85	130		75		
t_{PLH}	CLK	Q	C_L = 15 pF		5.6	9.4	1	10.5	ns
t_{PHL}					5.6	9.4	1	10.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 15 pF		6.5	10.2	1	11.5	ns
t_{PZL}					6.5	10.2	1	11.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 15 pF		6.2	10.2	1	11	ns
t_{PLZ}					6.2	10.2	1	11	
t_{PLH}	CLK	Q	C_L = 50 pF		6.4	10.4	1	11.5	ns
t_{PHL}					6.4	10.4	1	11.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		7.3	11.2	1	12.5	ns
t_{PZL}					7.3	11.2	1	12.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		7	11.2	1	12	ns
t_{PLZ}					7	11.2	1	12	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHCT374				UNIT
			T_A = 25°C		MIN	MAX	
			MIN	MAX			
$t_{sk(o)}$	Output skew	5 V ± 0.5 V		1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

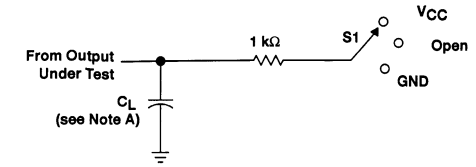
PARAMETER		SN74AHCT374			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	1.2	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.8	–1.2	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	3.8			V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

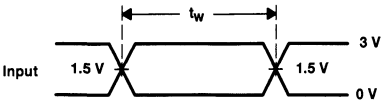
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	27	pF

PARAMETER MEASUREMENT INFORMATION

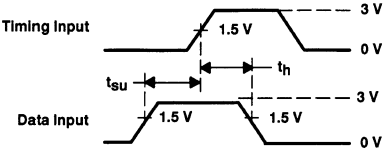


LOAD CIRCUIT

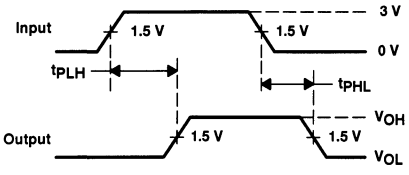
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



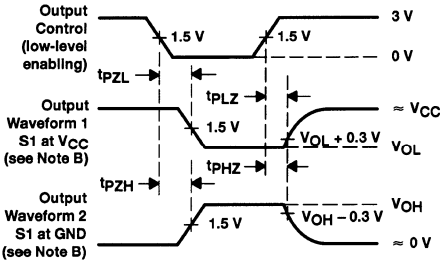
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
DELAY TIMES



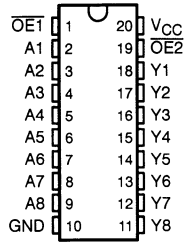
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

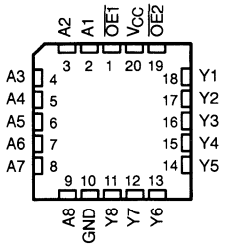
Figure 1. Load Circuit and Voltage Waveforms

- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHC540 . . . J OR W PACKAGE
SN74AHC540 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC540 . . . FK PACKAGE
(TOP VIEW)



description

The 'AHC540 octal buffers/drivers are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package to facilitate printed-circuit-board layout.

The 3-state control gate is a two-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide inverted data when they are not in the high-impedance state.

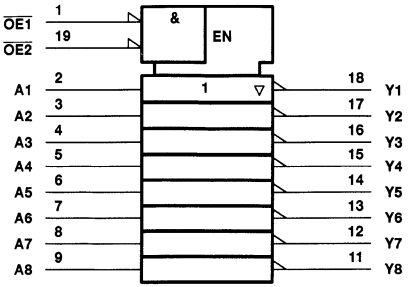
The SN54AHC540 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC540 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer/driver)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

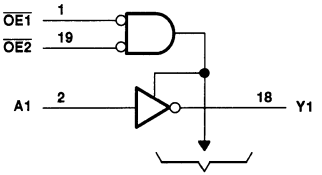
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			SN54AHC540		SN74AHC540		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC540		SN74AHC540		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
			3 V	2.9	3		2.9		2.9		
			4.5 V	4.4	4.5		4.4		4.4		
		I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
		I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
			3 V			0.1		0.1		0.1	
			4.5 V			0.1		0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	Data inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
	Control inputs					±0.1		±1		±1	
I_{OZ}†		V_O = V_{CC} or GND, V_I ($\overline{OE}$) = V_{IL} or V_{IH}	5.5 V			±0.25		±2.5		±2.5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
C_i		V_I = V_{CC} or GND	5 V		2	10				10	pF
C_o		V_O = V_{CC} or GND	5 V		4						pF

† For I/O pins, the parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC540					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A	Y	C_L = 15 pF		4.8	7	1	8.5	ns
t_{PHL}*					4.8	7	1	8.5	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		6.8	10.5	1	12.5	ns
t_{PZL}*					6.8	10.5	1	12.5	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		6.8	10.5	1	12.5	ns
t_{PLZ}*					6.8	10.5	1	12.5	
t_{PLH}	A	Y	C_L = 50 pF		7.3	10.5	1	12	ns
t_{PHL}					7.3	10.5	1	12	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		8	14	1	16	ns
t_{PZL}					8	14	1	16	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		8	15.4	1	17.5	ns
t_{PLZ}					8	15.4	1	17.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC540					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		4.8	7	1	8.5	ns
t_{PHL}					4.8	7	1	8.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF		6.8	10.5	1	12.5	ns
t_{PZL}					6.8	10.5	1	12.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF		6.8	10.5	1	12.5	ns
t_{PLZ}					6.8	10.5	1	12.5	
t_{PLH}	A	Y	C_L = 50 pF		7.3	10.5	1	12	ns
t_{PHL}					7.3	10.5	1	12	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		8	14	1	16	ns
t_{PZL}					8	14	1	16	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		8	15.4	1	17.5	ns
t_{PLZ}					8	15.4	1	17.5	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC540					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A	Y	C_L = 15 pF		3.7	5	1	6	ns
t_{PHL}*					3.7	5	1	6	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		4.7	7.2	1	8.5	ns
t_{PZL}*					4.7	7.2	1	8.5	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		4.5	6.8	1	8	ns
t_{PLZ}*					4.5	6.8	1	8	
t_{PLH}	A	Y	C_L = 50 pF		5.2	7	1	8	ns
t_{PHL}					5.2	7	1	8	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		6.2	9.2	1	10.5	ns
t_{PZL}					6.2	9.2	1	10.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		6	8.8	1	10	ns
t_{PLZ}					6	8.8	1	10	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC540					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		3.7	5	1	6	ns
t_{PHL}					3.7	5	1	6	
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF		4.7	7.2	1	8.5	ns
t_{PZL}					4.7	7.2	1	8.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF		4.5	6.8	1	8	ns
t_{PLZ}					4.5	6.8	1	8	
t_{PLH}	A	Y	C_L = 50 pF		5.2	7	1	8	ns
t_{PHL}					5.2	7	1	8	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		6.2	9.2	1	10.5	ns
t_{PZL}					6.2	9.2	1	10.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		6	8.8	1	10	ns
t_{PLZ}					6	8.8	1	10	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN74AHC540				UNIT
				T_A = 25°C		MIN	MAX	
				MIN	MAX			
$t_{sk(o)}$	A	Y	3.3 V ± 0.3 V		1.5		1.5	ns
			5 V ± 0.5 V		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

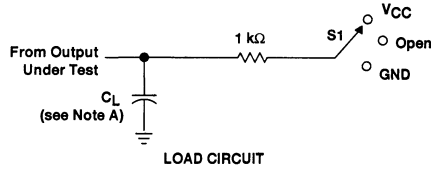
PARAMETER		SN74AHC540 MIN	SN74AHC540 MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.7		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

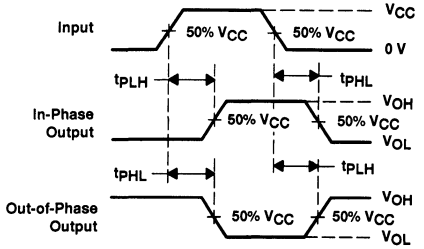
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	12	pF

PARAMETER MEASUREMENT INFORMATION

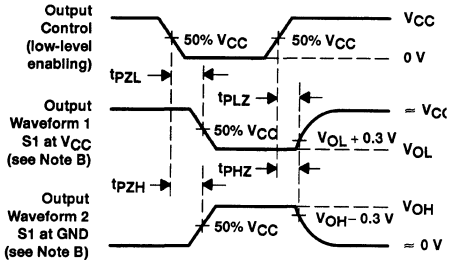


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
DELAY TIMES



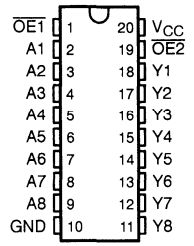
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

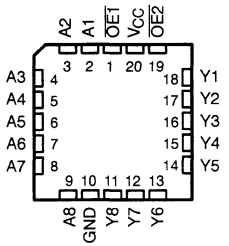
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHCT540 . . . J OR W PACKAGE
SN74AHCT540 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT540 . . . FK PACKAGE
(TOP VIEW)



description

The 'AHCT540 octal buffers/drivers are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package to facilitate printed-circuit-board layout.

The 3-state control gate is a two-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide inverted data when they are not in the high-impedance state.

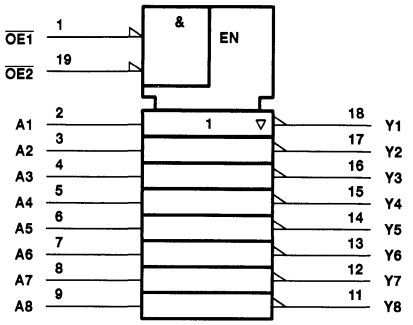
The SN54AHCT540 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT540 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

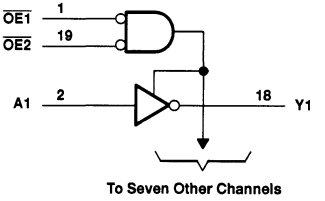
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHCT540		SN74AHCT540		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT540		SN74AHCT540		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		3.15		V
	I_{OH} = –8 mA		2.5			2.4		2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.25		±2.5		±2.5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
ΔI_{CC}†	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			1.35		1.5		1.5	mA
I_{off}	V_O = 5.5 V	0 V			0.5*				5	μA
C_i	V_I = V_{CC} or GND	5 V		2	10				10	pF
C_o	V_O = V_{CC} or GND	5 V		4						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT540					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A	Y	C_L = 15 pF		4	6	1	7.5	ns
t_{PHL}*					4	6	1	7.5	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		5.5	8	1	9	ns
t_{PZL}*					5.5	8	1	9	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		5	8	1	9	ns
t_{PLZ}*					5	8	1	9	
t_{PLH}	A	Y	C_L = 50 pF		6	8.5	1	10	ns
t_{PHL}					6	8.5	1	10	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		7.5	11	1	12	ns
t_{PZL}					7.5	11	1	12	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		8	11	1	12	ns
t_{PLZ}					8	11	1	12	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT540					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		4	6	1	7.5	ns
t_{PHL}					4	6	1	7.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF		5.5	8	1	9	ns
t_{PZL}					5.5	8	1	9	
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF		5	8	1	9	ns
t_{PLZ}					5	8	1	9	
t_{PLH}	A	Y	C_L = 50 pF		6	8.5	1	10	ns
t_{PHL}					6	8.5	1	10	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		7.5	11	1	12	ns
t_{PZL}					7.5	11	1	12	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		8	11	1	12	ns
t_{PLZ}					8	11	1	12	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN74AHCT540				UNIT
				T_A = 25°C		MIN	MAX	
				MIN	MAX			
$t_{sk(o)}$	A	Y	5 V ± 0.5 V		1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

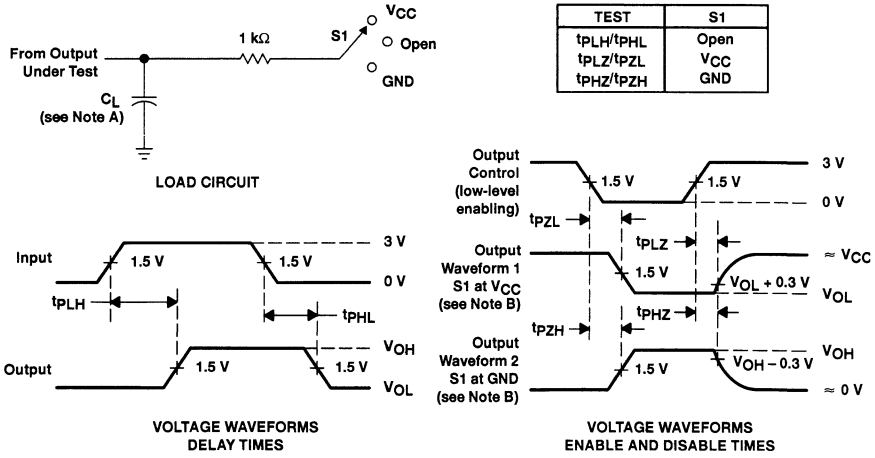
PARAMETER		SN74AHCT540		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.5		V
$V_{IH(D)}$	High-level dynamic input voltage	2		V
$V_{IL(D)}$	Low-level dynamic input voltage		0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	12	pF

PARAMETER MEASUREMENT INFORMATION

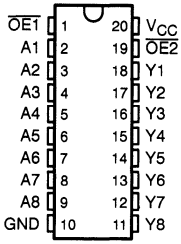


NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

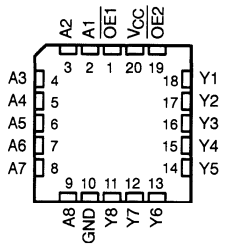
Figure 1. Load Circuit and Voltage Waveforms

- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHC541 . . . J OR W PACKAGE
SN74AHC541 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC541 . . . FK PACKAGE
(TOP VIEW)



description

The 'AHC541 octal buffers/drivers are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package to facilitate printed-circuit-board layout.

The 3-state control gate is a two-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide noninverted data when they are not in the high-impedance state.

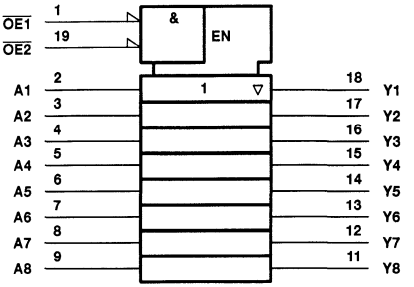
The SN54AHC541 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC541 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer/driver)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

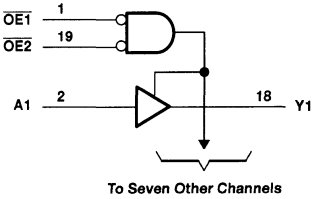
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			SN54AHC541		SN74AHC541		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 ± 0.3 V		–4		–4	mA
		V_{CC} = 5 ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 ± 0.3 V		4		4	mA
		V_{CC} = 5 ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 ± 0.3 V		100		100	ns/V
		V_{CC} = 5 ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC541		SN74AHC541		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
			3 V	2.9	3		2.9		2.9		
			4.5 V	4.4	4.5		4.4		4.4		
		I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
		I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
			3 V			0.1		0.1		0.1	
			4.5 V			0.1		0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	Data inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
	Control inputs					±0.1		±1		±1	
I_{OZ}†		V_O = V_{CC} or GND, V_I ($\overline{OE}$) = V_{IL} or V_{IH}	5.5 V			±0.25		±2.5		±2.5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
C_i		V_I = V_{CC} or GND	5 V		2	10				10	pF
C_o		V_O = V_{CC} or GND	5 V		4						pF

† For input and ouput, I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC541					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A	Y	C_L = 15 pF		5	7	1	8.5	ns
t_{PHL}*					5	7	1	8.5	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		6	10.5	1	11	ns
t_{PZL}*					6	10.5	1	11	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		7	11	1	12	ns
t_{PLZ}*					7	11	1	12	
t_{PLH}	A	Y	C_L = 50 pF		7.5	10.5	1	12	ns
t_{PHL}					7.5	10.5	1	12	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		8	14	1	16	ns
t_{PZL}					8	14	1	16	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		9	15.4	1	17.5	ns
t_{PLZ}					9	15.4	1	17.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC541					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		5	7	1	8.5	ns
t_{PHL}					5	7	1	8.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF		6	10.5	1	11	ns
t_{PZL}					6	10.5	1	11	
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF		7	11	1	12	ns
t_{PLZ}					7	11	1	12	
t_{PLH}	A	Y	C_L = 50 pF		7.5	10.5	1	12	ns
t_{PHL}					7.5	10.5	1	12	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		8	14	1	16	ns
t_{PZL}					8	14	1	16	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		9	15.4	1	17.5	ns
t_{PLZ}					9	15.4	1	17.5	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC541					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A	Y	C_L = 15 pF		3.5	5	1	6	ns
t_{PHL}*					3.5	5	1	6	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		4.7	7.2	1	8.5	ns
t_{PZL}*					4.7	7.2	1	8.5	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		5	7.5	1	8	ns
t_{PLZ}*					5	7.5	1	8	
t_{PLH}	A	Y	C_L = 50 pF		5	7	1	8	ns
t_{PHL}					5	7	1	8	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		6.2	9.2	1	10.5	ns
t_{PZL}					6.2	9.2	1	10.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		6	8.8	1	10	ns
t_{PLZ}					6	8.8	1	10	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC541					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		3.5	5	1	6	ns
t_{PHL}					3.5	5	1	6	
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF		4.7	7.2	1	8.5	ns
t_{PZL}					4.7	7.2	1	8.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF		5	7.5	1	8	ns
t_{PLZ}					5	7.5	1	8	
t_{PLH}	A	Y	C_L = 50 pF		5	7	1	8	ns
t_{PHL}					5	7	1	8	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		6.2	9.2	1	10.5	ns
t_{PZL}					6.2	9.2	1	10.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		6	8.8	1	10	ns
t_{PLZ}					6	8.8	1	10	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN74AHC541				UNIT
				T_A = 25°C		MIN	MAX	
				MIN	MAX			
$t_{sk(o)}$	A	Y	3.3 V ± 0.3 V		1.5		1.5	ns
			5 V ± 0.5 V		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

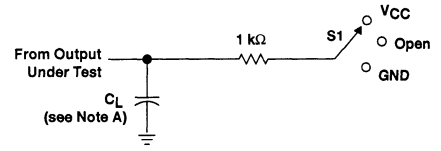
PARAMETER		SN74AHC541		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.7		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

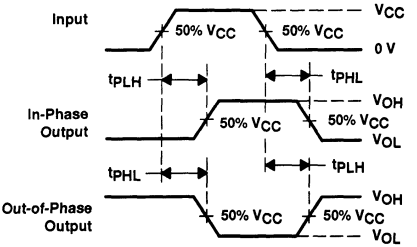
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	12	pF

PARAMETER MEASUREMENT INFORMATION

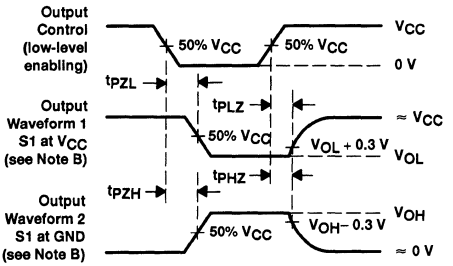


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES



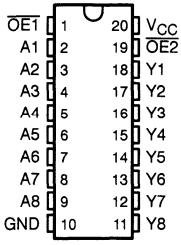
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

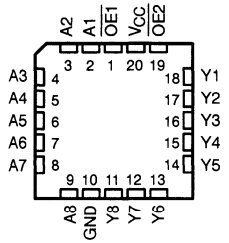
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHCT541 . . . J OR W PACKAGE
SN74AHCT541 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT541 . . . FK PACKAGE
(TOP VIEW)



description

The 'AHCT541 octal buffers/drivers are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package to facilitate printed-circuit-board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide noninverted data when they are not in the high-impedance state.

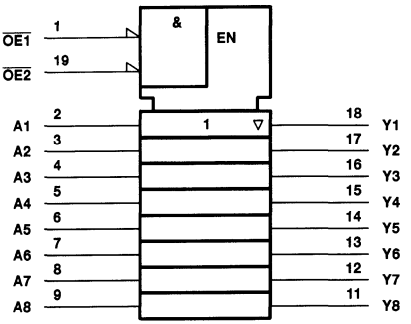
The SN54AHCT541 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT541 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

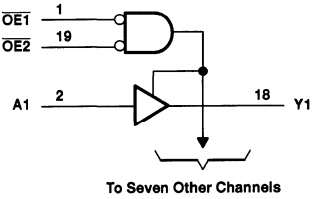
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Note 1)	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	–20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package	0.6 W
DW package	1.6 W
N package	1.3 W
PW package	0.7 W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHCT541		SN74AHCT541		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT541		SN74AHCT541		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		3.15		V
	I_{OH} = –8 mA		2.5			2.4		2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.25		±2.5		±2.5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		40		40	μA
ΔI_{CC}†	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			1.35		1.5		1.5	mA
I_{off}	V_O = 5.5 V	0 V			0.5*				5	μA
C_i	$V_I = V_{CC}$ or GND	5 V		2	10				10	pF
C_o	$V_O = V_{CC}$ or GND	5 V		4						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT541					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A	Y	C_L = 15 pF		4.1	6	1	6.5	ns
t_{PHL}*					3.7	5.5	1	6.5	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		5	7	1	8	ns
t_{PZL}*					5	7	1	8	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		4.5	7	1	8	ns
t_{PLZ}*					4.5	7	1	8	
t_{PLH}	A	Y	C_L = 50 pF		6.2	8.5	1	9.5	ns
t_{PHL}					6	8.5	1	9.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		7.5	10	1	12	ns
t_{PZL}					7.5	10	1	12	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		7	10	1	12	ns
t_{PLZ}					7	10	1	12	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT541					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L = 15 pF		4.1	6	1	6.5	ns
t_{PHL}					3.7	5.5	1	6.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF		5	7	1	8	ns
t_{PZL}					5	7	1	8	
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF		4.5	7	1	8	ns
t_{PLZ}					4.5	7	1	8	
t_{PLH}	A	Y	C_L = 50 pF		6.2	8.5	1	9.5	ns
t_{PHL}					6	8.5	1	9.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		7.5	10	1	12	ns
t_{PZL}					7.5	10	1	12	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		7	10	1	12	ns
t_{PLZ}					7	10	1	12	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN74AHCT541				UNIT
				T_A = 25°C		MIN	MAX	
				MIN	MAX			
$t_{sk(o)}$	A	Y	5 V ± 0.5 V		1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

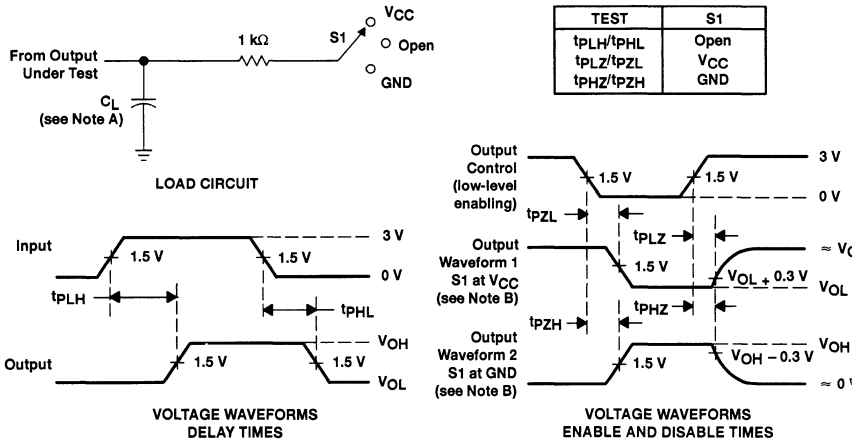
PARAMETER		SN74AHCT541		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.6		V
$V_{IH(D)}$	High-level dynamic input voltage	2		V
$V_{IL(D)}$	Low-level dynamic input voltage		0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	12	pF

PARAMETER MEASUREMENT INFORMATION

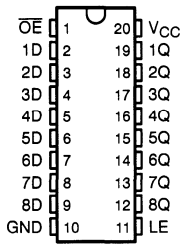


NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

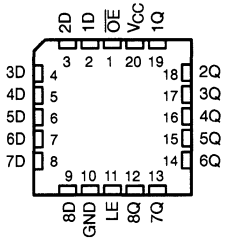
Figure 1. Load Circuit and Voltage Waveforms

- **3-State Outputs Directly Drive Bus Lines**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHC573 . . . J OR W PACKAGE
SN74AHC573 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC573 . . . FK PACKAGE
(TOP VIEW)



description

The 'AHC573 are octal transparent D-type latches.

When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

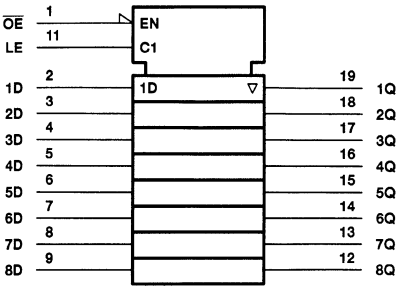
The SN54AHC573 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC573 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

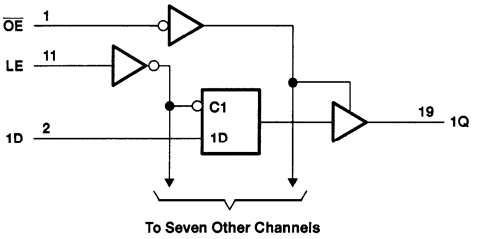
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			SN54AHC573		SN74AHC573		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC573		SN74AHC573		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
	I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND	5.5 V			±0.25		±2.5		±2.5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
C_i	V_I = V_{CC} or GND	5 V		2.5	10				10	pF
C_o	V_O = V_{CC} or GND	5 V		3.5						pF

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54AHC573		SN74AHC573		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	5		5		5		ns
t_{su}	Setup time, data before LE↓	3.5		3.5		3.5		ns
t_h	Hold time, data after LE↓	1.5		1.5		1.5		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54AHC573		SN74AHC573		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	5		5		5		ns
t_{su}	Setup time, data before LE↓	3.5		3.5		3.5		ns
t_h	Hold time, data after LE↓	1.5		1.5		1.5		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC573					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	D	Q	C_L = 15 pF		7	11	1	13	ns
t_{PHL}*					7	11	1	13	
t_{PLH}*	LE	Q	C_L = 15 pF		7.6	11.9	1	14	ns
t_{PHL}*					7.6	11.9	1	14	
t_{PZH}*	$\overline{OE}$	Q	C_L = 15 pF		7.3	11.5	1	13.5	ns
t_{PZL}*					7.3	11.5	1	13.5	
t_{PHZ}*	$\overline{OE}$	Q	C_L = 15 pF		8.3	11	1	13	ns
t_{PLZ}*					8.3	11	1	13	
t_{PLH}	D	Q	C_L = 50 pF		9.5	14.5	1	16.5	ns
t_{PHL}					9.5	14.5	1	16.5	
t_{PLH}	LE	Q	C_L = 50 pF		10.1	15.4	1	17.5	ns
t_{PHL}					10.1	15.4	1	17.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		9.8	15	1	17	ns
t_{PZL}					9.8	15	1	17	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		10.7	14.5	1	16.5	ns
t_{PLZ}					10.7	14.5	1	16.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC573 T_A = 25°C MIN	TYP	MAX	SN74AHC573 MIN	SN74AHC573 MAX	UNIT
t_{PLH}	D	Q	C_L = 15 pF		7	11	1	13	ns
t_{PHL}					7	11	1	13	
t_{PLH}	LE	Q	C_L = 15 pF		7.6	11.9	1	14	ns
t_{PHL}					7.6	11.9	1	14	
t_{PZH}	$\overline{OE}$	Q	C_L = 15 pF		7.3	11.5	1	13.5	ns
t_{PZL}					7.3	11.5	1	13.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 15 pF		8.3	11	1	13	ns
t_{PLZ}					8.3	11	1	13	
t_{PLH}	D	Q	C_L = 50 pF		9.5	14.5	1	16.5	ns
t_{PHL}					9.5	14.5	1	16.5	
t_{PLH}	LE	Q	C_L = 50 pF		10.1	15.4	1	17.5	ns
t_{PHL}					10.1	15.4	1	17.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		9.8	15	1	17	ns
t_{PZL}					9.8	15	1	17	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		10.7	14.5	1	16.5	ns
t_{PLZ}					10.7	14.5	1	16.5	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC573 T_A = 25°C MIN	TYP	MAX	SN54AHC573 MIN	SN54AHC573 MAX	UNIT
t_{PLH}*	D	Q	C_L = 15 pF		4.5	6.8	1	8	ns
t_{PHL}*					4.5	6.8	1	8	
t_{PLH}*	LE	Q	C_L = 15 pF		5	7.7	1	9	ns
t_{PHL}*					5	7.7	1	9	
t_{PZH}*	$\overline{OE}$	Q	C_L = 15 pF		5.2	7.7	1	9	ns
t_{PZL}*					5.2	7.7	1	9	
t_{PHZ}*	$\overline{OE}$	Q	C_L = 15 pF		5.2	7.7	1	9	ns
t_{PLZ}*					5.2	7.7	1	9	
t_{PLH}	D	Q	C_L = 50 pF		6	8.8	1	10	ns
t_{PHL}					6	8.8	1	10	
t_{PLH}	LE	Q	C_L = 50 pF		6.5	9.7	1	11	ns
t_{PHL}					6.5	9.7	1	11	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		6.7	9.7	1	11	ns
t_{PZL}					6.7	9.7	1	11	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		6.7	9.7	1	11	ns
t_{PLZ}					6.7	9.7	1	11	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC573					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	D	Q	C_L = 15 pF		4.5	6.8	1	8	ns
t_{PHL}					4.5	6.8	1	8	
t_{PLH}	LE	Q	C_L = 15 pF		5	7.7	1	9	ns
t_{PHL}					5	7.7	1	9	
t_{PZH}	$\overline{OE}$	Q	C_L = 15 pF		5.2	7.7	1	9	ns
t_{PZL}					5.2	7.7	1	9	
t_{PHZ}	$\overline{OE}$	Q	C_L = 15 pF		5.2	7.7	1	9	ns
t_{PLZ}					5.2	7.7	1	9	
t_{PLH}	D	Q	C_L = 50 pF		6	8.8	1	10	ns
t_{PHL}					6	8.8	1	10	
t_{PLH}	LE	Q	C_L = 50 pF		6.5	9.7	1	11	ns
t_{PHL}					6.5	9.7	1	11	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		6.7	9.7	1	11	ns
t_{PZL}					6.7	9.7	1	11	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		6.7	9.7	1	11	ns
t_{PLZ}					6.7	9.7	1	11	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHC573				UNIT
			T_A = 25°C		MIN	MAX	
			MIN	MAX			
$t_{sk(o)}$	Output skew	3.3 V ± 0.3 V		1.5		1.5	ns
		5 V ± 0.5 V		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

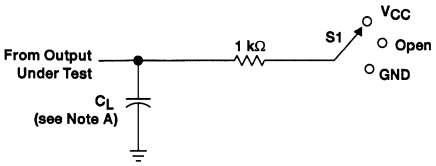
PARAMETER		SN74AHC573		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		1	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

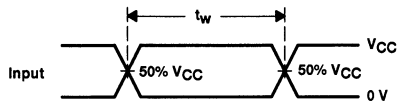
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	16	pF

PARAMETER MEASUREMENT INFORMATION

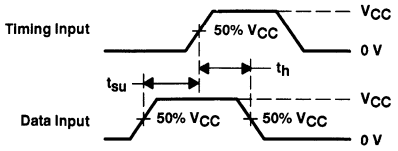


LOAD CIRCUIT

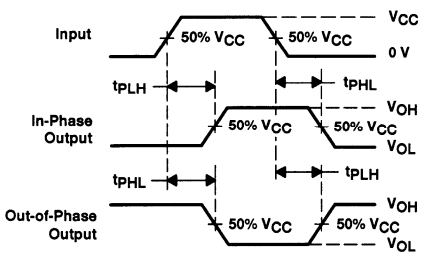
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



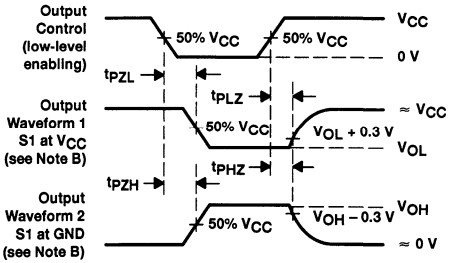
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
DELAY TIMES



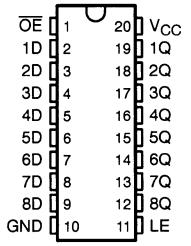
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

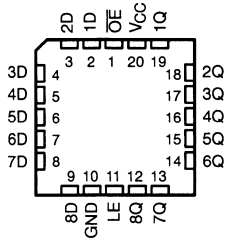
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHCT573 . . . J OR W PACKAGE
SN74AHCT573 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT573 . . . FK PACKAGE
(TOP VIEW)



description

The 'AHCT573 are octal-transparent D-type latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AHCT573 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT573 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

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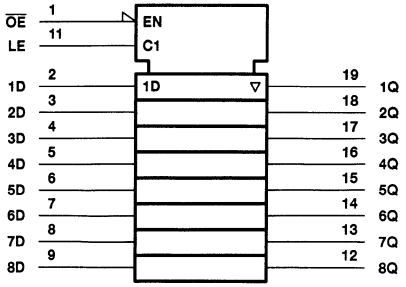
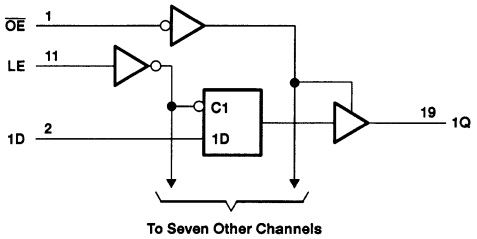


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHCT573		SN74AHCT573		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT573		SN74AHCT573		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		3.15		V
	I_{OH} = –8 mA		2.5			2.4		2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.25		±2.5		±2.5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		40		40	μA
ΔI_{CC}†	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			1.35		1.5		1.5	mA
I_{off}	V_O = 5.5 V	0 V			0.5*				5	μA
C_i	$V_I = V_{CC}$ or GND	5 V		2.5	10				10	pF
C_o	$V_O = V_{CC}$ or GND	5 V		3						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54AHCT573		SN74AHCT573		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	5		5		5		ns
t_{su}	Setup time, data before LE↓	3.5		3.5		3.5		ns
t_h	Hold time, data after LE↓	1.5		1.5		1.5		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT573					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	D	Q	C_L = 15 pF		4.2	6	1	6.5	ns
t_{PHL}*					5.1	7	1	9	
t_{PLH}*	LE	Q	C_L = 15 pF		4.7	6.5	1	7.5	ns
t_{PHL}*					5.6	7.5	1	9	
t_{PZH}*	$\overline{OE}$	Q	C_L = 15 pF		4.1	6.5	1	7	ns
t_{PZL}*					5.5	7.5	1	10	
t_{PHZ}*	$\overline{OE}$	Q	C_L = 15 pF		5.5	8	1	11	ns
t_{PLZ}*					5.4	8	1	9.5	
t_{PLH}	D	Q	C_L = 50 pF		5.2	7	1	7.5	ns
t_{PHL}					6.1	8	1	10	
t_{PLH}	LE	Q	C_L = 50 pF		5.7	7.5	1	8.5	ns
t_{PHL}					6.6	8.5	1	10	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		5.1	7.5	1	8	ns
t_{PZL}					6.5	8.5	1	11	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		6.7	9	1	12	ns
t_{PLZ}					6.4	9	1	10.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT573					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	D	Q	C_L = 15 pF		4.2	6	1	6.5	ns
t_{PHL}					5.1	7	1	9	
t_{PLH}	LE	Q	C_L = 15 pF		4.7	6.5	1	7.5	ns
t_{PHL}					5.6	7.5	1	9	
t_{PZH}	$\overline{OE}$	Q	C_L = 15 pF		4.1	6.5	1	7	ns
t_{PZL}					5.5	7.5	1	10	
t_{PHZ}	$\overline{OE}$	Q	C_L = 15 pF		5.5	8	1	11	ns
t_{PLZ}					5.4	8	1	9.5	
t_{PLH}	D	Q	C_L = 50 pF		5.2	7	1	7.5	ns
t_{PHL}					6.1	8	1	10	
t_{PLH}	LE	Q	C_L = 50 pF		5.7	7.5	1	8.5	ns
t_{PHL}					6.6	8.5	1	10	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		5.1	7.5	1	8	ns
t_{PZL}					6.5	8.5	1	11	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		6.7	9	1	12	ns
t_{PLZ}					6.4	9	1	10.5	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHCT573				UNIT
			T_A = 25°C		MIN	MAX	
			MIN	MAX			
$t_{sk(o)}$	Output skew	5 V ± 0.5 V		1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

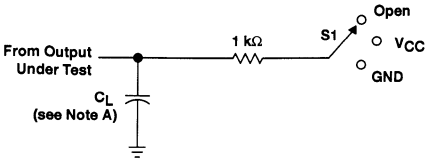
PARAMETER		SN74AHCT573		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		1.1	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.7	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	3.7		V
$V_{IH(D)}$	High-level dynamic input voltage	2		V
$V_{IL(D)}$	Low-level dynamic input voltage		0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

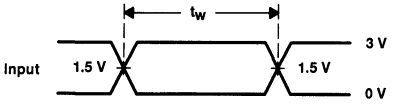
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	16	pF

PARAMETER MEASUREMENT INFORMATION

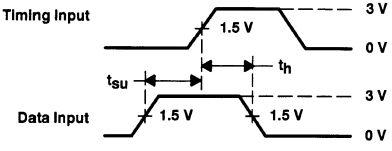


LOAD CIRCUIT

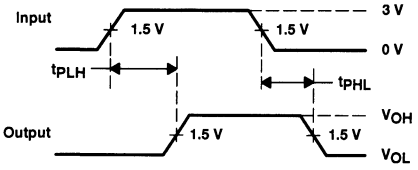
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



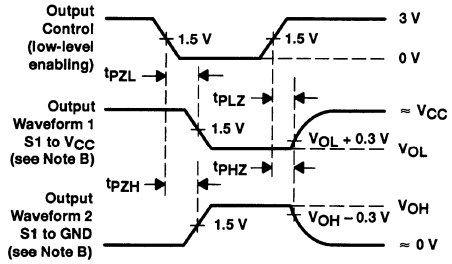
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

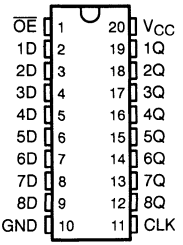
Figure 1. Load Circuit and Voltage Waveforms

SN54AHC574, SN74AHC574
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

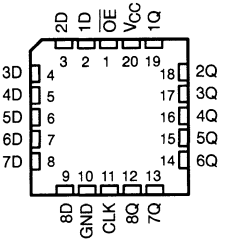
SCLS244B – OCTOBER 1995 – REVISED APRIL 1996

- **Operating Range 2-V to 5.5-V V_{CC}**
- **3-State Outputs Directly Drive Bus Lines**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHC574 . . . J OR W PACKAGE
SN74AHC574 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC574 . . . FK PACKAGE
(TOP VIEW)



description

The 'AHC574 are octal edge-triggered D-type flip-flops that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AHC574 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC574 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

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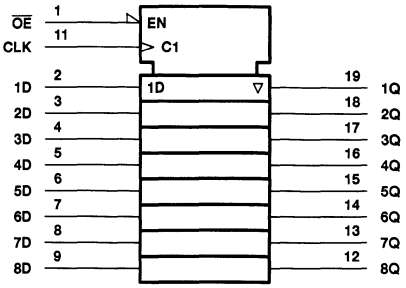
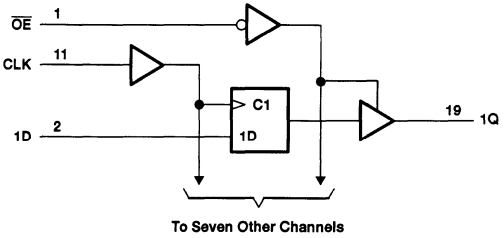
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			SN54AHC574		SN74AHC574		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC574		SN74AHC574		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
	I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.25		±2.5		±2.5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
C_i	V_I = V_{CC} or GND	5 V		3	10				10	pF
C_o	V_O = V_{CC} or GND	5 V		3						pF

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54AHC574		SN74AHC574		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, CLK high or low	5		5		5		ns
t_{su}	Setup time, data before CLK↑	3.5		3.5		3.5		ns
t_h	Hold time, data after CLK↑	1.5		1.5		1.5		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54AHC574		SN74AHC574		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, CLK high or low	5		5		5		ns
t_{su}	Setup time, data before CLK↑	3		3		3		ns
t_h	Hold time, data after CLK↑	1.5		1.5		1.5		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC574					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	80	125		65		MHz
			C_L = 50 pF	50	75		45		
t_{PLH}*	CLK	Q	C_L = 15 pF		8.5	13.2	1	15.5	ns
t_{PHL}*					8.5	13.2	1	15.5	
t_{PZH}*	$\overline{OE}$	Q	C_L = 15 pF		8.2	12.8	1	15	ns
t_{PZL}*					8.2	12.8	1	15	
t_{PHZ}*	$\overline{OE}$	Q	C_L = 15 pF		8.5	13	1	15	ns
t_{PLZ}*					8.5	13	1	15	
t_{PLH}	CLK	Q	C_L = 50 pF		11	16.7	1	19	ns
t_{PHL}					11	16.7	1	19	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		10.7	16.3	1	18.5	ns
t_{PZL}					10.7	16.3	1	18.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		11	15	1	17	ns
t_{PLZ}					11	15	1	17	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC574					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	80	125		65		MHz
			C_L = 50 pF	50	75		45		
t_{PLH}	CLK	Q	C_L = 15 pF		8.5	13.2	1	15.5	ns
t_{PHL}					8.5	13.2	1	15.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 15 pF		8.2	12.8	1	15	ns
t_{PZL}					8.2	12.8	1	15	
t_{PHZ}	$\overline{OE}$	Q	C_L = 15 pF		8.5	13	1	15	ns
t_{PLZ}					8.5	13	1	15	
t_{PLH}	CLK	Q	C_L = 50 pF		11	16.7	1	19	ns
t_{PHL}					11	16.7	1	19	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		10.7	16.3	1	18.5	ns
t_{PZL}					10.7	16.3	1	18.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		11	15	1	17	ns
t_{PLZ}					11	15	1	17	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC574					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	130	180		110		MHz
			C_L = 50 pF	85	115		75		
t_{PLH}*	CLK	Q	C_L = 15 pF		5.6	8.6	1	10	ns
t_{PHL}*					5.6	8.6	1	10	
t_{PZH}*	$\overline{OE}$	Q	C_L = 15 pF		5.9	9	1	10.5	ns
t_{PZL}*					5.9	9	1	10.5	
t_{PHZ}*	$\overline{OE}$	Q	C_L = 15 pF		5.5	9	1	10.5	ns
t_{PLZ}*					5.5	9	1	10.5	
t_{PLH}	CLK	Q	C_L = 50 pF		7.1	10.6	1	12	ns
t_{PHL}					7.1	10.6	1	12	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		7.4	11	1	12.5	ns
t_{PZL}					7.4	11	1	12.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		7.1	10.1	1	11.5	ns
t_{PLZ}					7.1	10.1	1	11.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC574					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	130	180		110		MHz
			C_L = 50 pF	85	115		75		
t_{PLH}	CLK	Q	C_L = 15 pF		5.6	8.6	1	10	ns
t_{PHL}					5.6	8.6	1	10	
t_{PZH}	$\overline{OE}$	Q	C_L = 15 pF		5.9	9	1	10.5	ns
t_{PZL}					5.9	9	1	10.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 15 pF		5.5	9	1	10.5	ns
t_{PLZ}					5.5	9	1	10.5	
t_{PLH}	CLK	Q	C_L = 50 pF		7.1	10.6	1	12	ns
t_{PHL}					7.1	10.6	1	12	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		7.4	11	1	12.5	ns
t_{PZL}					7.4	11	1	12.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		7.1	10.1	1	11.5	ns
t_{PLZ}					7.1	10.1	1	11.5	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHC574				UNIT
			T_A = 25°C		MIN	MAX	
			MIN	MAX			
$t_{sk(o)}$	Output skew	3.3 V ± 0.3 V		1.5		1.5	ns
		5 V ± 0.5 V		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

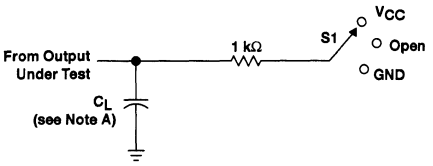
PARAMETER		SN74AHC574		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.2		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

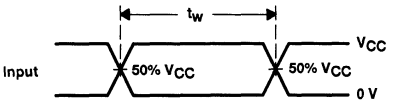
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	28	pF

PARAMETER MEASUREMENT INFORMATION

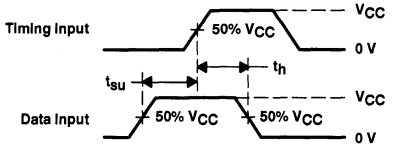


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

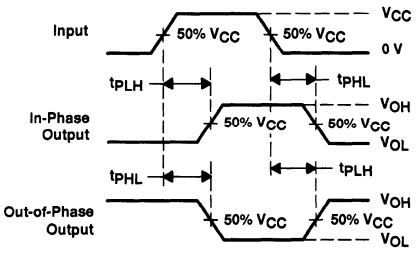
LOAD CIRCUIT



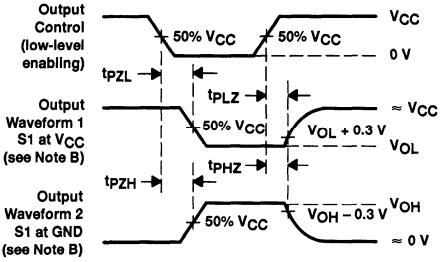
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
DELAY TIMES



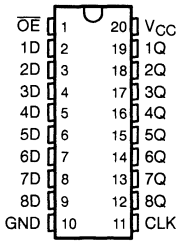
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

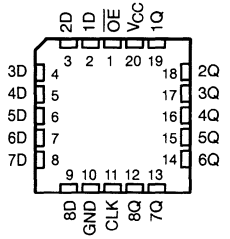
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHCT574 . . . J OR W PACKAGE
SN74AHCT574 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT574 . . . FK PACKAGE
(TOP VIEW)



description

The 'AHCT574 are octal edge-triggered D-type flip-flops that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input places the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

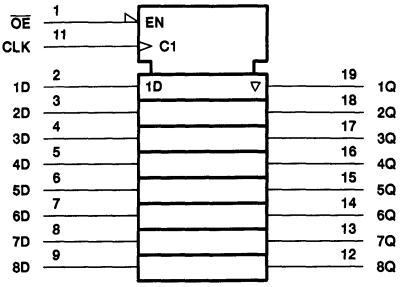
The SN54AHCT574 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT574 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L or H	X	Q_0
H	X	X	Z

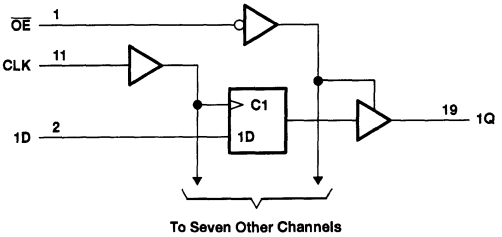
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±75 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHCT574		SN74AHCT574		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT574		SN74AHCT574		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		3.15		V
	I_{OH} = –8 mA		2.5			2.4		2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.25		±2.5		±2.5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		40		40	μA
ΔI_{CC}†	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			1.35		1.5		1.5	mA
I_{off}	V_O = 5.5 V	0 V			0.5*				5	μA
C_i	$V_I = V_{CC}$ or GND	5 V		3	10				10	pF
C_o	$V_O = V_{CC}$ or GND	5 V		3						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54AHCT574		SN74AHCT574		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, CLK high or low	5		5.5		5.5		ns
t_{su}	Setup time, data before CLK↑	3		3.5		3.5		ns
t_h	Hold time, data after CLK↑	1.5		1.5		1.5		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHCT574					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	130	180		110		MHz
			C_L = 50 pF	85	115		75		
t_{PLH}*	CLK	Q	C_L = 15 pF		5.5	8.6	1	10	ns
t_{PHL}*					5.5	8.6	1	10	
t_{PZH}*	$\overline{OE}$	Q	C_L = 15 pF		5	9	1	10.5	ns
t_{PZL}*					5	9	1	10.5	
t_{PHZ}*	$\overline{OE}$	Q	C_L = 15 pF		5.5	9	1	10.5	ns
t_{PLZ}*					5.5	9	1	10.5	
t_{PLH}	CLK	Q	C_L = 50 pF		7	10.6	1	12	ns
t_{PHL}					7	10.6	1	12	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		6	11	1	12.5	ns
t_{PZL}					6	11	1	12.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		7	10.1	1	11.5	ns
t_{PLZ}					7	10.1	1	11.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHCT574					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			C_L = 15 pF	130	180		110		MHz
			C_L = 50 pF	85	115		75		
t_{PLH}	CLK	Q	C_L = 15 pF		5.5	8.6	1	10	ns
t_{PHL}					5.5	8.6	1	10	
t_{PZH}	$\overline{OE}$	Q	C_L = 15 pF		5	9	1	10.5	ns
t_{PZL}					5	9	1	10.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 15 pF		5.5	9	1	10.5	ns
t_{PLZ}					5.5	9	1	10.5	
t_{PLH}	CLK	Q	C_L = 50 pF		7	10.6	1	12	ns
t_{PHL}					7	10.6	1	12	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		6	11	1	12.5	ns
t_{PZL}					6	11	1	12.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		7	10.1	1	11.5	ns
t_{PLZ}					7	10.1	1	11.5	

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHCT574		UNIT
			T_A = 25°C	MIN MAX	
			MIN MAX		
$t_{sk(o)}$	Output skew	5 V ± 0.5 V	1	1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

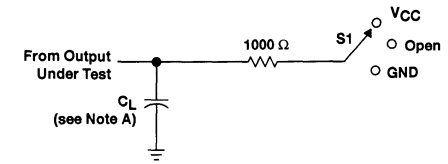
PARAMETER		SN74AHCT574		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	3.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2		V
$V_{IL(D)}$	Low-level dynamic input voltage		0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

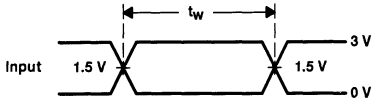
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	28	pF

PARAMETER MEASUREMENT INFORMATION

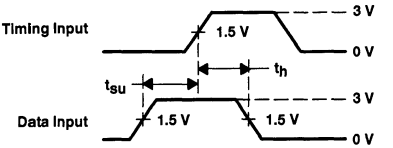


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

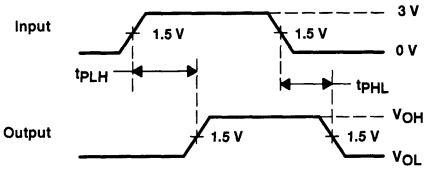
LOAD CIRCUIT



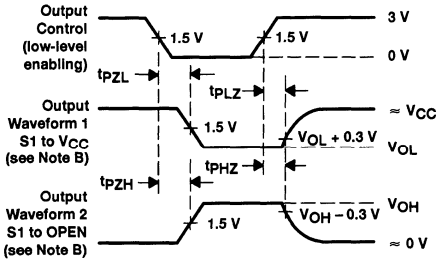
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

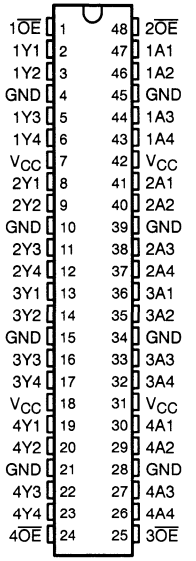
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

Contents

- **Members of the Texas Instruments *Widebus*™ Family**
- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Package and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54AHC16240 . . . WD PACKAGE
SN74AHC16240 . . . DL PACKAGE
(TOP VIEW)



description

The 'AHC16240 are 16-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide inverting outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

The SN74AHC16240 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54AHC16240 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC16240 is characterized for operation from –40°C to 85°C.

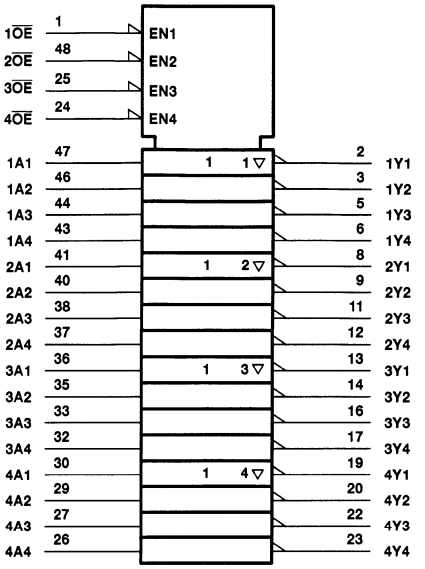
FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

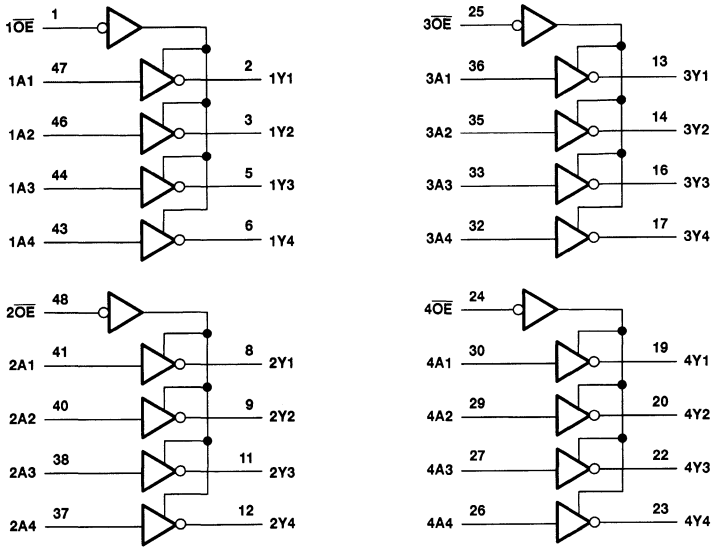
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through each V_{CC} or GND ..... ±75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DL package ..... 1.2 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

			SN54AHC16240		SN74AHC16240		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 ± 0.3 V		–4		–4	mA
		V_{CC} = 5 ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 ± 0.3 V		4		4	mA
		V_{CC} = 5 ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 ± 0.3 V		100		100	ns/V
		V_{CC} = 5 ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC16240		SN74AHC16240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
			3 V	2.9	3		2.9		2.9		
			4.5 V	4.4	4.5		4.4		4.4		
		I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
		I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
			3 V			0.1		0.1		0.1	
			4.5 V			0.1		0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	Data inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
	Control inputs					±0.1		±1		±1	
I_{OZ}†		V_O = V_{CC} or GND, V_I ($\overline{OE}$) = V_{IL} or V_{IH}	5.5 V			±0.25		±2.5		±2.5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
C_i		V_I = V_{CC} or GND	5 V		2.5	10				10	pF
C_o		V_O = V_{CC} or GND	5 V		3.5						pF

† The parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHC16240		SN74AHC16240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}*	A	Y	C_L = 15 pF		5.3	7.5	1	9	1	9	ns
t_{PHL}*					5.3	7.5	1	9	1	9	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		6.6	10.6	1	12.5	1	12.5	ns
t_{PZL}*					6.6	10.6	1	12.5	1	12.5	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		7.8	11.5	1	12.5	1	12.5	ns
t_{PLZ}*					7.8	11.5	1	12.5	1	12.5	
t_{PLH}	A	Y	C_L = 50 pF		7.8	11	1	12.5	1	12.5	ns
t_{PHL}					7.8	11	1	12.5	1	12.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		9.1	14.1	1	16	1	16	ns
t_{PZL}					9.1	14.1	1	16	1	16	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		10.3	14	1	16	1	16	ns
t_{PLZ}					10.3	14	1	16	1	16	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHC16240		SN74AHC16240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}*	A	Y	C_L = 15 pF		3.6	5.5	1	6.5	1	6.5	ns
t_{PHL}*					3.6	5.5	1	6.5	1	6.5	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		4.7	7.3	1	8.5	1	8.5	ns
t_{PZL}*					4.7	7.3	1	8.5	1	8.5	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		5.2	7.2	1	8.5	1	8.5	ns
t_{PLZ}*					5.2	7.2	1	8.5	1	8.5	
t_{PLH}	A	Y	C_L = 50 pF		5.1	7.5	1	8.5	1	8.5	ns
t_{PHL}					5.1	7.5	1	8.5	1	8.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		6.2	9.3	1	10.5	1	10.5	ns
t_{PZL}					6.2	9.3	1	10.5	1	10.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		6.7	9.2	1	10.5	1	10.5	ns
t_{PLZ}					6.7	9.2	1	10.5	1	10.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHC16240				UNIT
			T_A = 25°C		MIN	MAX	
			MIN	MAX			
$t_{sk(o)}$	Output skew	3.3 V ± 0.3 V		1.5		1.5	ns
		5 V ± 0.5 V		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

PRODUCT PREVIEW

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER		SN74AHC16240			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.6		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.6		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.6		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

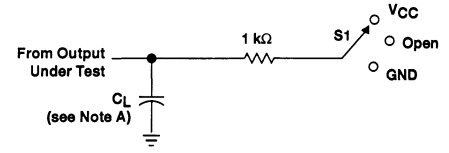
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	10	pF

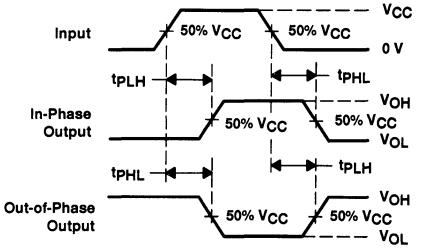
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

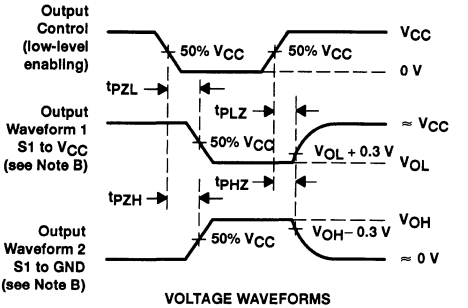


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
DELAY TIMES



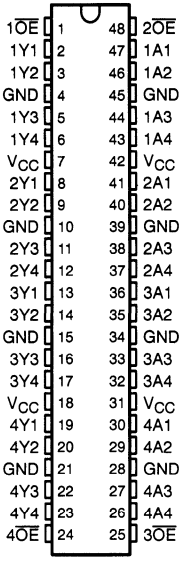
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Package and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54AHCT16240 . . . WD PACKAGE
SN74AHCT16240 . . . DL PACKAGE
(TOP VIEW)



description

The 'AHCT16240 are 16-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide inverting outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

The SN74AHCT16240 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54AHCT16240 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT16240 is characterized for operation from –40°C to 85°C.

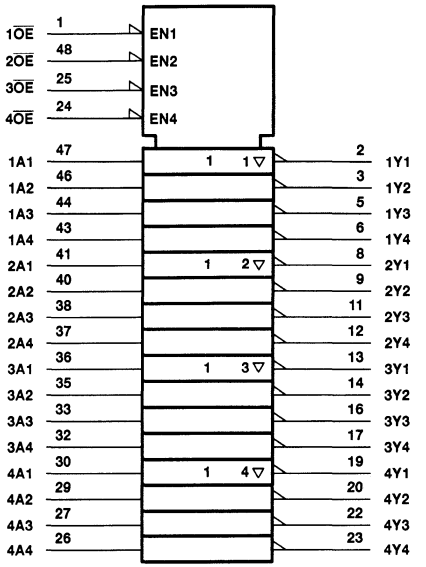
FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

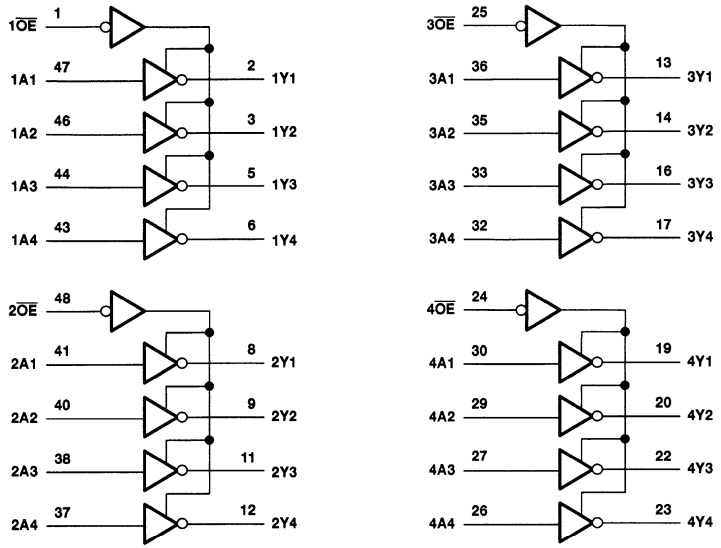
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through each V_{CC} or GND ..... ±75 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DL package ..... 1.2 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

		SN54AHCT16240		SN74AHCT16240		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT16240		SN74AHCT16240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		3.15		V
	I_{OH} = –8 mA		2.5			2.4		2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V		0.001	0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.25		±2.5		±2.5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		40		40	μA
ΔI_{CC}†	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			1.35		1.5		1.5	μA
I_{off}	V_O = 5.5 V	0 V			0.5*				5	μA
C_i	$V_I = V_{CC}$ or GND	5 V		2.5	10				10	pF
C_o	$V_O = V_{CC}$ or GND	5 V		3						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHCT16240		SN74AHCT16240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}*	A	Y	C_L = 15 pF		5.4	7.4	1	8.5	1	8.5	ns
t_{PHL}*					5.4	7.4	1	8.5	1	8.5	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		7.7	10.4	1	12	1	12	ns
t_{PZL}*					7.7	10.4	1	12	1	12	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		8.3	10.4	1	12	1	12	ns
t_{PLZ}*					8.3	10.4	1	12	1	12	
t_{PLH}	A	Y	C_L = 50 pF		5.9	8.4	1	9.5	1	9.5	ns
t_{PHL}					5.9	8.4	1	9.5	1	9.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		8.2	11.4	1	13	1	13	ns
t_{PZL}					8.2	11.4	1	13	1	13	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		8.8	11.4	1	13	1	13	ns
t_{PLZ}					8.8	11.4	1	13	1	13	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHCT16240				UNIT
			T_A = 25°C		MIN	MAX	
			MIN	MAX			
$t_{sk(o)}$	Output skew	5 V ± 0.5 V		1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER		SN74AHCT16240			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.6		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.6		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.1		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

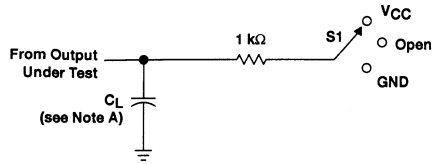
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	10	pF

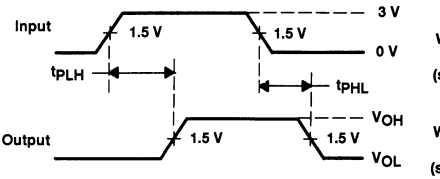
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

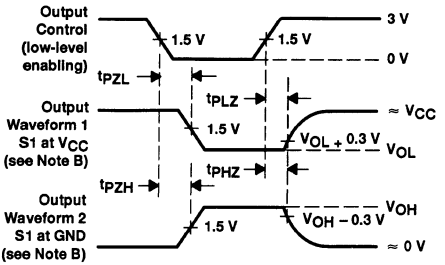


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
DELAY TIMES



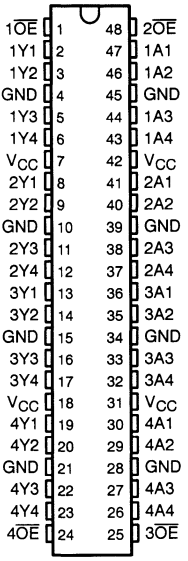
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54AHC16244 . . . WD PACKAGE
SN74AHC16244 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'AHC16244 are 16-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

The SN74AHC16244 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54AHC16244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC16244 is characterized for operation from –40°C to 85°C.

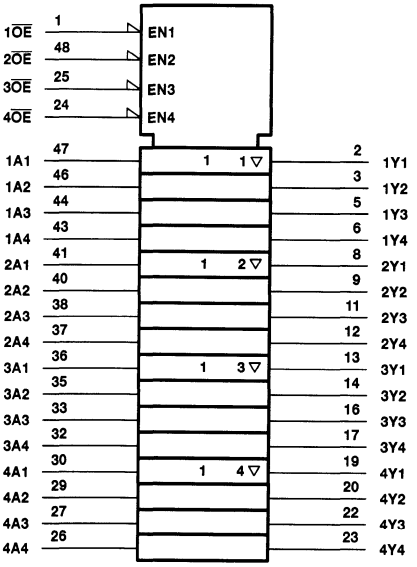
FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

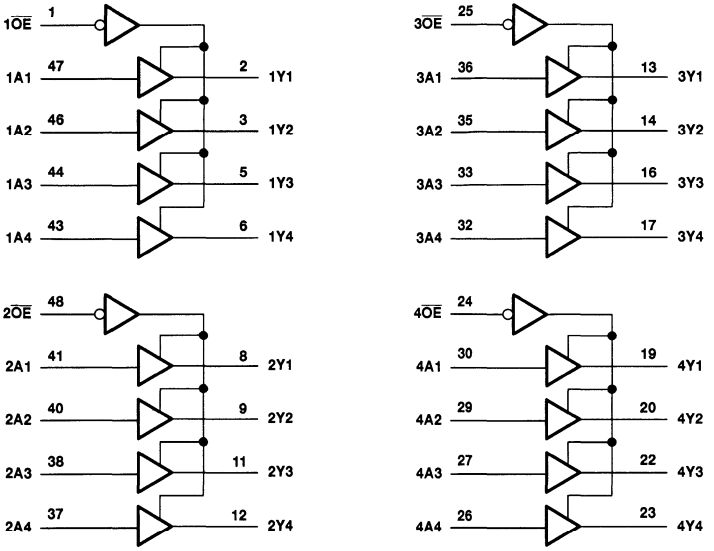
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through each V_{CC} or GND ..... ±75 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

			SN54AHC16244		SN74AHC16244		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 ± 0.3 V		–4		–4	mA
		V_{CC} = 5 ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 ± 0.3 V		4		4	mA
		V_{CC} = 5 ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 ± 0.3 V		100		100	ns/V
		V_{CC} = 5 ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC16244		SN74AHC16244		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
			3 V	2.9	3		2.9		2.9		
			4.5 V	4.4	4.5		4.4		4.4		
		I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
		I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
			3 V			0.1		0.1		0.1	
			4.5 V			0.1		0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	Data inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
	Control inputs					±0.1		±1		±1	
I_{OZ}		V_O = V_{CC} or GND, V_I ($\overline{OE}$) = V_{IL} or V_{IH}	5.5 V			±0.25		±2.5		±2.5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
C_i		V_I = V_{CC} or GND	5 V		2	10				10	pF
C_o		V_O = V_{CC} or GND	5 V		3.5						pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHC16244		SN74AHC16244		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}*	A	Y	C_L = 15 pF		5.8	8.4	1	10	1	10	ns
t_{PHL}*					5.8	8.4	1	10	1	10	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		6.6	10.6	1	12.5	1	12.5	ns
t_{PZL}*					6.6	10.6	1	12.5	1	12.5	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		5	9.7	1	11	1	11	ns
t_{PLZ}*					5	9.7	1	11	1	11	
t_{PLH}	A	Y	C_L = 50 pF		8.3	11.9	1	13.5	1	13.5	ns
t_{PHL}					8.3	11.9	1	13.5	1	13.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		9.1	14.1	1	16	1	16	ns
t_{PZL}					9.1	14.1	1	16	1	16	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		10.3	14	1	16	1	16	ns
t_{PLZ}					10.3	14	1	16	1	16	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHC16244		SN74AHC16244		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}*	A	Y	C_L = 15 pF		3.9	5.5	1	6.5	1	6.5	ns
t_{PHL}*					3.9	5.5	1	6.5	1	6.5	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		4.7	7.3	1	8.5	1	8.5	ns
t_{PZL}*					4.7	7.3	1	8.5	1	8.5	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		5	7.2	1	8.5	1	8.5	ns
t_{PLZ}*					5	7.2	1	8.5	1	8.5	
t_{PLH}	A	Y	C_L = 50 pF		5.4	7.5	1	8.5	1	8.5	ns
t_{PHL}					5.4	7.5	1	8.5	1	8.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		6.2	9.3	1	10.5	1	10.5	ns
t_{PZL}					6.2	9.3	1	10.5	1	10.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		6.7	9.2	1	10.5	1	10.5	ns
t_{PLZ}					6.7	9.2	1	10.5	1	10.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHC16244				UNIT
			T_A = 25°C		MIN	MAX	
			MIN	MAX			
$t_{sk(o)}$	Output skew	3.3 V ± 0.3 V		1.5		1.5	ns
		5 V ± 0.5 V		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER		SN74AHC16244			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.2		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.8		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

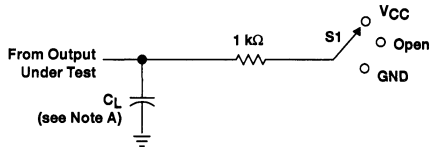
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	8.6	pF

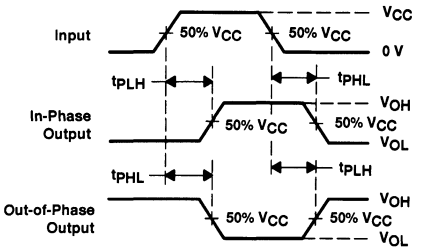
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

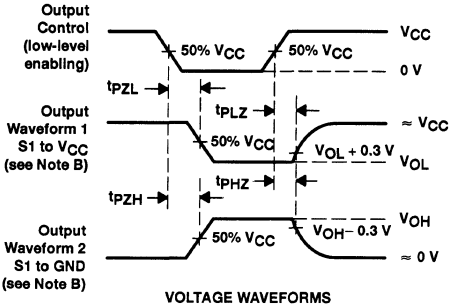


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
DELAY TIMES



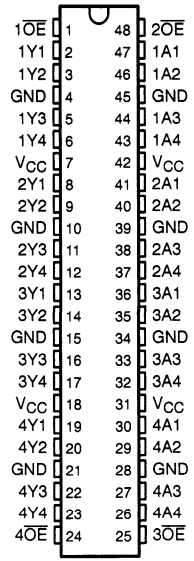
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54AHCT16244 . . . WD PACKAGE
SN74AHCT16244 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'AHCT16244 are 16-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

The SN74AHCT16244 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54AHCT16244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT16244 is characterized for operation from –40°C to 85°C.

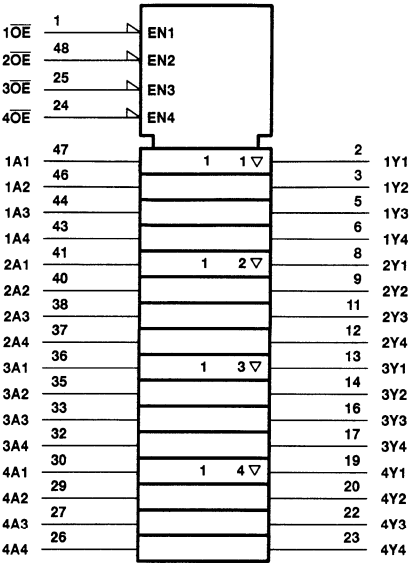
FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

PRODUCT PREVIEW

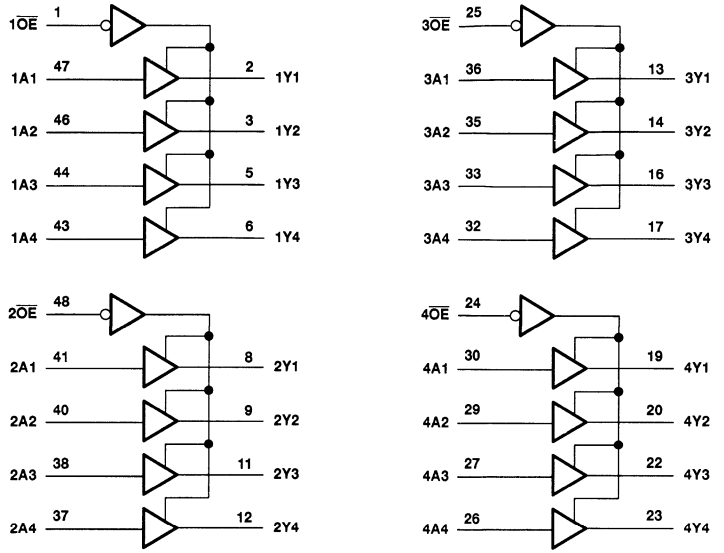
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Note 1)	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	–20 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±25 mA
Continuous current through each V_{CC} or GND	±75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package	0.85 W
DL package	1.2 W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

		SN54AHCT16244		SN74AHCT16244		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT16244		SN74AHCT16244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		3.15		V
	I_{OH} = –8 mA		2.5			2.4		2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.25		±2.5		±2.5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		40		40	μA
ΔI_{CC}†	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			1.35		1.5		1.5	mA
I_{off}	V_O = 5.5 V	0 V			0.5*				5	μA
C_i	$V_I = V_{CC}$ or GND	5 V		2.5	10				10	pF
C_o	$V_O = V_{CC}$ or GND	5 V		3						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHCT16244		SN74AHCT16244		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}*	A	Y	C_L = 15 pF		5.4	7.4	1	8.5	1	8.5	ns
t_{PHL}*					5.4	7.4	1	8.5	1	8.5	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		7.7	10.4	1	12	1	12	ns
t_{PZL}*					7.7	10.4	1	12	1	12	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		5	9.4	1	10	1	10	ns
t_{PLZ}*					5	9.4	1	10	1	10	
t_{PLH}	A	Y	C_L = 50 pF		5.9	8.4	1	9.5	1	9.5	ns
t_{PHL}					5.9	8.4	1	9.5	1	9.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		8.2	11.4	1	13	1	13	ns
t_{PZL}					8.2	11.4	1	13	1	13	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		8.8	11.4	1	13	1	13	ns
t_{PLZ}					8.8	11.4	1	13	1	13	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHCT16244				UNIT
			T_A = 25°C		MIN	MAX	
			MIN	MAX			
$t_{sk(o)}$	Output skew	5 V ± 0.5 V		1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER		SN74AHCT16244			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.7		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.7		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.1		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

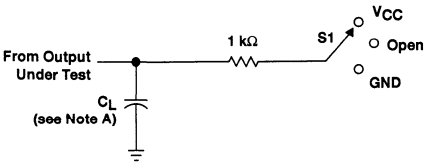
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	8.2	pF

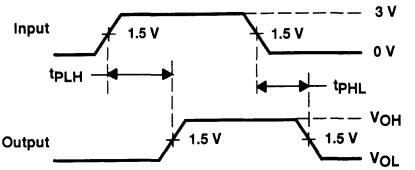
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

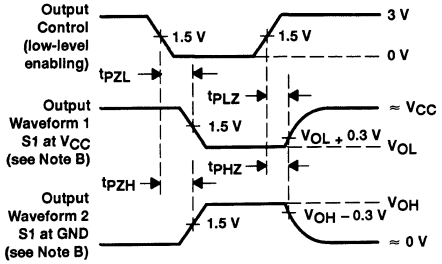


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
DELAY TIMES



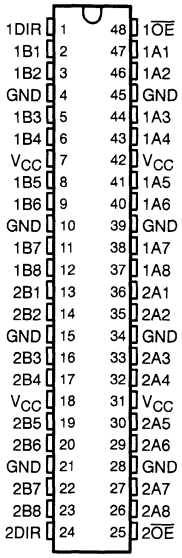
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54AHC16245 . . . WD PACKAGE
SN74AHC16245 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'AHC16245 are 16-bit (dual-octal) noninverting 3-state transceivers designed for synchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

The SN74AHC16245 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54AHC16245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC16245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

PRODUCT PREVIEW

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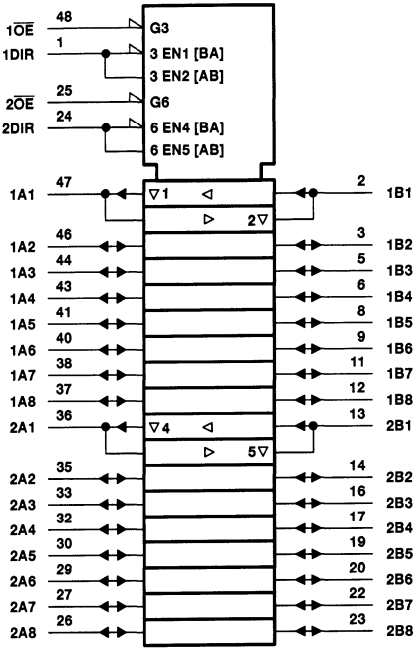
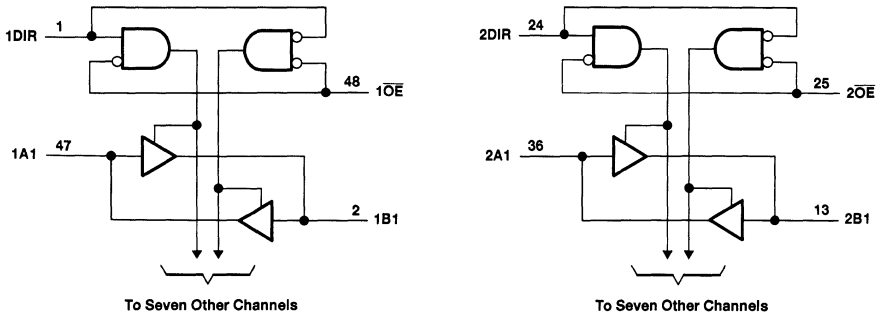
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through each V_{CC} or GND ..... ±75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

PRODUCT PREVIEW

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

			SN54AHC16245		SN74AHC16245		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 ± 0.3 V		–4		–4	mA
		V_{CC} = 5 ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 ± 0.3 V		4		4	mA
		V_{CC} = 5 ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 ± 0.3 V		100		100	ns/V
		V_{CC} = 5 ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC16245		SN74AHC16245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
			3 V	2.9	3		2.9		2.9		
			4.5 V	4.4	4.5		4.4		4.4		
		I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
		I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
			3 V			0.1		0.1		0.1	
			4.5 V			0.1		0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	A or B inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
	$\overline{OE}$ or DIR					±0.1		±1		±1	
I_{OZ}†		$V_O = V_{CC}$ or GND, V_I ($\overline{OE}$) = V_{IL} or V_{IH}	5.5 V			±0.25		±2.5		±2.5	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		40		40	μA
C_i	$\overline{OE}$ or DIR	$V_I = V_{CC}$ or GND	5 V		2.5	10				10	pF
C_{io}	A or B inputs	$V_I = V_{CC}$ or GND	5 V		4						pF

† The parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHC16245		SN74AHC16245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}*	A or B	B or A	C_L = 15 pF		5.8	8.4	1	10	1	10	ns
t_{PHL}*					5.8	8.4	1	10	1	10	
t_{PZH}*	$\overline{OE}$	A or B	C_L = 15 pF		8.5	13.2	1	15.5	1	15.5	ns
t_{PZL}*					8.5	13.2	1	15.5	1	15.5	
t_{PHZ}*	$\overline{OE}$	A or B	C_L = 15 pF		8.9	12.5	1	15.5	1	15.5	ns
t_{PLZ}*					8.9	12.5	1	15.5	1	15.5	
t_{PLH}	A or B	B or A	C_L = 50 pF		8.3	11.9	1	13.5	1	13.5	ns
t_{PHL}					8.3	11.9	1	13.5	1	13.5	
t_{PZH}	$\overline{OE}$	A or B	C_L = 50 pF		11	16.7	1	19	1	19	ns
t_{PZL}					11	16.7	1	19	1	19	
t_{PHZ}	$\overline{OE}$	A or B	C_L = 50 pF		11.5	15.8	1	18	1	18	ns
t_{PLZ}					11.5	15.8	1	18	1	18	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHC16245		SN74AHC16245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}*	A or B	B or A	C_L = 15 pF		4	5.5	1	6.5	1	6.5	ns
t_{PHL}*					4	5.5	1	6.5	1	6.5	
t_{PZH}*	$\overline{OE}$	A or B	C_L = 15 pF		5.8	8.5	1	10	1	10	ns
t_{PZL}*					5.8	8.5	1	10	1	10	
t_{PHZ}*	$\overline{OE}$	A or B	C_L = 15 pF		5.6	7.8	1	9.2	1	9.2	ns
t_{PLZ}*					5.6	7.8	1	9.2	1	9.2	
t_{PLH}	A or B	B or A	C_L = 50 pF		5.5	7.5	1	8.5	1	8.5	ns
t_{PHL}					5.5	7.5	1	8.5	1	8.5	
t_{PZH}	$\overline{OE}$	A or B	C_L = 50 pF		7.3	10.6	1	12	1	12	ns
t_{PZL}					7.3	10.6	1	12	1	12	
t_{PHZ}	$\overline{OE}$	A or B	C_L = 50 pF		7	9.7	1	11	1	11	ns
t_{PLZ}					7	9.7	1	11	1	11	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHC16245				UNIT
			T_A = 25°C		MIN	MAX	
			MIN	MAX			
$t_{sk(o)}$	Output skew	3.3 V ± 0.3 V		1.5		1.5	ns
		5 V ± 0.5 V		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

PRODUCT PREVIEW

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

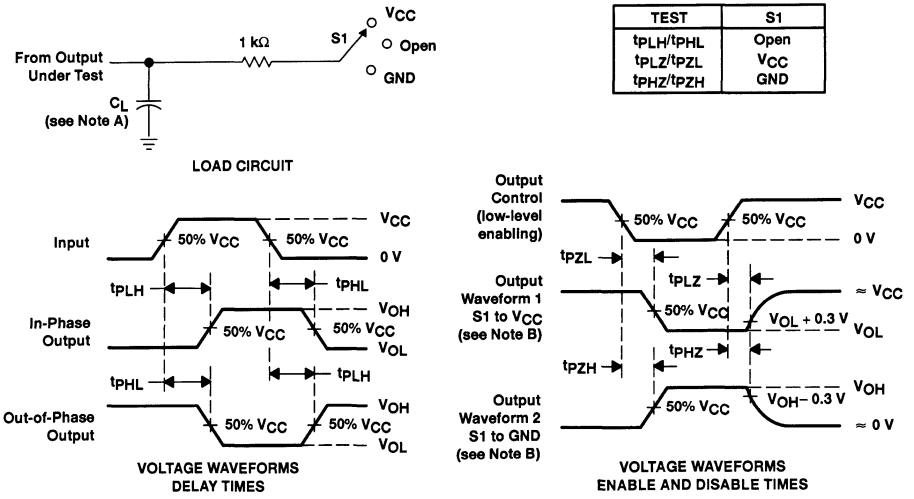
PARAMETER		SN74AHC16245			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.9		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.9		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.3		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	No load, f = 1 MHz	14	pF

PARAMETER MEASUREMENT INFORMATION

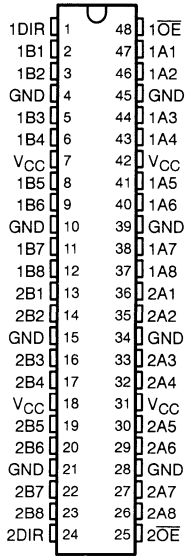


NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54AHCT16245 . . . WD PACKAGE
SN74AHCT16245 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'AHCT16245 are 16-bit (dual-octal) noninverting 3-state transceivers designed for synchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

The SN74AHCT16245 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54AHCT16245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT16245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

PRODUCT PREVIEW

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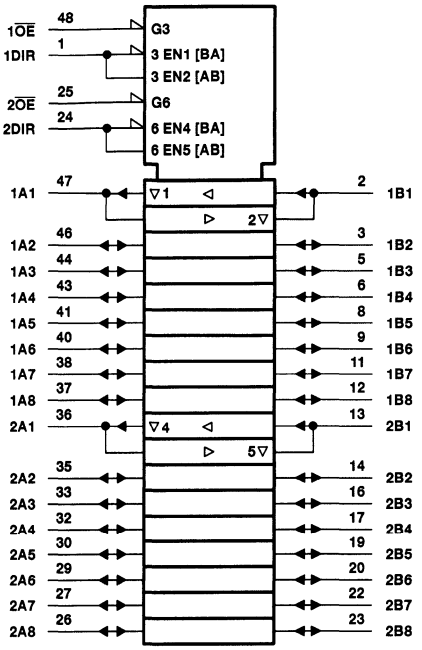
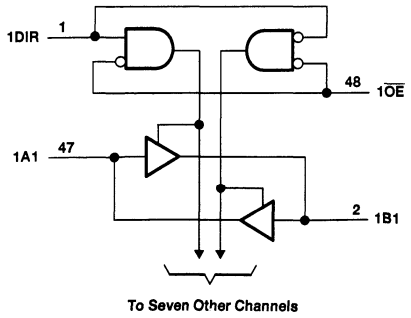
PRODUCT PREVIEW

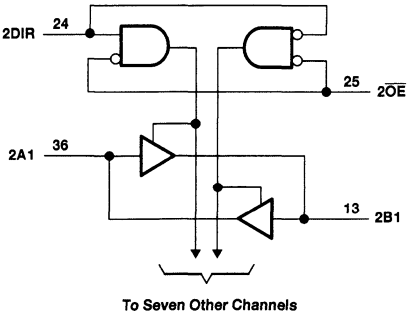
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through each V_{CC} or GND ..... ±75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

		SN54AHCT16245		SN74AHCT16245		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IO}	Input/output voltage, A or B pins	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT16245		SN74AHCT16245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		3.15		V
		I_{OH} = –8 mA		2.5			2.4		2.4		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		I_{OL} = 8 mA				0.36		0.44		0.44	
I_{OZ}†	A or B inputs	V_O = V_{CC} or GND	5.5 V			±0.25		±2.5		±2.5	μA
I_I	$\overline{OE}$ or DIR	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
ΔI_{CC}‡		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
I_{off}		V_O = 5.5 V	0 V			0.5*				5	μA
C_i	$\overline{OE}$ or DIR	V_I = V_{CC} or GND	5 V		2.5	10				10	pF
C_{io}	A or B inputs	V_I = V_{CC} or GND	5 V		4						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† For I/O ports, the parameter I_{OZ} includes the input leakage current.
‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHCT16245		SN74AHCT16245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}*	A or B	B or A	C_L = 15 pF		4.5	7.7	1	8.5	1	8.5	ns
t_{PHL}*					4.5	7.7	1	8.5	1	8.5	
t_{PZH}*	$\overline{OE}$	A or B	C_L = 15 pF		8.9	13.8	1	15	1	15	ns
t_{PZL}*					8.9	13.8	1	15	1	15	
t_{PHZ}*	$\overline{OE}$	A or B	C_L = 15 pF		9.2	14.4	1	15.5	1	15.5	ns
t_{PLZ}*					9.2	14.4	1	15.5	1	15.5	
t_{PLH}	A or B	B or A	C_L = 50 pF		5.3	8.7	1	9.5	1	9.5	ns
t_{PHL}					5.3	8.7	1	9.5	1	9.5	
t_{PZH}	$\overline{OE}$	A or B	C_L = 50 pF		9.7	14.8	1	16	1	16	ns
t_{PZL}					9.7	14.8	1	16	1	16	
t_{PHZ}	$\overline{OE}$	A or B	C_L = 50 pF		10	15.4	1	16.5	1	16.5	ns
t_{PLZ}					10	15.4	1	16.5	1	16.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHCT16245			UNIT
			T_A = 25°C		MIN	MAX
			MIN	MAX		
$t_{sk(o)}$	Output skew	5 V ± 0.5 V		1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

PRODUCT PREVIEW

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

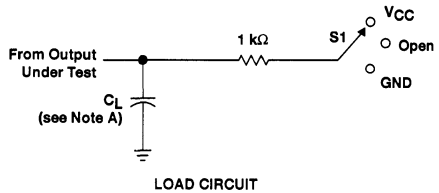
PARAMETER		SN74AHCT16245			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}				V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}				V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

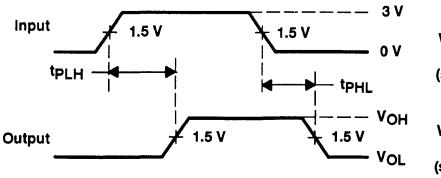
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	No load, f = 1 MHz	13	pF

PARAMETER MEASUREMENT INFORMATION

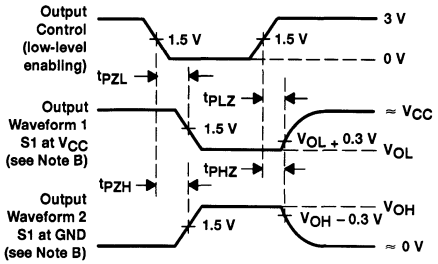


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

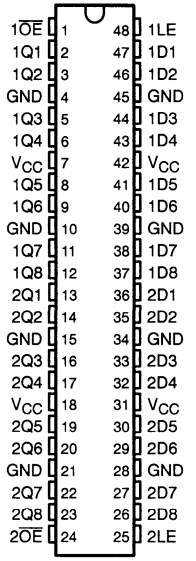
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **Members of the Texas Instruments *Widebus*™ Family**
- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54AHC16373 . . . WD PACKAGE
SN74AHC16373 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'AHC16373 are 16-bit transparent D-type latches with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74AHC16373 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54AHC16373 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC16373 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

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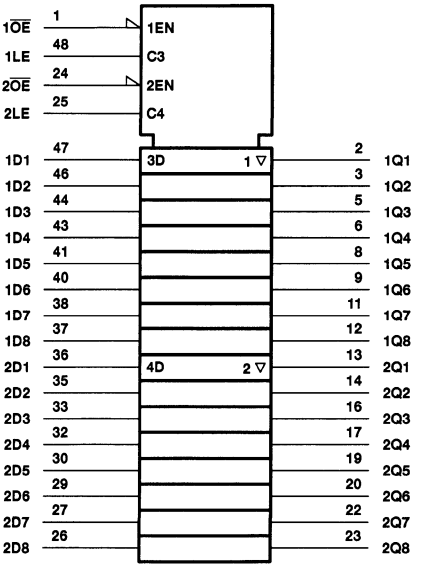
FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

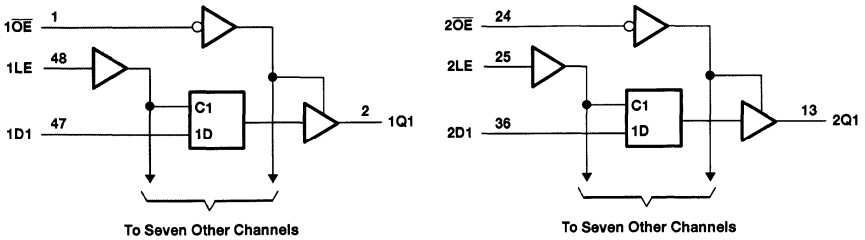
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through each V_{CC} or GND ..... ±75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

			SN54AHC16373		SN74AHC16373		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 ± 0.3 V		–4		–4	mA
		V_{CC} = 5 ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 ± 0.3 V		4		4	mA
		V_{CC} = 5 ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 ± 0.3 V		100		100	ns/V
		V_{CC} = 5 ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC16373		SN74AHC16373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	2 V	1.9			1.9		1.9		V
		3 V	2.9			2.9		2.9		
		4.5 V	4.4			4.4		4.4		
	I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
	I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	V_O = V_{CC} or GND, V_I = V_{IL} or V_{IH}	5.5 V			±0.25		±2.5		±2.5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
C_i	V_I = V_{CC} or GND	5 V		4	10				10	pF
C_o	V_O = V_{CC} or GND	5 V		6						pF

† The parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54AHC16373		SN74AHC16373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, $\overline{LE}$ high	5		5		5		ns
t_{su}	Setup time, data before $\overline{LE}\downarrow$	4		4		4		ns
t_h	Hold time, data after $\overline{LE}\downarrow$	1		1		1		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54AHC16373		SN74AHC16373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, $\overline{LE}$ high	5		5		5		ns
t_{su}	Setup time, data before $\overline{LE}\downarrow$	4		4		4		ns
t_h	Hold time, data after $\overline{LE}\downarrow$	1		1		1		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHC16373		SN74AHC16373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}*	D	Q	C_L = 15 pF		7.3	11.4	1	13.5	1	13.5	ns
t_{PHL}*					7.3	11.4	1	13.5	1	13.5	
t_{PLH}*	LE	Q	C_L = 15 pF		7	11	1	13	1	13	ns
t_{PHL}*					7	11	1	13	1	13	
t_{PZH}*	$\overline{OE}$	Q	C_L = 15 pF		7.3	11.4	1	13.5	1	13.5	ns
t_{PZL}*					7.3	11.4	1	13.5	1	13.5	
t_{PHZ}*	$\overline{OE}$	Q	C_L = 15 pF		7	10	1	12	1	12	ns
t_{PLZ}*					7	10	1	12	1	12	
t_{PLH}	D	Q	C_L = 50 pF		9.8	14.9	1	17	1	17	ns
t_{PHL}					9.8	14.9	1	17	1	17	
t_{PLH}	LE	Q	C_L = 50 pF		9.5	14.5	1	16.5	1	16.5	ns
t_{PHL}					9.5	14.5	1	16.5	1	16.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		9.8	14.9	1	17	1	17	ns
t_{PZL}					9.8	14.9	1	17	1	17	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		9.5	13.2	1	15	1	15	ns
t_{PLZ}					9.5	13.2	1	15	1	15	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHC16373		SN74AHC16373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}*	D	Q	C_L = 15 pF		5	7.2	1	8.5	1	8.5	ns
t_{PHL}*					5	7.2	1	8.5	1	8.5	
t_{PLH}*	LE	Q	C_L = 15 pF		4.9	7.2	1	8.5	1	8.5	ns
t_{PHL}*					4.9	7.2	1	8.5	1	8.5	
t_{PZH}*	$\overline{OE}$	Q	C_L = 15 pF		5.5	8.1	1	9.5	1	9.5	ns
t_{PZL}*					5.5	8.1	1	9.5	1	9.5	
t_{PHZ}*	$\overline{OE}$	Q	C_L = 15 pF		5	7.2	1	8.5	1	8.5	ns
t_{PLZ}*					5	7.2	1	8.5	1	8.5	
t_{PLH}	D	Q	C_L = 50 pF		6.5	9.2	1	10.5	1	10.5	ns
t_{PHL}					6.5	9.2	1	10.5	1	10.5	
t_{PLH}	LE	Q	C_L = 50 pF		6.4	9.2	1	10.5	1	10.5	ns
t_{PHL}					6.4	9.2	1	10.5	1	10.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		7	10.1	1	11.5	1	11.5	ns
t_{PZL}					7	10.1	1	11.5	1	11.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		6.5	9.2	1	10.5	1	10.5	ns
t_{PLZ}					6.5	9.2	1	10.5	1	10.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHC16373		UNIT
			T_A = 25°C		
			MIN	MAX	
$t_{sk(o)}$	Output skew	3.3 V ± 0.3 V		1.5	ns
		5 V ± 0.5 V		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

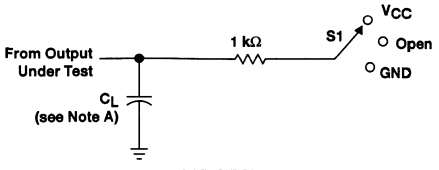
PARAMETER		SN74AHC16373			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.1			V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

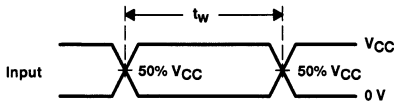
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	18	pF

PARAMETER MEASUREMENT INFORMATION

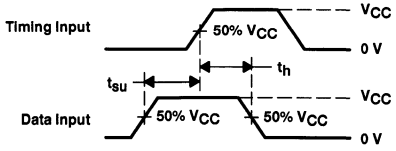


LOAD CIRCUIT

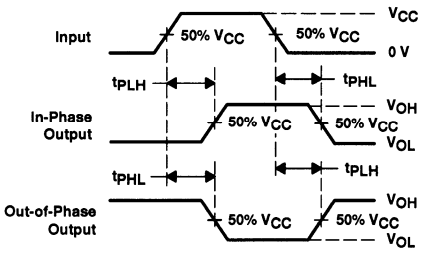
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



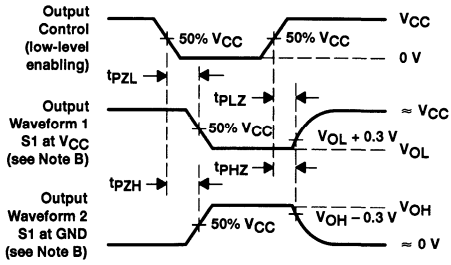
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

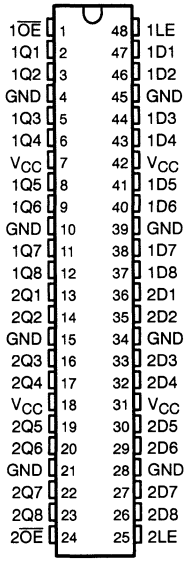
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **Members of the Texas Instruments *Widebus*™ Family**
- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54AHCT16373 . . . WD PACKAGE
SN74AHCT16373 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'AHCT16373 are 16-bit transparent D-type latches with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74AHCT16373 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54AHCT16373 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT16373 is characterized for operation from –40°C to 85°C.

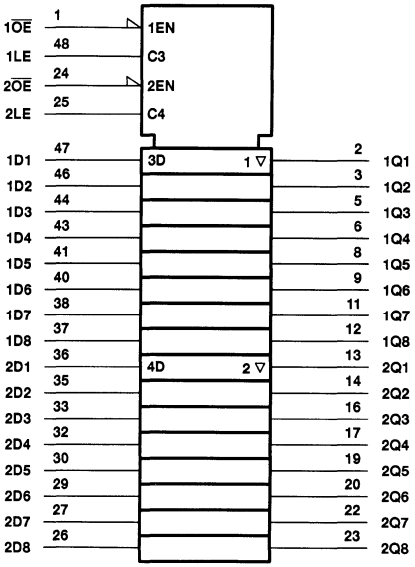
PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE
(each latch)

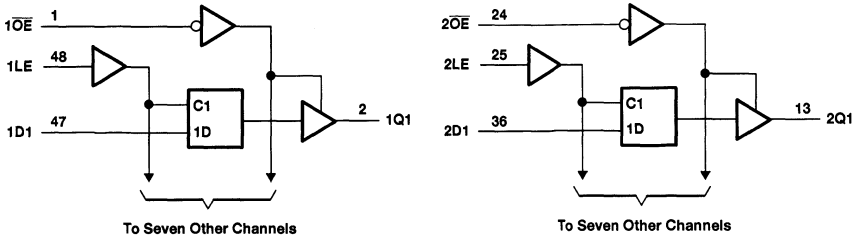
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through each V_{CC} or GND ..... ±75 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

		SN54AHCT16373		SN74AHCT16373		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT16373		SN74AHCT16373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		3.15		V
	I_{OH} = –8 mA		2.5			2.4		2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.25		±2.5		±2.5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		40		40	μA
ΔI_{CC}†	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
I_{off}	V_O = 5.5 V	0 V			0.5*				5	μA
C_i	$V_I = V_{CC}$ or GND	5 V		4						pF
C_o	$V_O = V_{CC}$ or GND	5 V		6						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54AHCT16373		SN74AHCT16373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, $\overline{LE}$ high	6.5		6.5		6.5		ns
t_{su}	Setup time, data before $\overline{LE}\downarrow$	1.5		1.5		1.5		ns
t_h	Hold time, data after $\overline{LE}\downarrow$	3.5		3.5		3.5		ns

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHCT16373		SN74AHCT16373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}*	D	Q	C_L = 15 pF		5.1	8.5	1	9.5	1	9.5	ns
t_{PHL}*					5.1	8.5	1	9.5	1	9.5	
t_{PLH}*	LE	Q	C_L = 15 pF		7.7	12.3	1	13.5	1	13.5	ns
t_{PHL}*					7.7	12.3	1	13.5	1	13.5	
t_{PZH}*	$\overline{OE}$	Q	C_L = 15 pF		6.3	10.9	1	12.5	1	12.5	ns
t_{PZL}*					6.3	10.9	1	12.5	1	12.5	
t_{PHZ}*	$\overline{OE}$	Q	C_L = 15 pF		6	10.2	1	11	1	11	ns
t_{PLZ}*					6	10.2	1	11	1	11	
t_{PLH}	D	Q	C_L = 50 pF		5.9	9.5	1	10.5	1	10.5	ns
t_{PHL}					5.9	9.5	1	10.5	1	10.5	
t_{PLH}	LE	Q	C_L = 50 pF		8.5	13.3	1	14.5	1	14.5	ns
t_{PHL}					8.5	13.3	1	14.5	1	14.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		7.1	11.9	1	13.5	1	13.5	ns
t_{PZL}					7.1	11.9	1	13.5	1	13.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		6.8	11.2	1	12	1	12	ns
t_{PLZ}					6.8	11.2	1	12	1	12	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHCT16373				UNIT
			T_A = 25°C		MIN	MAX	
			MIN	MAX			
$t_{sk(o)}$	Output skew	5 V ± 0.5 V		1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER		SN74AHCT16373			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	1.2	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.8	–1.2	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.1			V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

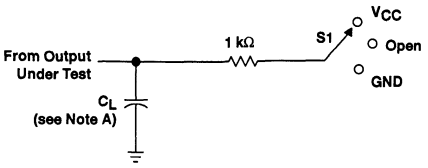
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	17	pF

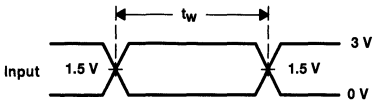
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

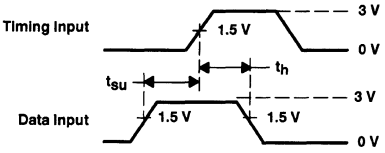


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

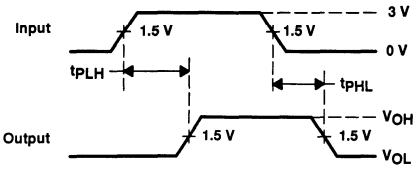
LOAD CIRCUIT



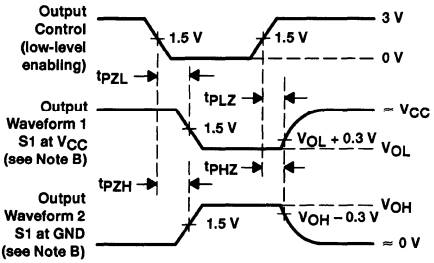
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
DELAY TIMES



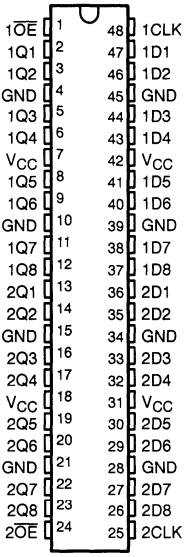
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **Operating Range 2-V to 5.5-V V_{CC}**
- **3-State Outputs Drive Bus Lines Directly**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54AHC16374 . . . WD PACKAGE
SN74AHC16374 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'AHC16374 are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74AHC16374 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54AHC16374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC16374 is characterized for operation from –40°C to 85°C.

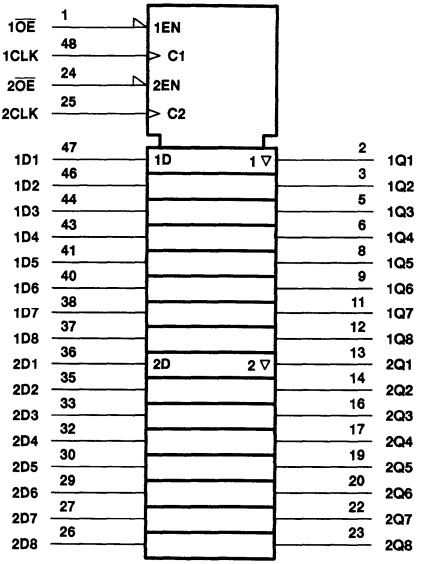
PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

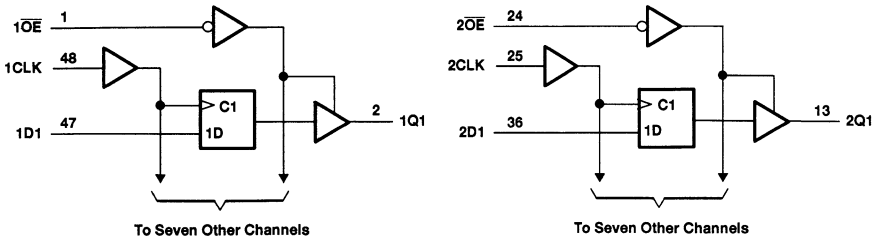
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through each V_{CC} or GND ..... ±75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

			SN54AHC16374		SN74AHC16374		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 ± 0.3 V		–4		–4	mA
		V_{CC} = 5 ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 ± 0.3 V		4		4	mA
		V_{CC} = 5 ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 ± 0.3 V		100		100	ns/V
		V_{CC} = 5 ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC16374		SN74AHC16374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
	I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.25		±2.5		±2.5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
C_i	V_I = V_{CC} or GND	5 V		4	10				10	pF
C_o	V_O = V_{CC} or GND	5 V		6						pF

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54AHC16374		SN74AHC16374		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, CLK high or low	5		5.5		5.5		ns
t_{su}	Setup time, data before CLK↑	4.5		4		4		ns
t_h	Hold time, data after CLK↑	2		2		2		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54AHC16374		SN74AHC16374		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, CLK high or low	5		5		5		ns
t_{su}	Setup time, data before CLK↑	3		3		3		ns
t_h	Hold time, data after CLK↑	2		2		2		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHC16374		SN74AHC16374		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	80	130		70		70		MHz
			C_L = 50 pF	55	85		50		50		
t_{PLH}*	CLK	Q	C_L = 15 pF		8.1	12.7	1	15	1	15	ns
t_{PHL}*					8.1	12.7	1	15	1	15	
t_{PZH}*	$\overline{OE}$	Q	C_L = 15 pF		7.1	11	1	13	1	13	ns
t_{PZL}*					7.1	11	1	13	1	13	
t_{PHZ}*	$\overline{OE}$	Q	C_L = 15 pF		7.5	10.5	1	12.5	1	12.5	ns
t_{PLZ}*					7.5	10.5	1	12.5	1	12.5	
t_{PLH}	CLK	Q	C_L = 50 pF		10.6	16.2	1	18.5	1	18.5	ns
t_{PHL}					10.6	16.2	1	18.5	1	18.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		9.6	14.5	1	16.5	1	16.5	ns
t_{PZL}					9.6	14.5	1	16.5	1	16.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		10.2	14	1	16	1	16	ns
t_{PLZ}					10.2	14	1	16	1	16	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHC16374		SN74AHC16374		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	130	185		110		110		MHz
			C_L = 50 pF	85	120		75		75		
t_{PLH}*	CLK	Q	C_L = 15 pF		5.4	8.1	1	9.5	1	9.5	ns
t_{PHL}*					5.4	8.1	1	9.5	1	9.5	
t_{PZH}*	$\overline{OE}$	Q	C_L = 15 pF		5.1	7.6	1	9	1	9	ns
t_{PZL}*					5.1	7.6	1	9	1	9	
t_{PHZ}*	$\overline{OE}$	Q	C_L = 15 pF		4.6	6.8	1	8	1	8	ns
t_{PLZ}*					4.6	6.8	1	8	1	8	
t_{PLH}	CLK	Q	C_L = 50 pF		6.9	10.1	1	11.5	1	11.5	ns
t_{PHL}					6.9	10.1	1	11.5	1	11.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		6.6	9.6	1	11	1	11	ns
t_{PZL}					6.6	9.6	1	11	1	11	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		6.1	8.8	1	10	1	10	ns
t_{PLZ}					6.1	8.8	1	10	1	10	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHC16374				UNIT
			T_A = 25°C		MIN	MAX	
			MIN	MAX			
$t_{sk(o)}$	Output skew	3.3 V ± 0.3 V		1.5		1.5	ns
		5 V ± 0.5 V		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

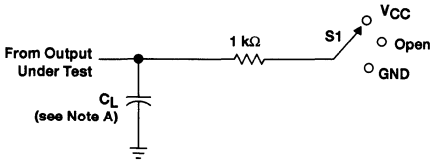
PARAMETER		SN74AHC16374			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5	1	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.5	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4			V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

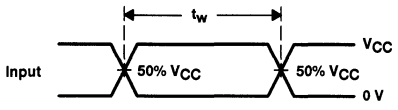
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	32	pF

PARAMETER MEASUREMENT INFORMATION

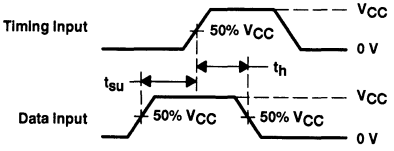


LOAD CIRCUIT

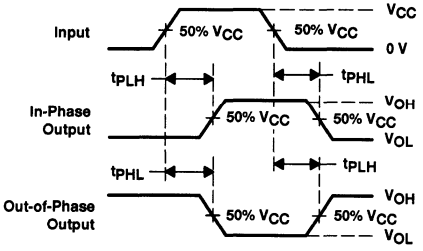
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



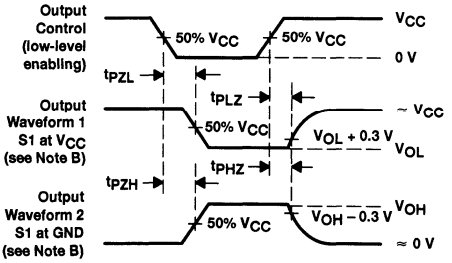
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
DELAY TIMES



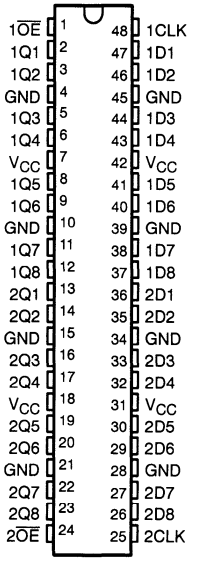
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54AHCT16374 . . . WD PACKAGE
SN74AHCT16374 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'AHCT16374 are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74AHCT16374 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54AHCT16374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT16374 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

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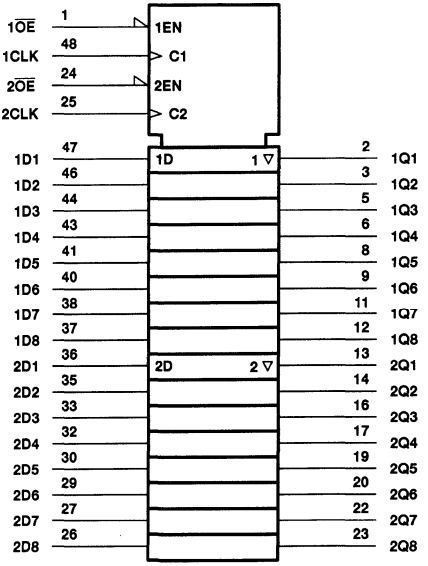
FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

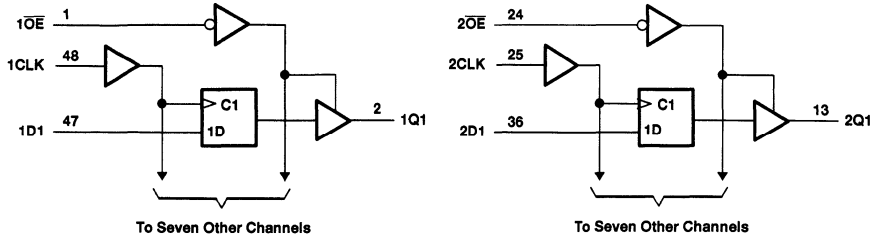
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through each V_{CC} or GND ..... ±75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

PRODUCT PREVIEW

recommended operating conditions (see Note 3)

		SN54AHCT16374		SN74AHCT16374		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT16374		SN74AHCT16374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		3.15		V
	I_{OH} = –8 mA		2.5			2.4		2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_{OZ}	$V_O = V_{CC}$ or GND, $V_I = V_{IH}$ or V_{IL}	5.5 V			±0.25		±2.5		±2.5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		40		40	μA
ΔI_{CC}†	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
I_{off}	V_O = 5.5 V	0 V			0.5*				5	μA
C_i	$V_I = V_{CC}$ or GND	5 V		4	10				10	pF
C_o	$V_O = V_{CC}$ or GND	5 V		6						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54AHCT16374		SN74AHCT16374		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, CLK high or low	6.5		6.5		6.5		ns
t_{su}	Setup time, data before CLK↑	2.5		2.5		2.5		ns
t_h	Hold time, data after CLK↑	2.5		2.5		2.5		ns

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHCT16374		SN74AHCT16374		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	90	140		80		110		MHz
			C_L = 50 pF	85	130		75		75		
t_{PLH}*	CLK	Q	C_L = 15 pF		5.6	9.4	1	10.5	1	10.5	ns
t_{PHL}*					5.6	9.4	1	10.5	1	10.5	
t_{PZH}*	$\overline{OE}$	Q	C_L = 15 pF		6.5	10.2	1	11.5	1	11.5	ns
t_{PZL}*					6.5	10.2	1	11.5	1	11.5	
t_{PHZ}*	$\overline{OE}$	Q	C_L = 15 pF		6.2	10.2	1	11	1	11	ns
t_{PLZ}*					6.2	10.2	1	11	1	11	
t_{PLH}	CLK	Q	C_L = 50 pF		6.4	10.4	1	11.5	1	11.5	ns
t_{PHL}					6.4	10.4	1	11.5	1	11.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		7.3	11.2	1	12.5	1	12.5	ns
t_{PZL}					7.3	11.2	1	12.5	1	12.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		7	11.2	1	12	1	12	ns
t_{PLZ}					7	11.2	1	12	1	12	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER		V_{CC}	SN74AHCT16374			UNIT
			T_A = 25°C		MIN	MAX
			MIN	MAX		
$t_{sk(o)}$	Output skew	5 V ± 0.5 V		1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER		SN74AHCT16374			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	1.2	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.8	–1.2	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	3.8			V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

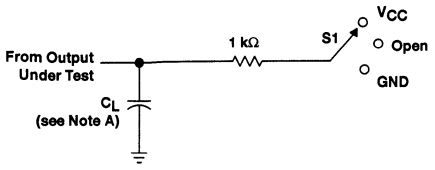
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	27	pF

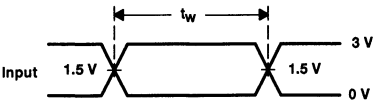
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

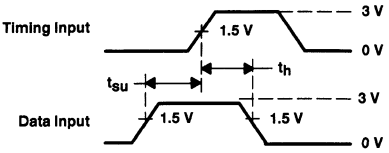


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

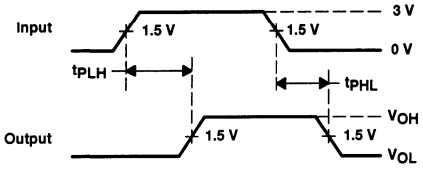
LOAD CIRCUIT



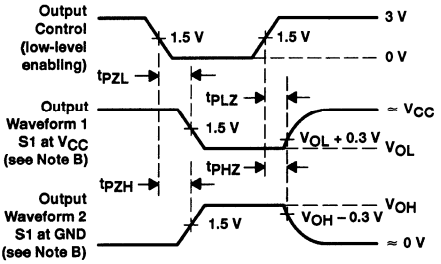
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

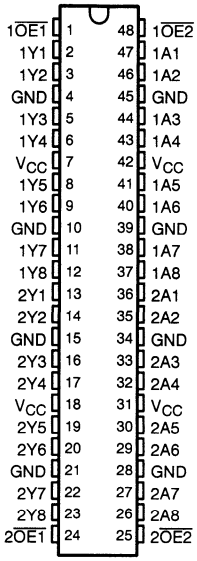
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **Members of the Texas Instruments *Widebus*™ Family**
- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54AHC16540 . . . WD PACKAGE
SN74AHC16540 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

These 16-bit buffers and bus drivers provide a high-performance bus interface for wide data paths.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state.

The SN74AHC16540 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54AHC16540 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC16540 is characterized for operation from –40°C to 85°C.

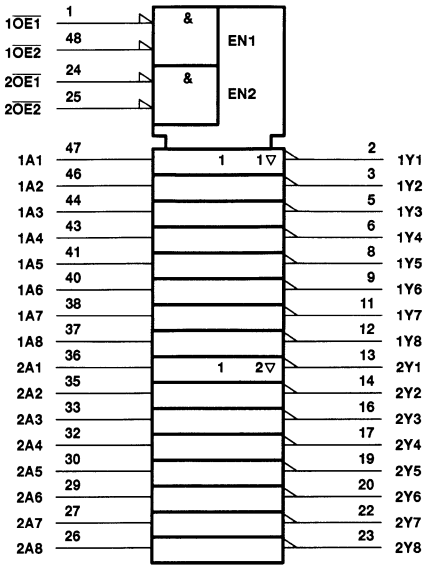
FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

PRODUCT PREVIEW

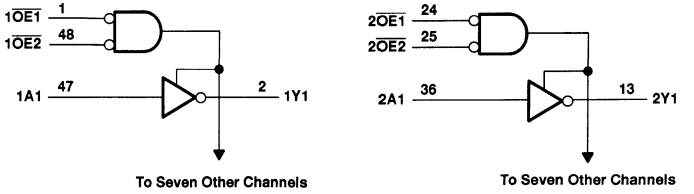
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through each V_{CC} or GND ..... ±75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

			SN54AHC16540		SN74AHC16540		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	µA
		V_{CC} = 3.3 ± 0.3 V		–4		–4	mA
		V_{CC} = 5 ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	µA
		V_{CC} = 3.3 ± 0.3 V		4		4	mA
		V_{CC} = 5 ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 ± 0.3 V		100		100	ns/V
		V_{CC} = 5 ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC16540		SN74AHC16540		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
			3 V	2.9	3		2.9		2.9		
			4.5 V	4.4	4.5		4.4		4.4		
		I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
		I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
			3 V			0.1		0.1		0.1	
			4.5 V			0.1		0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	Data inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
	Control inputs					±0.1		±1		±1	
I_{OZ}†		V_O = V_{CC} or GND, V_I ($\overline{OE}$) = V_{IL} or V_{IH}	5.5 V			±0.25		±2.5		±2.5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
C_i		V_I = V_{CC} or GND	5 V		2	10				10	pF
C_o		V_O = V_{CC} or GND	5 V		4						pF

† The parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHC16540		SN74AHC16540		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}*	A	Y	C_L = 15 pF		4.8	7	1	8.5	1	8.5	ns
t_{PHL}*					4.8	7	1	8.5	1	8.5	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		6.8	10.5	1	12.5	1	12.5	ns
t_{PZL}*					6.8	10.5	1	12.5	1	12.5	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		6.8	10.5	1	12.5	1	12.5	ns
t_{PLZ}*					6.8	10.5	1	12.5	1	12.5	
t_{PLH}	A	Y	C_L = 50 pF		7.3	10.5	1	12	1	12	ns
t_{PHL}					7.3	10.5	1	12	1	12	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		8	14	1	16	1	16	ns
t_{PZL}					8	14	1	16	1	16	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		8	15.4	1	17.5	1	17.5	ns
t_{PLZ}					8	15.4	1	17.5	1	17.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHC16540		SN74AHC16540		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}*	A	Y	C_L = 15 pF		3.7	5	1	6	1	6	ns
t_{PHL}*					3.7	5	1	6	1	6	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		4.7	7.2	1	8.5	1	8.5	ns
t_{PZL}*					4.7	7.2	1	8.5	1	8.5	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		4.5	6.8	1	8	1	8	ns
t_{PLZ}*					4.5	6.8	1	8	1	8	
t_{PLH}	A	Y	C_L = 50 pF		5.2	7	1	8	1	8	ns
t_{PHL}					5.2	7	1	8	1	8	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		6.2	9.2	1	10.5	1	10.5	ns
t_{PZL}					6.2	9.2	1	10.5	1	10.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		6	8.8	1	10	1	10	ns
t_{PLZ}					6	8.8	1	10	1	10	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN74AHC16540				UNIT
				T_A = 25°C		MIN	MAX	
				MIN	MAX			
$t_{sk(o)}$	A	Y	3.3 V ± 0.3 V		1.5		1.5	ns
			5 V ± 0.5 V		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER		SN74AHC16540			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.7			V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

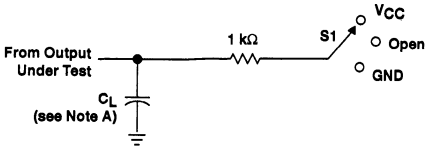
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	12	pF

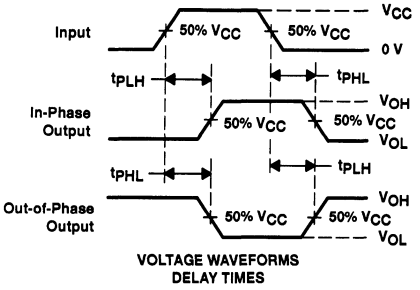
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

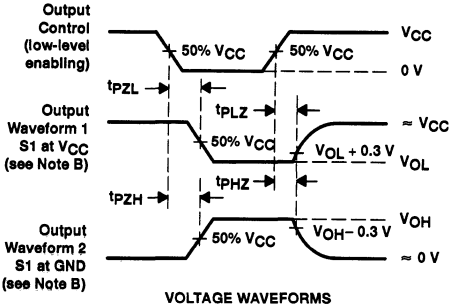


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
DELAY TIMES



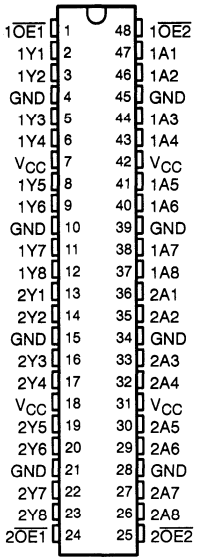
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Members of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54AHCT16540 . . . WD PACKAGE
SN74AHCT16540 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

These 16-bit buffers and bus drivers provide a high-performance bus interface for wide data paths.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state.

The SN74AHCT16540 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54AHCT16540 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT16540 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

PRODUCT PREVIEW

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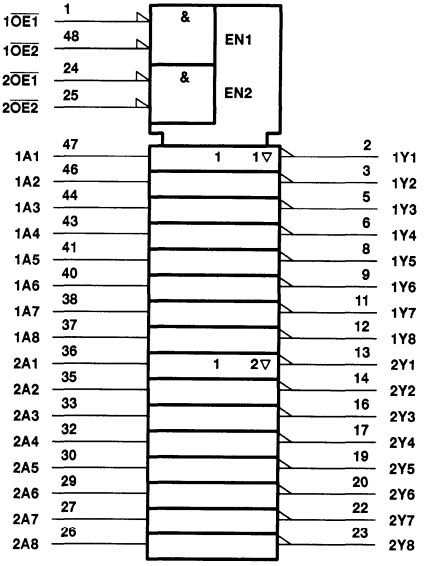
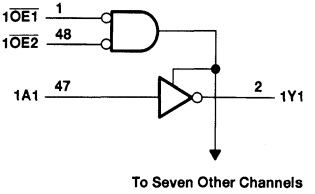
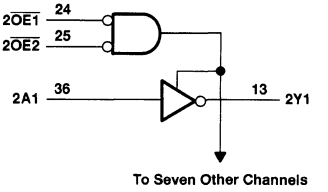
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through each V_{CC} or GND ..... ±75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

		SN54AHCT16540		SN74AHCT16540		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT16540		SN74AHCT16540		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		3.15		V
	I_{OH} = –8 mA		2.5			2.4		2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.25		±2.5		±2.5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
ΔI_{CC}†	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			1.35		1.5		1.5	mA
I_{off}	V_O = 5.5 V	0 V			0.5*				5	μA
C_i	V_I = V_{CC} or GND	5 V		2	10				10	pF
C_o	V_O = V_{CC} or GND	5 V		4						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHCT16540		SN74AHCT16540		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}*	A	Y	C_L = 15 pF		4	6	1	7.5	1	7.5	ns
t_{PHL}*					4	6	1	7.5	1	7.5	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		5.5	8	1	9	1	9	ns
t_{PZL}*					5.5	8	1	9	1	9	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		5	8	1	9	1	9	ns
t_{PLZ}*					5	8	1	9	1	9	
t_{PLH}	A	Y	C_L = 50 pF		6	8.5	1	10	1	10	ns
t_{PHL}					6	8.5	1	10	1	10	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		7.5	11	1	12	1	12	ns
t_{PZL}					7.5	11	1	12	1	12	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		8	11	1	12	1	12	ns
t_{PLZ}					8	11	1	12	1	12	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN74AHCT16540				UNIT
				T_A = 25°C		MIN	MAX	
				MIN	MAX			
$t_{sk(o)}$	A	Y	5 V ± 0.5 V		1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

PRODUCT PREVIEW

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

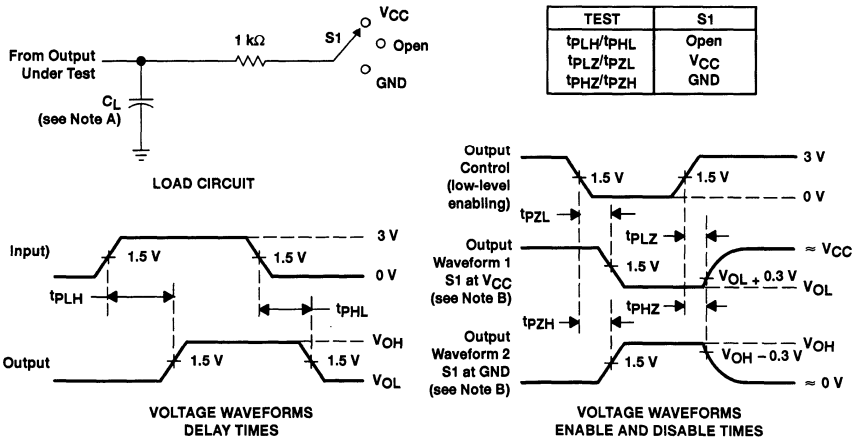
PARAMETER		SN74AHCT16540			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.5			V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	12	pF

PARAMETER MEASUREMENT INFORMATION



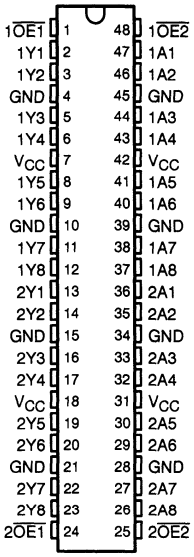
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **Members of the Texas Instruments *Widebus*™ Family**
- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54AHC16541 . . . WD PACKAGE
SN74AHC16541 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'AHC16541 are noninverting 16-bit buffers composed of two 8-bit sections with separate output-enable signals. For either 8-bit buffer section, the two output-enable (1$\overline{OE1}$ and 1$\overline{OE2}$ or 2$\overline{OE1}$ and 2$\overline{OE2}$) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 8-bit buffer section are in the high-impedance state.

The SN74AHC16541 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54AHC16541 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC16541 is characterized for operation from –40°C to 85°C.

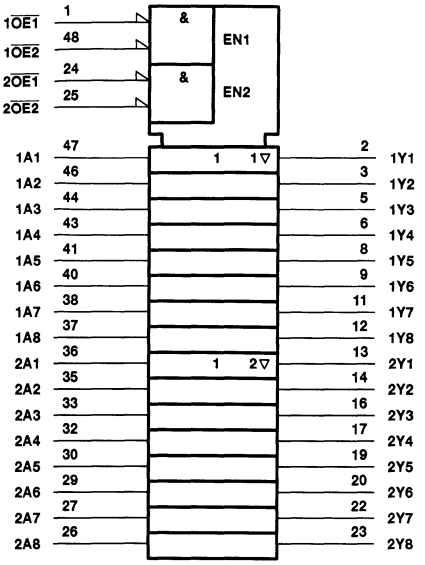
FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

PRODUCT PREVIEW

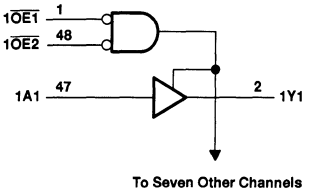
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

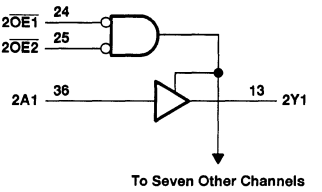
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through each V_{CC} or GND ..... ±75 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

			SN54AHC16541		SN74AHC16541		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 ± 0.3 V		–4		–4	mA
		V_{CC} = 5 ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 ± 0.3 V		4		4	mA
		V_{CC} = 5 ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 ± 0.3 V		100		100	ns/V
		V_{CC} = 5 ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC16541		SN74AHC16541		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
			3 V	2.9	3		2.9		2.9		
			4.5 V	4.4	4.5		4.4		4.4		
		I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
		I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
			3 V			0.1		0.1		0.1	
			4.5 V			0.1		0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	Data inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
	Control inputs					±0.1		±1		±1	
I_{OZ}†		V_O = V_{CC} or GND, V_I ($\overline{OE}$) = V_{IL} or V_{IH}	5.5 V			±0.25		±2.5		±2.5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
C_i		V_I = V_{CC} or GND	5 V		2	10				10	pF
C_o		V_O = V_{CC} or GND	5 V		4						pF

† For input and ouput, I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHC16541		SN74AHC16541		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}*	A	Y	C_L = 15 pF		5	7	1	8.5	1	8.5	ns
t_{PHL}*					5	7	1	8.5	1	8.5	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		6	10.5	1	11	1	11	ns
t_{PZL}*					6	10.5	1	11	1	11	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		7	11	1	12	1	12	ns
t_{PLZ}*					7	11	1	12	1	12	
t_{PLH}	A	Y	C_L = 50 pF		7.5	10.5	1	12	1	12	ns
t_{PHL}					7.5	10.5	1	12	1	12	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		8	14	1	16	1	16	ns
t_{PZL}					8	14	1	16	1	16	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		9	15.4	1	17.5	1	17.5	ns
t_{PLZ}					9	15.4	1	17.5	1	17.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHC16541		SN74AHC16541		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}*	A	Y	C_L = 15 pF		3.5	5	1	6	1	6	ns
t_{PHL}*					3.5	5	1	6	1	6	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		4.7	7.2	1	8.5	1	8.5	ns
t_{PZL}*					4.7	7.2	1	8.5	1	8.5	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		5	7.5	1	8	1	8	ns
t_{PLZ}*					5	7.5	1	8	1	8	
t_{PLH}	A	Y	C_L = 50 pF		5	7	1	8	1	8	ns
t_{PHL}					5	7	1	8	1	8	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		6.2	9.2	1	10.5	1	10.5	ns
t_{PZL}					6.2	9.2	1	10.5	1	10.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		6	8.8	1	10	1	10	ns
t_{PLZ}					6	8.8	1	10	1	10	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN74AHC16541				UNIT
				T_A = 25°C		MIN	MAX	
				MIN	MAX			
$t_{sk(o)}$	A	Y	3.3 V ± 0.3 V		1.5		1.5	ns
			5 V ± 0.5 V		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER		SN74AHC16541		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.7		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

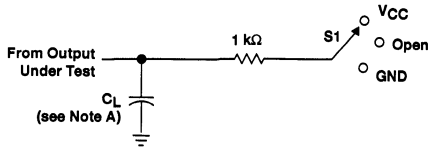
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	12	pF

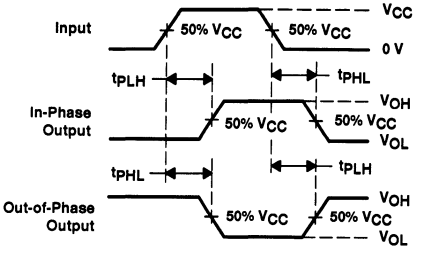
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

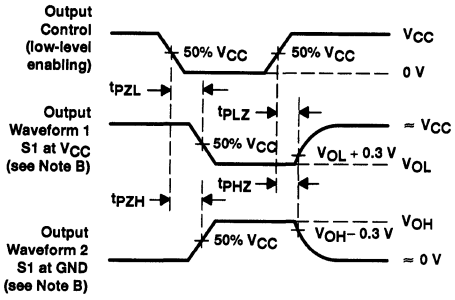


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
DELAY TIMES



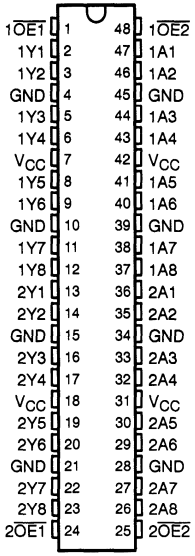
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54AHCT16541 . . . WD PACKAGE
SN74AHCT16541 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'AHCT16541 are noninverting 16-bit buffers composed of two 8-bit sections with separate output-enable signals. For either 8-bit buffer section, the two output-enable (1$\overline{OE1}$ and 1$\overline{OE2}$ or 2$\overline{OE1}$ and 2$\overline{OE2}$) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 8-bit buffer section are in the high-impedance state.

The SN74AHCT16541 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54AHCT16541 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT16541 is characterized for operation from –40°C to 85°C.

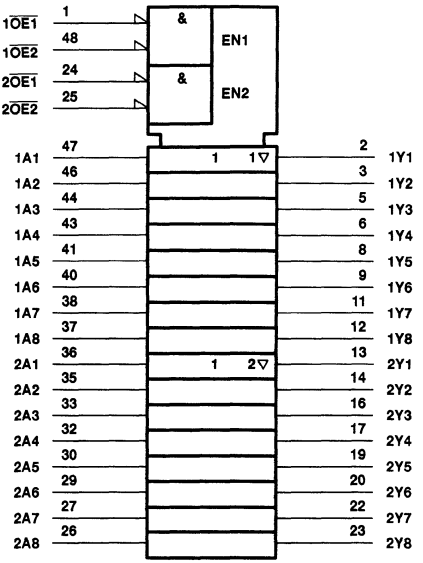
FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

PRODUCT PREVIEW

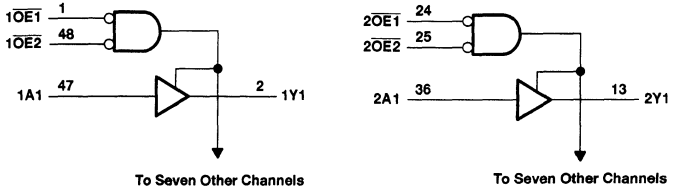
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... –20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through each V_{CC} or GND ..... ±75 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

		SN54AHCT16541		SN74AHCT16541		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT16541		SN74AHCT16541		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	4.5 V	3.15	3.65		3.15		3.15		V
	I_{OH} = –8 mA		2.5			2.4		2.4		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.25		±2.5		±2.5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
ΔI_{CC}†	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			1.35		1.5		1.5	μA
I_{off}	V_O = 5.5 V	0 V			0.5*				5	μA
C_i	V_I = V_{CC} or GND	5 V		2	10				10	pF
C_o	V_O = V_{CC} or GND	5 V		4						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHCT16541		SN74AHCT16541		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}*	A	Y	C_L = 15 pF		4.1	6	1	6.5	1	6.5	ns
t_{PHL}*					3.7	5.5	1	6.5	1	6.5	
t_{PZH}*	$\overline{OE}$	Y	C_L = 15 pF		5	7	1	8	1	8	ns
t_{PZL}*					5	7	1	8	1	8	
t_{PHZ}*	$\overline{OE}$	Y	C_L = 15 pF		4.5	7	1	8	1	8	ns
t_{PLZ}*					4.5	7	1	8	1	8	
t_{PLH}	A	Y	C_L = 50 pF		6.2	8.5	1	9.5	1	9.5	ns
t_{PHL}					6	8.5	1	9.5	1	9.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		7.5	10	1	12	1	12	ns
t_{PZL}					7.5	10	1	12	1	12	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		7	10	1	12	1	12	ns
t_{PLZ}					7	10	1	12	1	12	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

output-skew characteristics, C_L = 50 pF (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN74AHCT16541				UNIT
				T_A = 25°C		MIN	MAX	
				MIN	MAX			
$t_{sk(o)}$	A	Y	5 V ± 0.5 V		1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

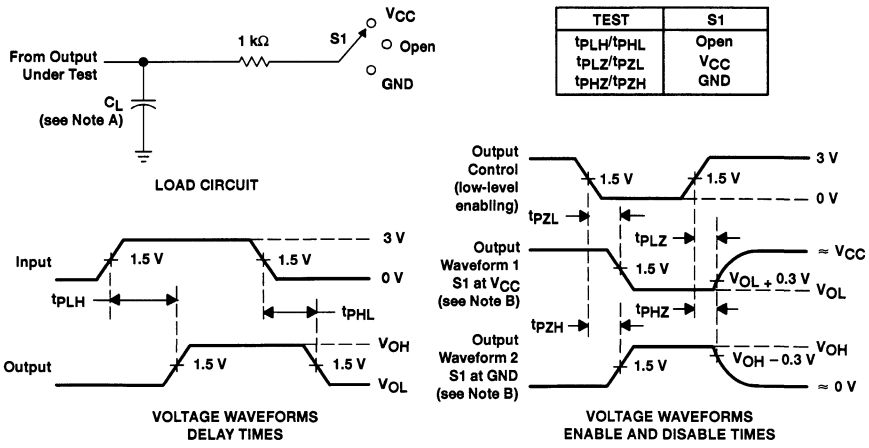
PARAMETER		SN74AHCT16541		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.6		V
$V_{IH(D)}$	High-level dynamic input voltage	2		V
$V_{IL(D)}$	Low-level dynamic input voltage		0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	12	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

Contents

Contents (continued)

Contents (continued)

Extended Temperature Range -40°C to + 125°C

All 74HC/HCT devices contained in this Data Book are specified for operation from -40°C to +85°C.

The plastic encapsulated HC/HCT functions (Dual-In-Line and Small Outline) may be operated in the -40°C to +125°C range provided the 54 HC/HCT data sheets limits are applied.

For power consumption considerations the maximum capacitive load for this extended operating temperature range is limited to 50 pF for all devices.

For higher capacitive loads, as specified for some device types, a power consumption calculation should be carried out using the following formula.

P_D = (C_{PD} x V_{CC} x V_{CC} x fi) + (n x C_{LOAD} x V_{CC} x V_{CC} x fo)
fi = INPUT FREQUENCY
fo = OUTPUT FREQUENCY
n = NUMBER OF OUTPUTS SWITCHING
C_{PD} = REGARDING DATA SHEETS

For operation at 125°C the power dissipation should not exceed 300 mW for SO-packages and 400 mW for DIL-packages. For SSOP (DB) packages please contact your local sales representatives.

- **Package Options Include Plastic Small-Outline (D), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

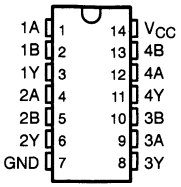
These devices contain four independent 2-input NAND gates. They perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54HC00 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC00 is characterized for operation from –40°C to 85°C.

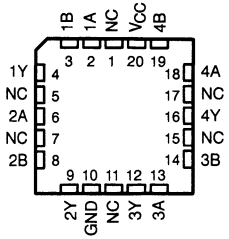
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

SN54HC00 . . . J OR W PACKAGE
SN74HC00 . . . D, N, OR PW PACKAGE
(TOP VIEW)

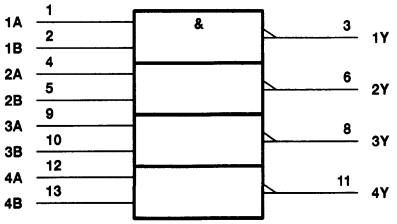


SN54HC00 . . . FK PACKAGE
(TOP VIEW)



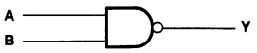
NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, PW, and W packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC00			SN74HC00			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC00		SN74HC00		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			2		40		20	μA
C_i			2 V to 6 V		3	10		10		10	pF

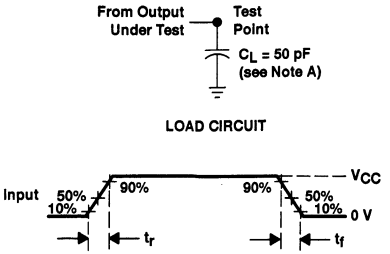
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC00		SN74HC00		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		45	90		135		115	ns
			4.5 V		9	18		27		23	
			6 V		8	15		23		20	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

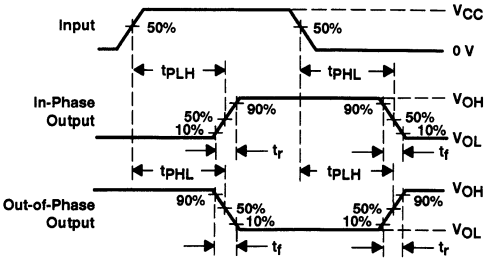
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	20	pF

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

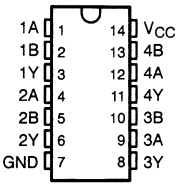
NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

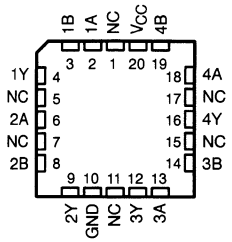
SCLS062A – NOVEMBER 1988 – REVISED JANUARY 1996

- **Inputs Are TTL-Voltage Compatible**
- **Package Options Include Plastic Small-Outline (D), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HCT00 . . . J OR W PACKAGE
SN74HCT00 . . . D, N, OR PW PACKAGE
(TOP VIEW)



SN54HCT00 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

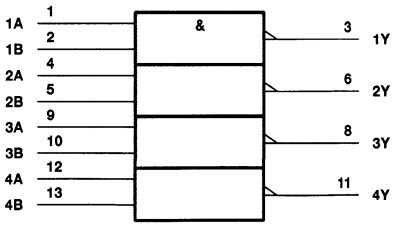
These devices contain four independent 2-input NAND gates. They perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54HCT00 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT00 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, PW, and W packages.

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HCT00			SN74HCT00			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time		0		500	0		500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT00		SN74HCT00		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	4.5 V	4.4	4.499		4.4		4.4		V
		I_{OH} = –4 mA		3.98	4.3		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
		I_{OL} = 4 mA			0.17	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0		5.5 V			2		40		20	μA
ΔI_{CC}‡	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i			4.5 V to 5.5 V		3	10		10		10	pF

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

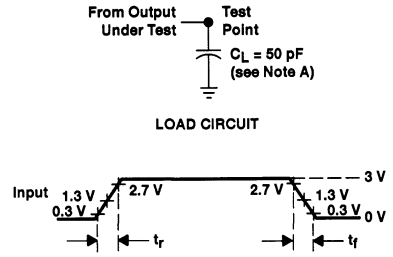
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT00		SN74HCT00		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	4.5 V		11	20		30		25	ns
			5.5 V		10	18		27		22	
t_t		Y	4.5 V		9	15		22		19	ns
			5.5 V		8	14		20		17	

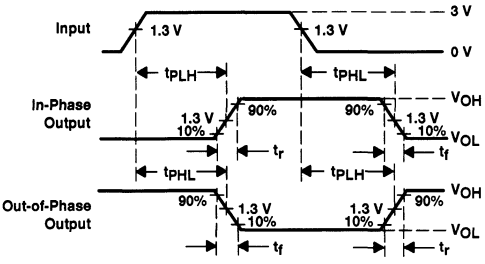
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	20	pF

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

SCLS076A – DECEMBER 1982 – REVISED JANUARY 1996

- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

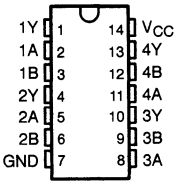
These devices contain four independent 2-input NOR gates. They perform the Boolean function $Y = \overline{A + B}$ or $Y = \overline{A} \bullet \overline{B}$ in positive logic.

The SN54HC02 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC02 is characterized for operation from –40°C to 85°C.

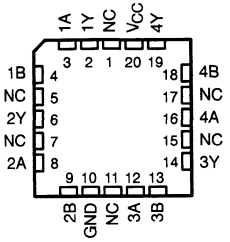
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

SN54HC02 . . . J OR W PACKAGE
SN74HC02 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)

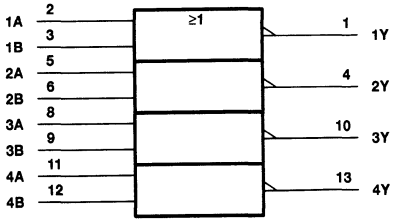


SN54HC02 . . . FK PACKAGE
(TOP VIEW)



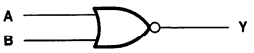
NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
DB and PW packages ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC02			SN74HC02			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC02		SN74HC02		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V			±0.1		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			2		40		20	μA
C_i			2 V to 6 V		3	10		10		10	pF

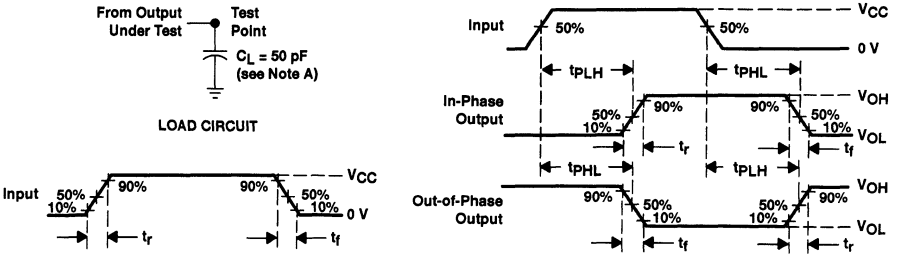
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC02		SN74HC02		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		45	90		135		115	ns
			4.5 V		9	18		27		23	
			6 V		8	15		23		20	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	22	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

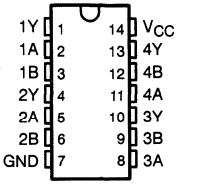
These devices contain four independent 2-input NOR gates. They perform the Boolean function $Y = \overline{A} \bullet \overline{B}$ or $Y = \overline{A + B}$ in positive logic.

The SN54HCT02 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT02 is characterized for operation from –40°C to 85°C.

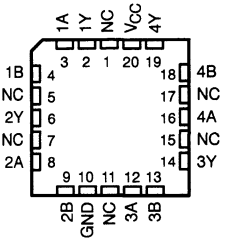
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

SN54HCT02 . . . J OR W PACKAGE
SN74HCT02 . . . D OR N PACKAGE
(TOP VIEW)

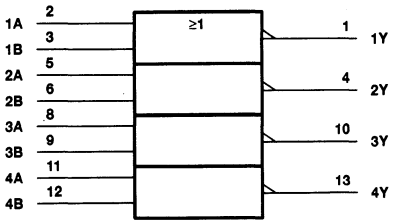


SN54HCT02 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HCT02			SN74HCT02			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time		0		500	0		500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT02		SN74HCT02		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 µA	4.5 V	4.4	4.499		4.4		4.4		V
		I_{OH} = –4 mA		3.98	4.3		3.7		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	4.5 V		0.001	0.1		0.1		0.1	V
		I_{OL} = 4 mA			0.17	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0,	I_O = 0	5.5 V			2		40		20	µA
ΔI_{CC}‡	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i			4.5 V to 5.5 V		3	10		10		10	pF

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

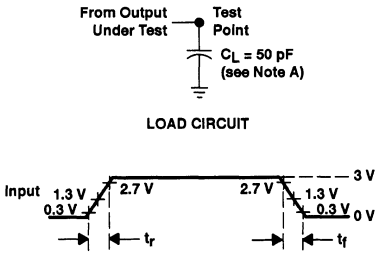
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT02		SN74HCT02		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	4.5 V		11	20		30		25	ns
			5.5 V		10	18		27		22	
t_t		Y	4.5 V		9	15		22		19	ns
			5.5 V		8	14		20		17	

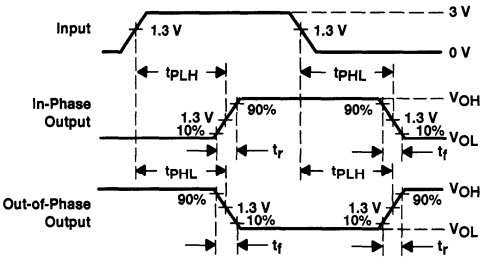
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	20	pF

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

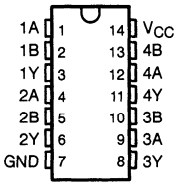
These devices contain four independent 2-input NAND gates. They perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic. The open-drain outputs require pullup resistors to perform correctly. They may be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

The SN54HC03 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC03 is characterized for operation from –40°C to 85°C.

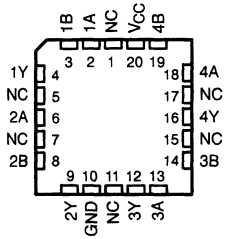
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

SN54HC03 . . . J OR W PACKAGE
SN74HC03 . . . D OR N PACKAGE
(TOP VIEW)

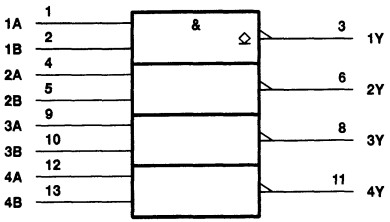


SN54HC03 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC03			SN74HC03			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC03		SN74HC03		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
I_{OH}	V_I = V_{IH} or V_{IL},	V_O = V_{CC}	6 V		0.01	0.5		10		5	µA
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			2		40		20	µA
C_i			2 V to 6 V		3	10		10		10	pF

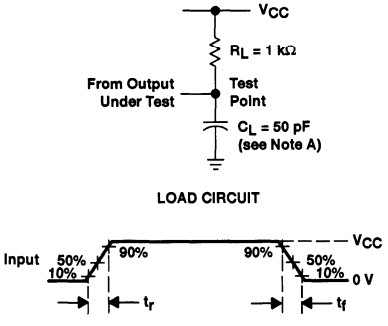
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

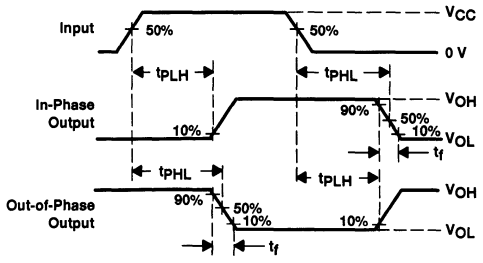
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC03		SN74HC03		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2 V		60	105		155		131	ns
			4.5 V		13	25		36		31	
			6 V		10	23		31		27	
t_{PHL}	A or B	Y	2 V		50	100		150		125	ns
			4.5 V		10	20		30		25	
			6 V		8	17		25		21	
t_f		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	20	pF

PARAMETER MEASUREMENT INFORMATION





NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCLS078A – DECEMBER 1982 – REVISED JANUARY 1996

- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

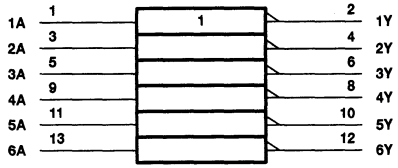
These devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$ in positive logic.

The SN54HC04 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC04 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

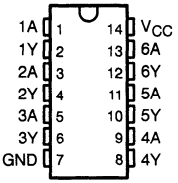
logic symbol†



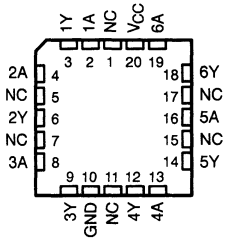
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)

SN54HC04 . . . J OR W PACKAGE
SN74HC04 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54HC04 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
DB and PW packages ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC04			SN74HC04			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC04		SN74HC04		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			2		40		20	μA
C_i			2 V to 6 V		3	10		10		10	pF

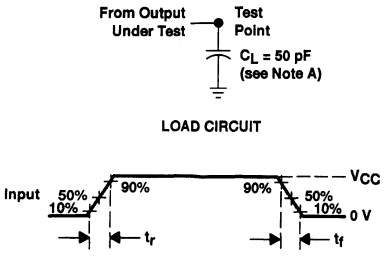
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC04		SN74HC04		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		45	95		145		120	ns
			4.5 V		9	19		29		24	
			6 V		8	16		25		20	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

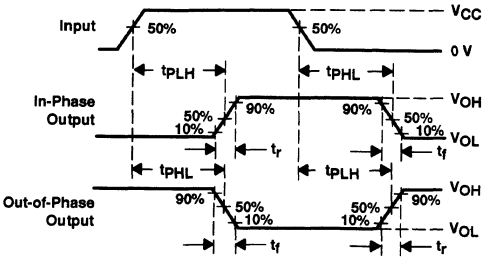
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per inverter	No load	20	pF

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

SCLS079A – MARCH 1984 – REVISED JANUARY 1996

- **Unbuffered Outputs**
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

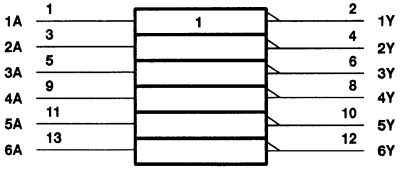
These devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$ in positive logic.

The SN54HCU04 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCU04 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each inverter)

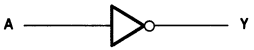
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†

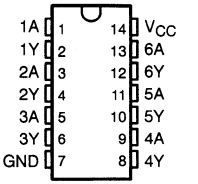


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

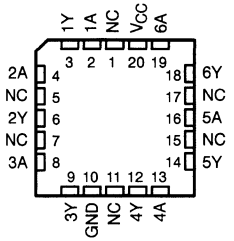
logic diagram (positive logic)



SN54HCU04 . . . J OR W PACKAGE
SN74HCU04 . . . D OR N PACKAGE
(TOP VIEW)



SN54HCU04 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HCU04			SN74HCU04			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.7			1.7			V
		V_{CC} = 4.5 V	3.6			3.6			
		V_{CC} = 6 V	4.8			4.8			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCU04		SN74HCU04		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{CC} or GND	I_{OH} = –20 μA	2 V	1.8			1.8		1.8		V
			4.5 V	4			4		4		
			6 V	5.5			5.5		5.5		
		I_{OH} = –4 mA	4.5 V	3.98			3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48			5.2		5.34		
V_{OL}	V_I = V_{CC} or GND	I_{OL} = 20 μA	2 V			0.2		0.2		0.2	V
			4.5 V			0.5		0.5		0.5	
			6 V			0.5		0.5		0.5	
		I_{OL} = 4 mA	4.5 V			0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V			0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V			±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			2		40		20	μA
C_i			2 V to 6 V		3	10		10		10	pF

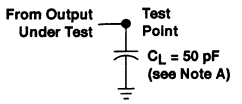
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCU04		SN74HCU04		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		40	80		120		100	ns
			4.5 V		8	16		24		20	
			6 V		7	14		20		17	
t_f		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

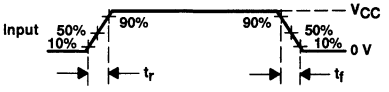
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per inverter	No load	20	pF

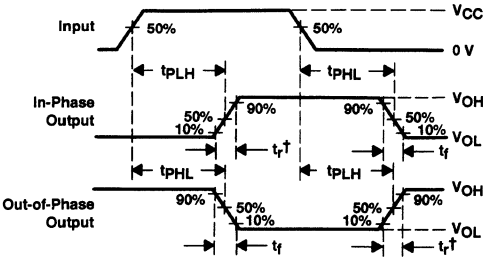
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



† t_r is not applicable to 'HCU devices.

VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Package Options Include Plastic Small-Outline (D), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

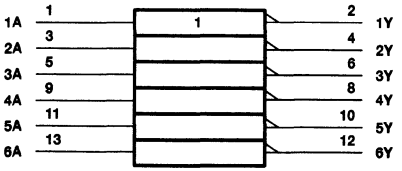
These devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$ in positive logic.

The SN54HCT04 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT04 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

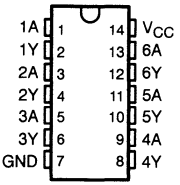
logic symbol†



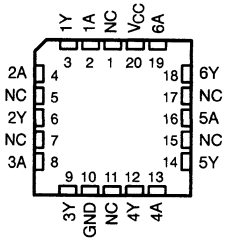
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and PW packages.

logic diagram (positive logic)

SN54HCT04 . . . J OR W PACKAGE
SN74HCT04 . . . D, N, OR PW PACKAGE
(TOP VIEW)



SN54HCT04 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HCT04			SN74HCT04			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time		0		500	0		500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT04		SN74HCT04		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 μA	4.5 V	4.4	4.499		4.4		4.4		V
		I_{OH} = –4 mA		3.98	4.3		3.7		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
		I_{OL} = 4 mA			0.17	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0		5.5 V			2		40		20	μA
ΔI_{CC}‡	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i			4.5 V to 5.5 V		3	10		10		10	pF

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

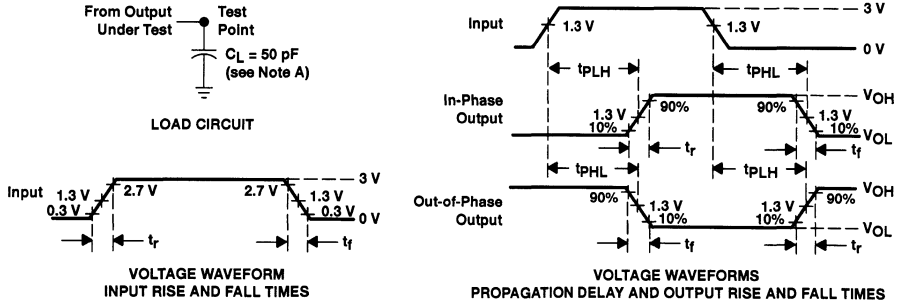
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT04		SN74HCT04		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5 V		14	20		30		25	ns
			5.5 V		13	18		27		23	
t_t		Y	4.5 V		9	15		22		19	ns
			5.5 V		8	14		20		17	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per inverter	No load	20	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

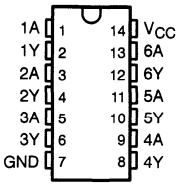
These devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$ in positive logic. The open-drain outputs require pullup resistors to perform correctly. They may be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

The SN54HC05 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC05 is characterized for operation from –40°C to 85°C.

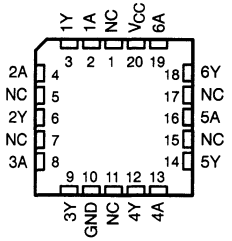
FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

SN54HC05 . . . J OR W PACKAGE
SN74HC05 . . . D OR N PACKAGE
(TOP VIEW)

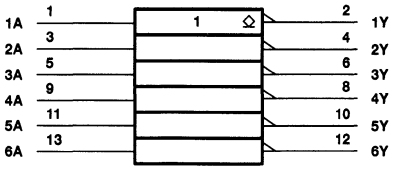


SN54HC05 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC05			SN74HC05			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C		SN54HC05	SN74HC05	UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
I_{OH}	$V_I = V_{IH}$ or V_{IL},	$V_O = V_{CC}$	6 V		0.01	0.5		10		5	µA
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0,	I_O = 0	6 V			2		40		20	µA
C_i			2 V to 6 V		3	10		10		10	pF

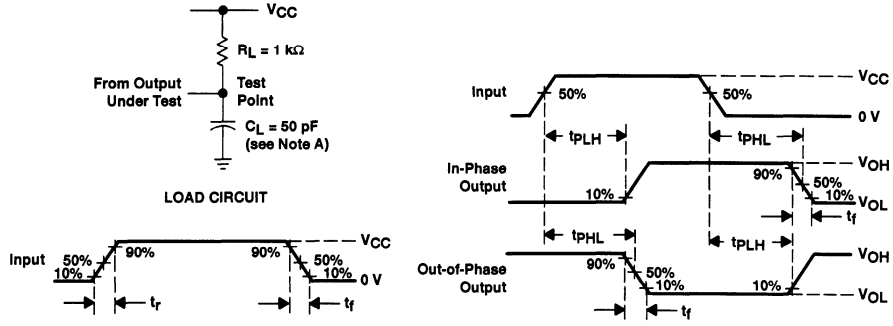
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC05		SN74HC05		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2 V		60	115		175		145	ns
			4.5 V		13	23		35		29	
			6 V		10	20		30		25	
t_{PHL}	A	Y	2 V		45	85		130		105	ns
			4.5 V		9	17		26		21	
			6 V		8	14		22		18	
t_f		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per inverter	No load	20	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Package Options Include Plastic Small-Outline (D), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

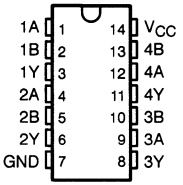
These devices contain four independent 2-input AND gates. They perform the Boolean function $Y = A \bullet B$ or $Y = \overline{A + B}$ in positive logic.

The SN54HC08 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC08 is characterized for operation from –40°C to 85°C.

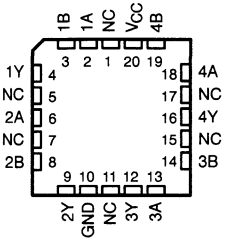
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

SN54HC08 . . . J OR W PACKAGE
SN74HC08 . . . D, N, OR PW PACKAGE
(TOP VIEW)

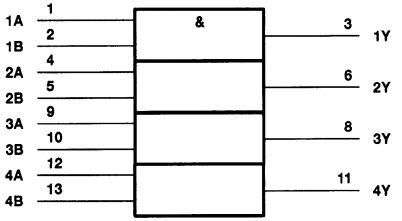


SN54HC08 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, PW, and W packages.

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC08			SN74HC08			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC08		SN74HC08		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V			±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			2		40		20	μA
C_i			2 V to 6 V		3	10		10		10	pF

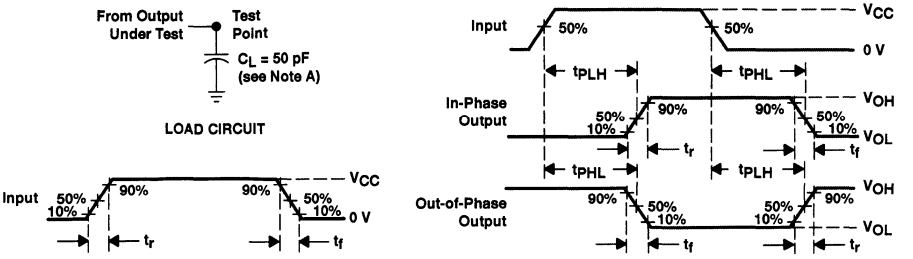
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC08		SN74HC08		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		50	100		150		125	ns
			4.5 V		10	20		30		25	
			6 V		8	17		25		21	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	20	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

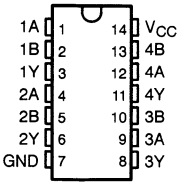
These devices contain four independent 2-input AND gates. They perform the Boolean function $Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

The SN54HCT08 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT08 is characterized for operation from –40°C to 85°C.

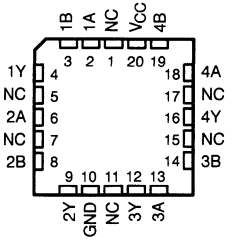
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

SN54HCT08 . . . J OR W PACKAGE
SN74HCT08 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)

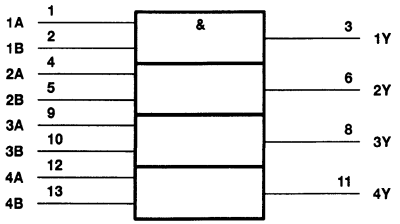


SN54HCT08 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
DB and PW packages ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HCT08			SN74HCT08			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time		0		500	0		500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT08		SN74HCT08		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 μA	4.5 V	4.4	4.499		4.4		4.4		V
		I_{OH} = –4 mA		3.98	4.3		3.7		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
		I_{OL} = 4 mA			0.17	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0		5.5 V			2		40		20	μA
ΔI_{CC}‡	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i			4.5 V to 5.5 V		3	10		10		10	pF

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

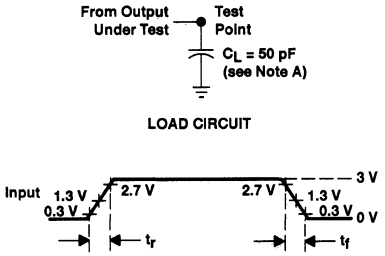
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT08		SN74HCT08		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	4.5 V		15	24		35		30	ns
			5.5 V		13	22		32		27	
t_t		Y	4.5 V		9	15		22		19	ns
			5.5 V		8	14		20		17	

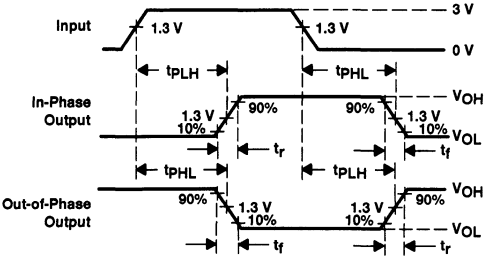
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	20	pF

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

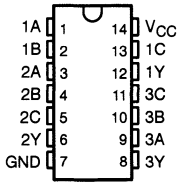
These devices contain three independent 3-input NAND gates. They perform the Boolean function $Y = \overline{A \bullet B \bullet C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

The SN54HC10 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC10 is characterized for operation from –40°C to 85°C.

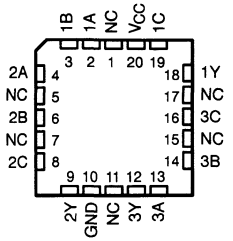
FUNCTION TABLE
(each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

SN54HC10 . . . J OR W PACKAGE
SN74HC10 . . . D OR N PACKAGE
(TOP VIEW)

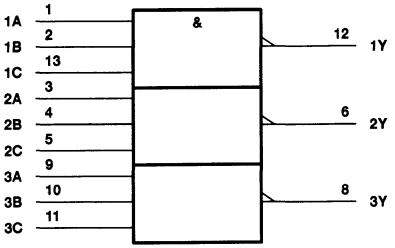


SN54HC10 . . . FK PACKAGE
(TOP VIEW)



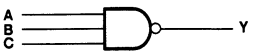
NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC10			SN74HC10			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC10		SN74HC10		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V			±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			2		40		20	μA
C_i			2 V to 6 V		3	10		10		10	pF

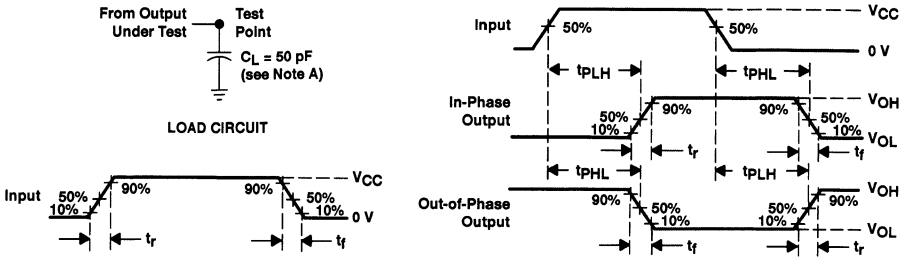
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC10		SN74HC10		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	2 V		35	95		145		120	ns
			4.5 V		10	19		29		24	
			6 V		9	16		25		20	
t_t		Y	2 V		23	75		110		95	ns
			4.5 V		6	15		22		19	
			6 V		5	13		19		16	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	25	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

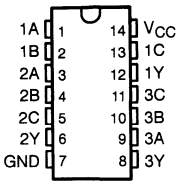
These devices contain three independent 3-input AND gates. They perform the Boolean function $Y = A \bullet B \bullet C$ or $Y = \overline{\overline{A} + \overline{B} + \overline{C}}$ in positive logic.

The SN54HC11 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC11 is characterized for operation from –40°C to 85°C.

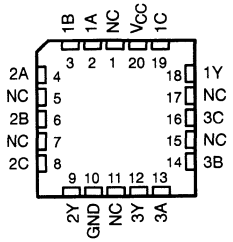
FUNCTION TABLE
(each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

SN54HC11 . . . J OR W PACKAGE
SN74HC11 . . . D OR N PACKAGE
(TOP VIEW)

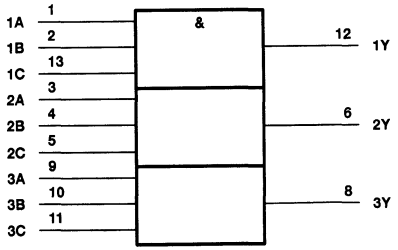


SN54HC11 . . . FK PACKAGE
(TOP VIEW)



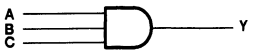
NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC11			SN74HC11			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC11		SN74HC11		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			2		40		20	μA
C_i			2 V to 6 V		3	10		10		10	pF

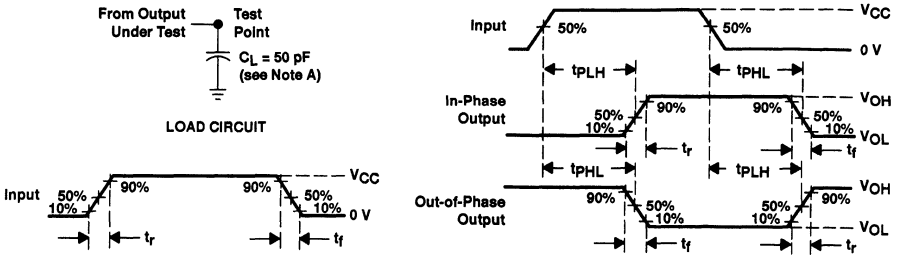
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC11		SN74HC11		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	2 V		35	100		150		125	ns
			4.5 V		10	20		30		25	
			6 V		8	17		25		21	
t_t		Y	2 V		25	75		110		95	ns
			4.5 V		7	15		22		19	
			6 V		5	13		19		16	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	25	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Package Options Include Plastic Small-Outline (D), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

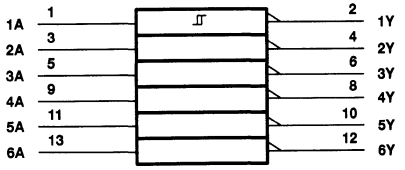
These Schmitt-trigger devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$ in positive logic.

The SN54HC14 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC14 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

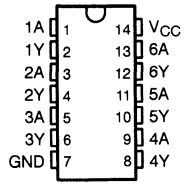
logic symbol†



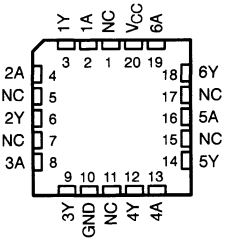
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, PW, and W packages.

logic diagram (positive logic)

SN54HC14 . . . J OR W PACKAGE
SN74HC14 . . . D, N, OR PW PACKAGE
(TOP VIEW)



SN54HC14 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC14			SN74HC14			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC14		SN74HC14		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
V_{T+}			2 V	0.7	1.2	1.5	0.7	1.5	0.7	1.5	V
			4.5 V	1.55	2.5	3.15	1.55	3.15	1.55	3.15	
			6 V	2.1	3.3	4.2	2.1	4.2	2.1	4.2	
V_{T-}			2 V	0.3	0.6	1	0.3	1	0.3	1	V
			4.5 V	0.9	1.6	2.45	0.9	2.45	0.9	2.45	
			6 V	1.2	2	3.2	1.2	3.2	1.2	3.2	
$V_{T+} - V_{T-}$			2 V	0.2	0.6	1.2	0.2	1.2	0.2	1.2	V
			4.5 V	0.4	0.9	2.1	0.4	2.1	0.4	2.1	
			6 V	0.5	1.3	2.5	0.5	2.5	0.5	2.5	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			2		40		20	μA
C_i			2 V to 6 V		3	10		10		10	pF

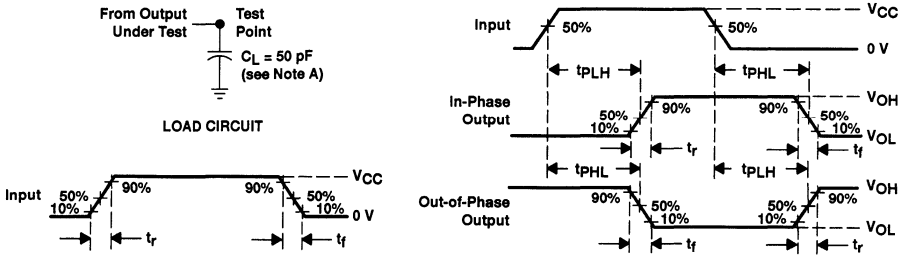
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC14		SN74HC14		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		55	125		190		155	ns
			4.5 V		12	25		38		31	
			6 V		11	21		32		26	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per inverter	No load	20	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

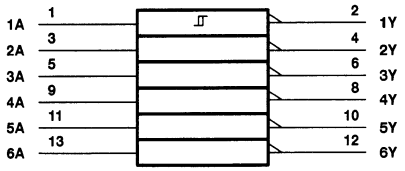
The 'HCT14 contain six independent inverters. The devices perform the Boolean function $Y = \overline{A}$ in positive logic.

The SN54HCT14 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT14 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each inverter)

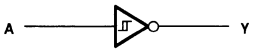
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†

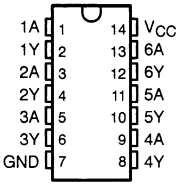


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

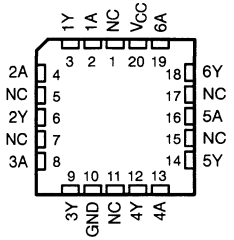
logic diagram (positive logic)



SN54HCT14 . . . J OR W PACKAGE
SN74HCT14 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54HCT14 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to V_{CC} +0.5 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} +0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
DB and PW packages ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HCT14		SN74HCT14		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.1		2.1		V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V		0.5		0.5	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
T_A	Operating free-air temperature		–55	125	–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT14		SN74HCT14		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{T+} Positive-going threshold			4.5 V	1.2	1.5	1.9	1.2	1.9	1.2	1.9	V
			5.5 V	1.4	1.7	2.1	1.4	2.1	1.4	2.1	
V_{T-} Negative-going threshold			4.5 V	0.5	0.9	1.2	0.5	1.2	0.5	1.2	V
			5.5 V	0.6	1	1.4	0.6	1.4	0.6	1.4	
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)			4.5 V	0.4	0.6	1.4	0.4	1.4	0.4	1.4	V
			5.5 V	0.4	0.65	1.5	0.4	1.5	0.4	1.5	
V_{OH}	V_I = V_{IH} or V_{IL},	I_{OH} = –20 μA	4.5 V	4.4	4.49		4.4		4.4		V
	V_I = V_{IH} or V_{IL},	I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL},	I_{OL} = 20 μA	4.5 V		.001	0.1		0.1		0.1	V
	V_I = V_{IH} or V_{IL},	I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	V_I = V_{CC} or GND		5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	5.5 V			2		40		20	μA
ΔI_{CC}†	One input at 0.5 V or 2.4 V, Other inputs at GND or V_{CC}		5.5 V		0.2	2.4		3		2.9	mA
C_i	V_I = V_{CC} or GND		5 V		3	10		10		10	pF

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

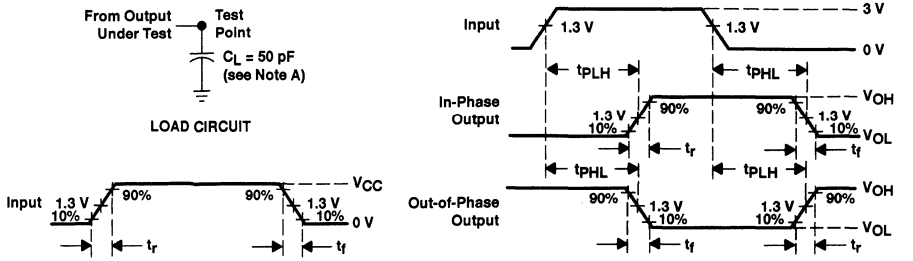
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT14		SN74HCT14		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5 V		20	32		48		40	ns
			5.5 V		18	30		45		38	
t_t		Y	4.5 V		7	15		22		19	ns
			5.5 V		6	14		20		17	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	10	pF

PARAMETER MEASUREMENT INFORMATION

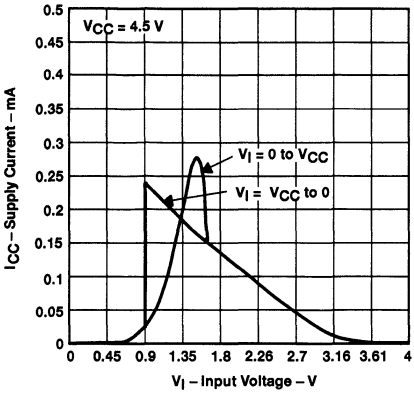


NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

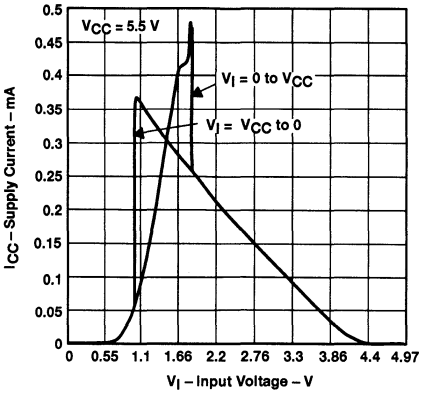
Figure 1. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

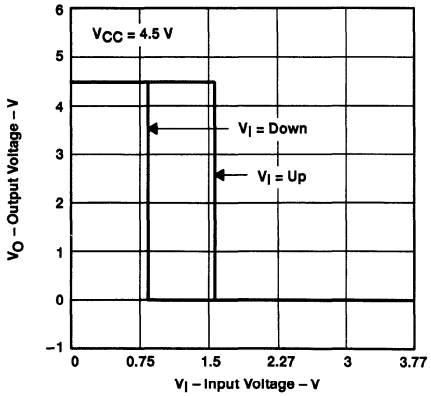
SUPPLY CURRENT vs INPUT VOLTAGE



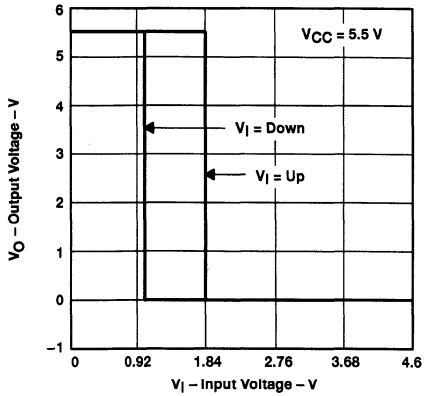
SUPPLY CURRENT vs INPUT VOLTAGE



OUTPUT VOLTAGE vs INPUT VOLTAGE



OUTPUT VOLTAGE vs INPUT VOLTAGE



- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

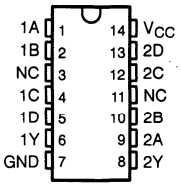
These devices contain two independent 4-input NAND gates. They perform the Boolean function $Y = \overline{A \bullet B \bullet C \bullet D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

The SN54HC20 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC20 is characterized for operation from –40°C to 85°C.

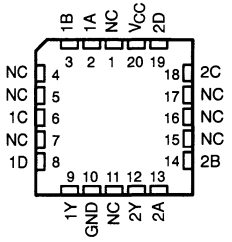
FUNCTION TABLE
(each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

SN54HC20 . . . J OR W PACKAGE
SN74HC20 . . . D OR N PACKAGE
(TOP VIEW)

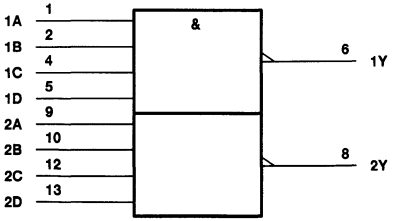


SN54HC20 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)

Pin numbers shown are for the D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC20			SN74HC20			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC20		SN74HC20		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			2		40		20	μA
C_i			2 V to 6 V		3	10		10		10	pF

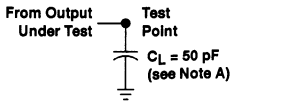
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC20		SN74HC20		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, C, or D	Y	2 V		45	110		165		140	ns
			4.5 V		14	22		33		28	
			6 V		11	19		28		24	
t_t		Y	2 V		27	75		110		95	ns
			4.5 V		9	15		22		19	
			6 V		7	13		19		16	

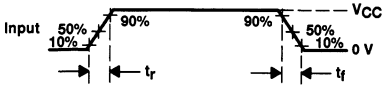
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	25	pF

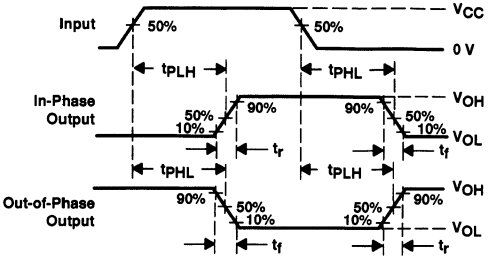
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



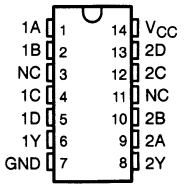
VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

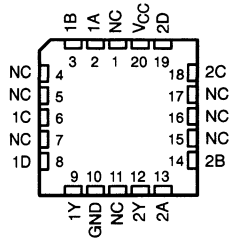
Figure 1. Load Circuit and Voltage Waveforms

- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC21 . . . J OR W PACKAGE
SN74HC21 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC21 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

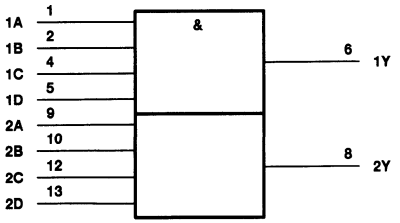
These devices contain two independent 2-input AND gates. They perform the Boolean function $Y = A \bullet B \bullet C \bullet D$ or $Y = \overline{\overline{A} + \overline{B} + \overline{C} + \overline{D}}$ in positive logic.

The SN54HC21 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC21 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)

Pin numbers shown are for the D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC21			SN74HC21			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC21		SN74HC21		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			2		40		20	μA
C_i			2 V to 6 V		3	10		10		10	pF

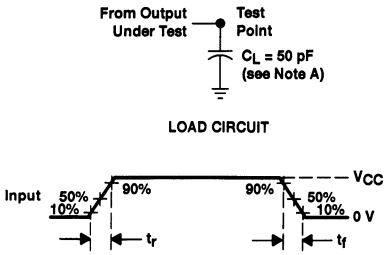
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC21		SN74HC21		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, C, or D	Y	2 V		44	110		165		140	ns
			4.5 V		14	22		33		28	
			6 V		11	19		28		24	
t_t		Y	2 V		29	75		110		95	ns
			4.5 V		10	15		22		19	
			6 V		8	13		19		16	

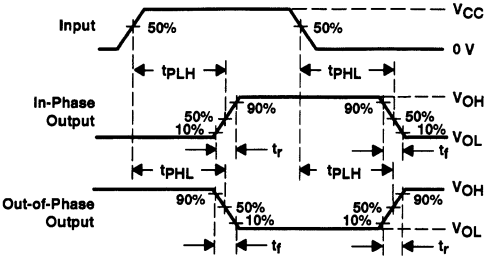
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	25	pF

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

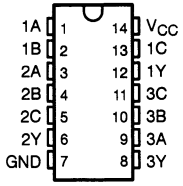
These devices contain three independent 3-input NOR gates. They perform the Boolean function $Y = \overline{A + B + C}$ or $Y = \overline{A} \bullet \overline{B} \bullet \overline{C}$ in positive logic.

The SN54HC27 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC27 is characterized for operation from –40°C to 85°C.

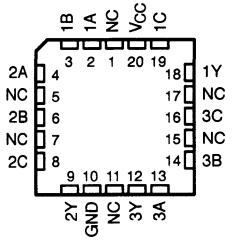
FUNCTION TABLE
(each gate)

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

SN54HC27 . . . J OR W PACKAGE
SN74HC27 . . . D OR N PACKAGE
(TOP VIEW)

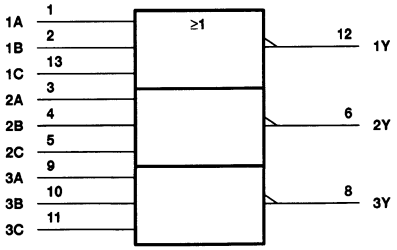


SN54HC27 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC27			SN74HC27			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC27		SN74HC27		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			2		40		20	μA
C_i			2 V to 6 V		3	10		10		10	pF

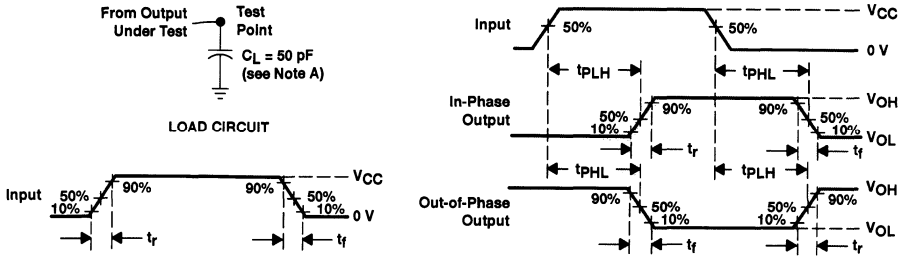
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC27		SN74HC27		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	2 V		35	90		135		115	ns
			4.5 V		10	18		27		23	
			6 V		9	15		23		20	
t_t		Y	2 V		27	75		110		95	ns
			4.5 V		7	15		22		19	
			6 V		6	13		19		16	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	25	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

SCLS200A – DECEMBER 1982 – REVISED JANUARY 1996

- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

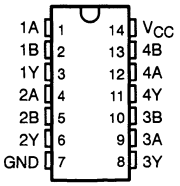
These devices contain four independent 2-input OR gates. They perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = A + B$ in positive logic.

The SN54HC32 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC32 is characterized for operation from –40°C to 85°C.

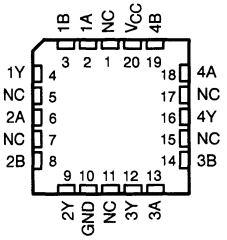
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

SN54HC32 . . . J OR W PACKAGE
SN74HC32 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)

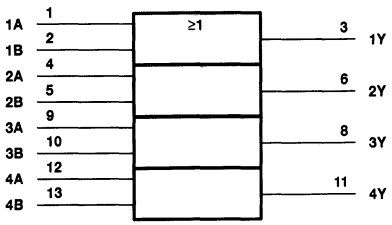


SN54HC32 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
DB and PW packages ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC32			SN74HC32			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC32		SN74HC32		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V			±0.1		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			2		40		20	μA
C_i			2 V to 6 V		3	10		10		10	pF

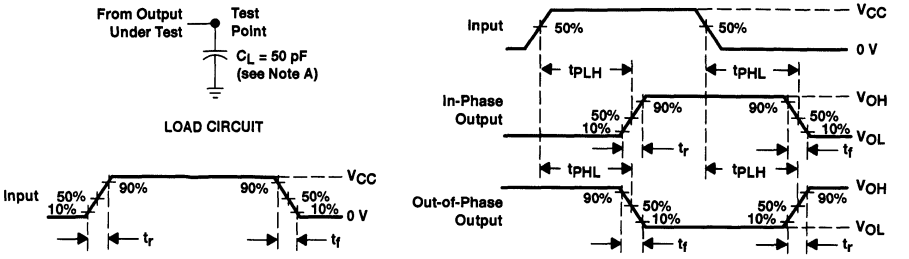
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC32		SN74HC32		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		50	100		150		125	ns
			4.5 V		10	20		30		25	
			6 V		8	17		25		21	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	20	pF

PARAMETER MEASUREMENT INFORMATION



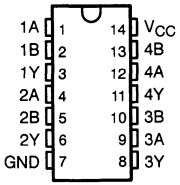
NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

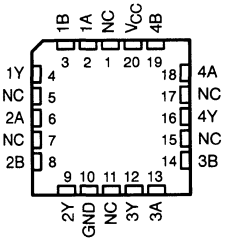
SCLS064A – NOVEMBER 1988 – REVISED JANUARY 1996

- **Inputs Are TTL-Voltage Compatible**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HCT32 . . . J OR W PACKAGE
SN74HCT32 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54HCT32 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

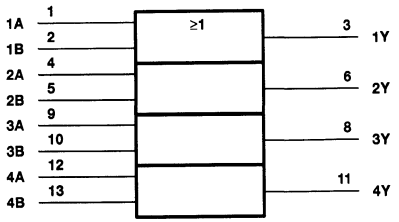
The 'HCT32 contain four independent 2-input OR gates. They perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = A + B$ in positive logic.

The SN54HCT32 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT32 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
DB and PW packages ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HCT32			SN74HCT32			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time		0		500	0		500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT32		SN74HCT32		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 μA	4.5 V	4.4	4.499		4.4		4.4		V
		I_{OH} = –4 mA		3.98	4.3		3.7		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
		I_{OL} = 4 mA			0.17	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0		5.5 V			2		40		20	μA
ΔI_{CC}‡	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i			4.5 V to 5.5 V		3	10		10		10	pF

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

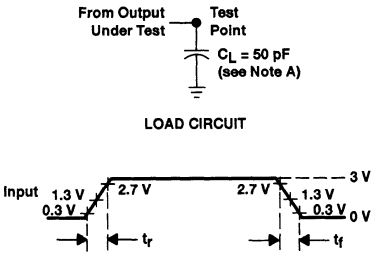
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT32		SN74HCT32		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	4.5 V		15	24		35		30	ns
			5.5 V		13	22		32		27	
t_t		Y	4.5 V		9	15		22		19	ns
			5.5 V		8	14		20		17	

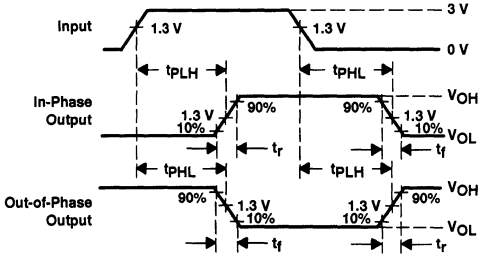
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	20	pF

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES

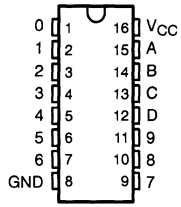
NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

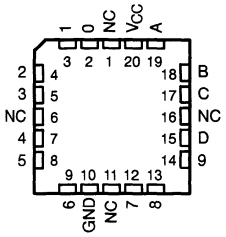
SCLS091A – DECEMBER 1982 – REVISED JANUARY 1996

- **Full Decoding of Input Logic**
- **All Outputs Are High for Invalid BCD Conditions**
- **Also for Applications as 3-Line to 8-Line Decoders**
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC42 . . . J OR W PACKAGE
SN74HC42 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC42 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

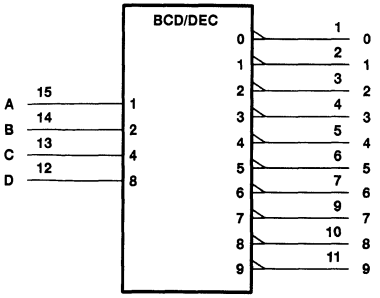
These monolithic decimal decoders consist of eight inverters and ten 4-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all inputs remain off for all invalid input conditions.

The SN54HC42 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC42 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

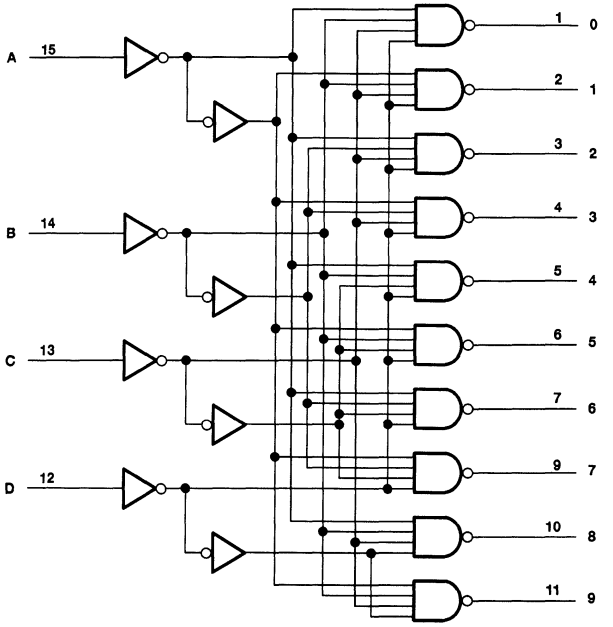
NO.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
Invalid	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC42			SN74HC42			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC42		SN74HC42		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

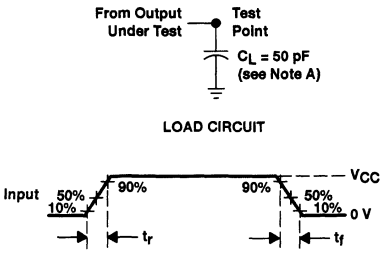
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC42		SN74HC42		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, C, or D	0–9	2 V		65	150		225		190	ns
			4.5 V		18	30		45		38	
			6 V		14	26		38		32	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		7	13		19		16	

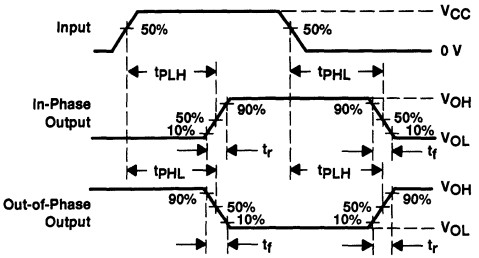
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	39	pF

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

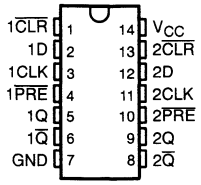
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

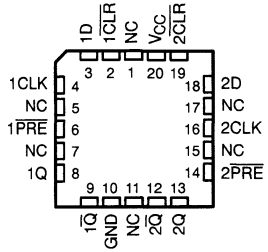
The 'HC74 contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of CLK. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The SN54HC74 is characterized for operation over the full military temperature range –55°C to 125°C. The SN74HC74 is characterized for operation from –40°C to 85°C.

SN54HC74 . . . J OR W PACKAGE
SN74HC74 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54HC74 . . . FK PACKAGE
(TOP VIEW)



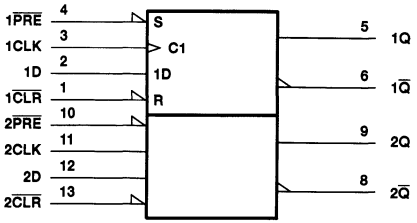
NC – No internal connection

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

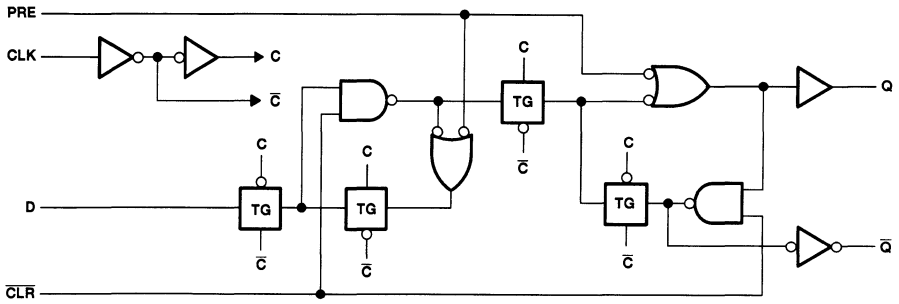
† This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
DB and PW packages ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC74			SN74HC74			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC74		SN74HC74		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V			±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			4		80		40	μA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC74		SN74HC74		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	29	
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		CLK high or low	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time before CLK↑	Data	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2 V	25		40		30		
			4.5 V	5		8		6		
			6 V	4		7		5		
t_h	Hold time, data after CLK↑		2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		

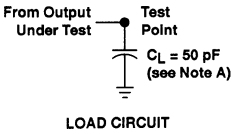
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC74		SN74HC74		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	10		4.2		5		MHz
			4.5 V	31	50		21		25		
			6 V	36	60		25		29		
t_{pd}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2 V		70	230		345		290	ns
			4.5 V		20	46		69		58	
			6 V		15	39		59		49	
	CLK	Q or $\overline{Q}$	2 V		70	175		250		220	
			4.5 V		20	35		50		44	
			6 V		15	30		42		37	
t_t		Q or $\overline{Q}$	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

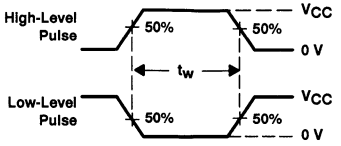
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	No load	35	pF

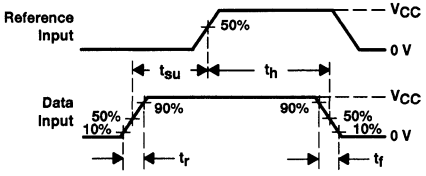
PARAMETER MEASUREMENT INFORMATION



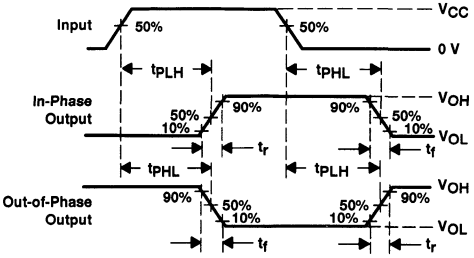
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

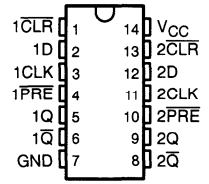
- **Inputs Are TTL-Voltage Compatible**
- **Package Options Include Plastic Small-Outline (D), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

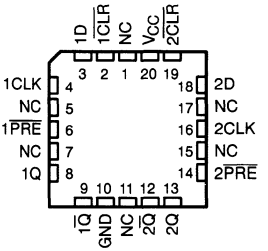
The 'HCT74 contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of CLK. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

The SN54HCT74 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT74 is characterized for operation from –40°C to 85°C.

SN54HCT74 . . . J OR W PACKAGE
SN74HCT74 . . . D, N, OR PW PACKAGE
(TOP VIEW)



SN54HCT74 . . . FK PACKAGE
(TOP VIEW)



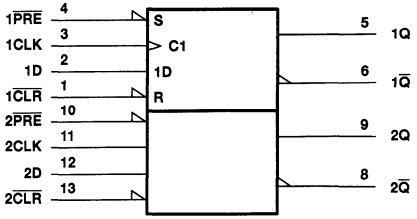
NC – No internal connection

FUNCTION TABLE

INPUTS				OUTPUT	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

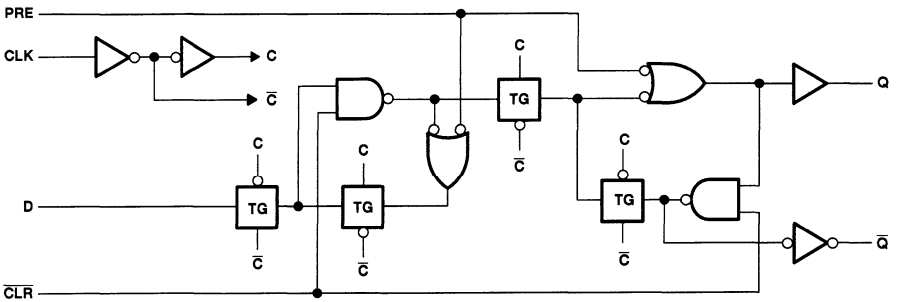
† This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, PW, and W packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HCT74			SN74HCT74			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time		0		500	0		500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT74		SN74HCT74		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	4.5 V	4.4	4.499		4.4		4.4		V
		I_{OH} = –4 mA		3.98	4.3		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
		I_{OL} = 4 mA			0.17	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}†	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i			4.5 V to 5.5 V		3	10		10		10	pF

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HCT74		SN74HCT74		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		4.5 V	0	27	0	18	0	22	MHz
			5.5 V	0	30	0	20	0	24	
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	4.5 V	16		24		20		ns
			5.5 V	14		21		18		
		CLK high or low	4.5 V	18		27		23		
			5.5 V	16		24		21		
t_{su}	Setup time before CLK↑	Data	4.5 V	12		18		15		ns
			5.5 V	11		16		14		
		$\overline{PRE}$ or $\overline{CLR}$ inactive	4.5 V	0		0		0		
			5.5 V	0		0		0		
t_h	Hold time, data after CLK↑		4.5 V	0		0		0		ns
			5.5 V	0		0		0		

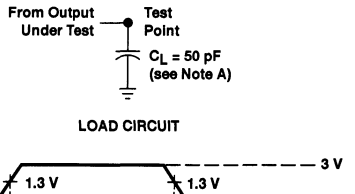
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT74		SN74HCT74		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			4.5 V	27	40		18		22		MHz
			5.5 V	30	46		20		24		
t_{pd}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	4.5 V		21	35		53		44	ns
			5.5 V		17	31		48		40	
	CLK	Q or $\overline{Q}$	4.5 V		20	28		42		35	
			5.5 V		18	25		38		31	
t_t		Q or $\overline{Q}$	4.5 V		8	15		22		19	ns
			5.5 V		7	14		20		17	

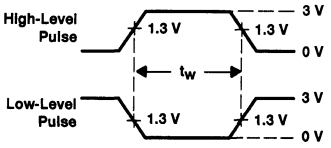
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	No load	35	pF

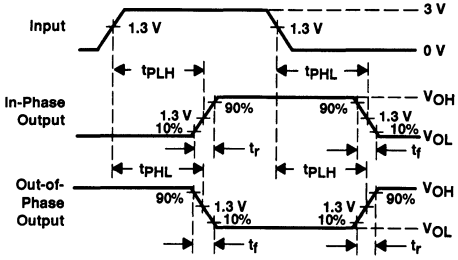
PARAMETER MEASUREMENT INFORMATION



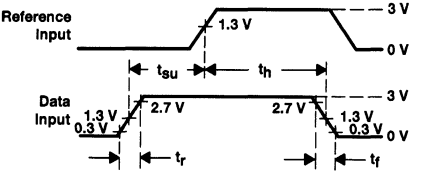
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

These devices contain four independent 2-input exclusive-OR gates. They perform the Boolean function $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

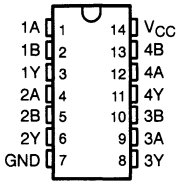
A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

The SN54HC86 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC86 is characterized for operation from –40°C to 85°C.

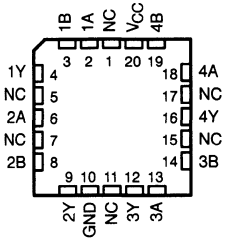
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

SN54HC86 . . . J OR W PACKAGE
SN74HC86 . . . D OR N PACKAGE
(TOP VIEW)

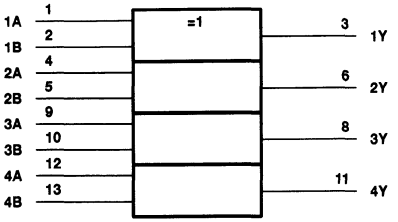


SN54HC86 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

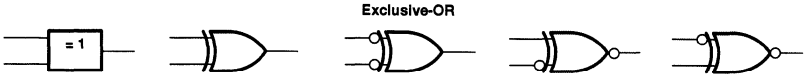
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

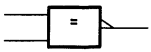
exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



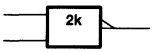
These are five equivalent exclusive-OR symbols valid for an 'HC86 gate in positive logic; negation may be shown at any two ports.

Logic Identity Element



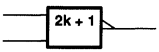
The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

Even-Parity Element



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

Odd-Parity Element



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC86			SN74HC86			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC86		SN74HC86		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			2		40		20	μA
C_i			2 V to 6 V		3	10		10		10	pF

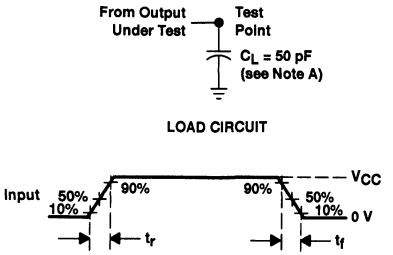
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC86		SN74HC86		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		40	100		150		125	ns
			4.5 V		12	20		30		25	
			6 V		10	17		25		21	
t_t		Y	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

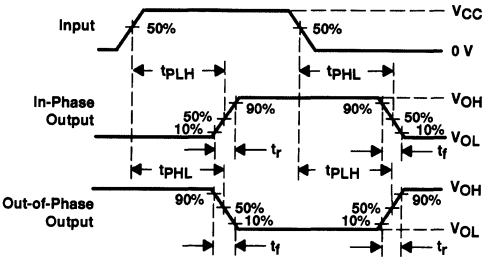
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	35	pF

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

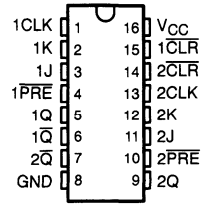
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

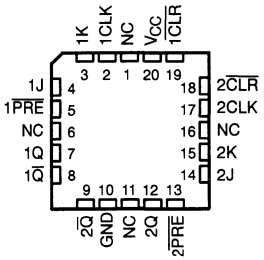
The 'HC112 contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset ($\overline{PRE}$) or clear (CLR) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of CLK. Following the hold-time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops perform as toggle flip-flops by tying J and K high.

The SN54HC112 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC112 is characterized for operation from –40°C to 85°C.

SN54HC112 . . . J OR W PACKAGE
SN74HC112 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC112 . . . FK PACKAGE
(TOP VIEW)



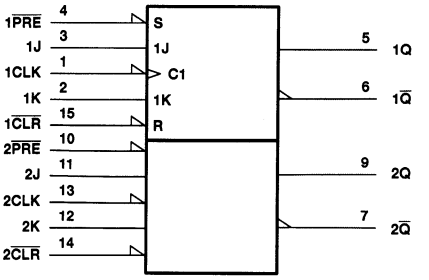
NC – No internal connection

FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_0	$\overline{Q}_0$

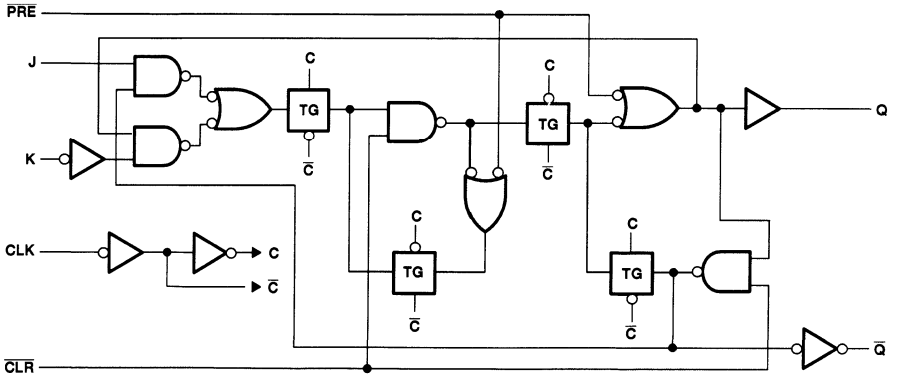
† This configuration is nonstable; that is, it does not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram, each flip-flop (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.3 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC112			SN74HC112			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t‡	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

‡ If this device is used in the threshold region (from V_{IL}max = 0.5 V to V_{IH}min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC112		SN74HC112		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			4		80		40	μA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC112		SN74HC112		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	5	0	3.4	0	4	MHz
			4.5 V	0	25	0	17	0	20	
			6 V	0	29	0	20	0	24	
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		CLK high or low	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		25		21		
t_{su}	Setup time before CLK↓	Data (J, K)	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		25		21		
t_h	Hold time, data after CLK↓		2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		

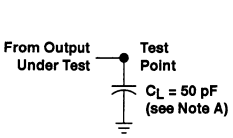
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC112		SN74HC112		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	5	10		3.4		4		MHz
			4.5 V	25	50		17		20		
			6 V	29	60		20		24		
t_{pd}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2 V		54	165		245		205	ns
			4.5 V		16	33		49		41	
			6 V		13	28		42		35	
	CLK	Q or $\overline{Q}$	2 V		56	125		185		155	
			4.5 V		16	25		37		31	
			6 V		13	21		31		26	
t_t		Q or $\overline{Q}$	2 V		29	75		110		95	ns
			4.5 V		9	15		22		19	
			6 V		8	13		19		16	

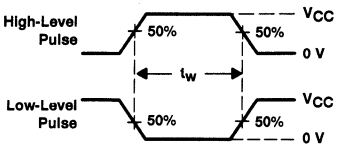
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	No load	35	pF

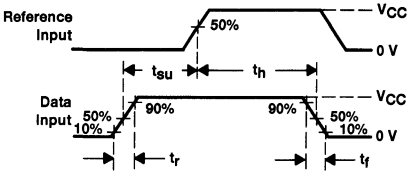
PARAMETER MEASUREMENT INFORMATION



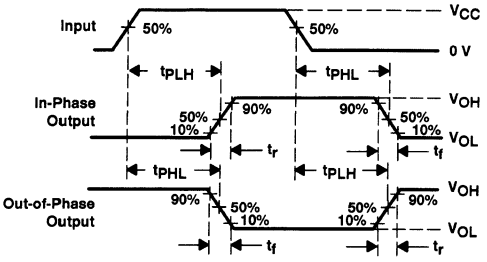
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



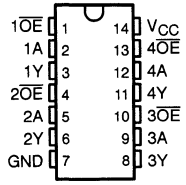
VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

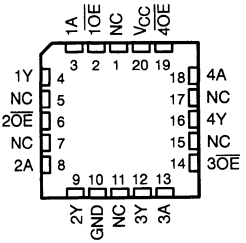
Figure 1. Load Circuit and Voltage Waveforms

- **High-Current 3-State Outputs Interface Directly With System Bus or Can Drive up to 15 LSTTL Loads**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC125 . . . J OR W PACKAGE
SN74HC125 . . . D, DB, OR N PACKAGE
(TOP VIEW)



SN54HC125 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

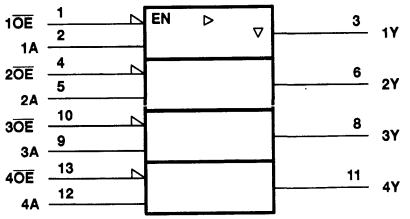
These quadruple bus buffer gates feature independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ($\overline{OE}$) input is high.

The SN54HC125 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC125 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

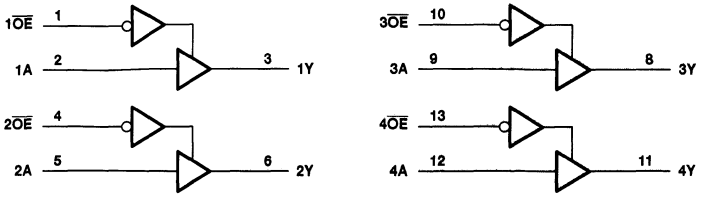
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
DB package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC125			SN74HC125			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC125		SN74HC125		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0		6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC125		SN74HC125		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		48	120		150		150	ns
			4.5 V		14	24		36		30	
			6 V		11	20		25		26	
t_{en}	$\overline{OE}$	Y	2 V		53	120		180		150	ns
			4.5 V		14	24		36		30	
			6 V		11	20		31		26	
t_{dis}	$\overline{OE}$	Y	2 V		30	120		180		150	ns
			4.5 V		15	24		36		30	
			6 V		14	20		31		26	
t_t		Any	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

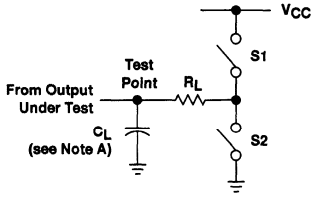
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC125		SN74HC125		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		67	150		225		190	ns
			4.5 V		19	30		45		38	
			6 V		15	25		39		32	
t_{en}	$\overline{OE}$	Y	2 V		100	135		200		170	ns
			4.5 V		20	27		40		34	
			6 V		17	23		34		29	
t_t		Any	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

operating characteristics, T_A = 25°C

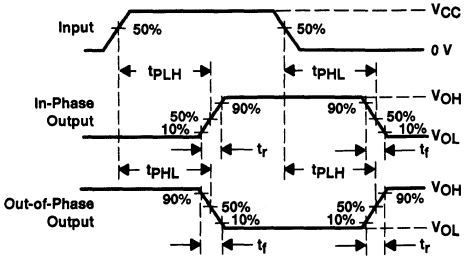
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	45	pF

PARAMETER MEASUREMENT INFORMATION

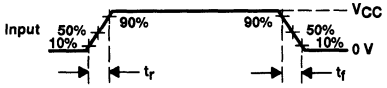


LOAD CIRCUIT

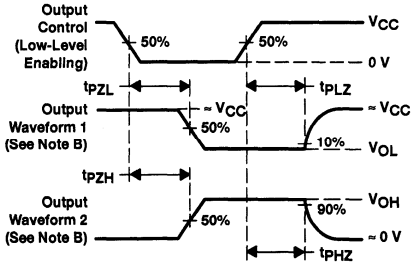
PARAMETER		RL	CL	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



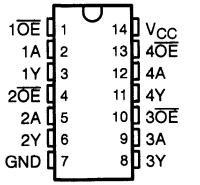
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

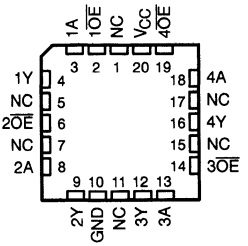
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **High-Current 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HCT125 . . . J OR W PACKAGE
SN74HCT125 . . . D OR N PACKAGE
(TOP VIEW)



SN54HCT125 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

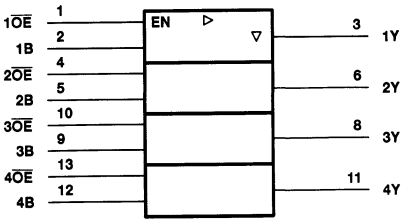
These bus buffer gates feature independent line drivers with 3-state outputs. Each output is disasbled when the associated output-enable ($\overline{OE}$) input is high.

The SN54HCT125 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT125 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

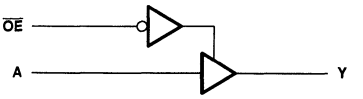
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HCT125			SN74HCT125			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time		0		500	0		500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT125		SN74HCT125		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	4.5 V	4.4	4.499		4.4		4.4		V
		I_{OH} = –6 mA		3.98	4.3		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
		I_{OL} = 6 mA			0.17	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0,	V_I = V_{IH} or V_{IL}	5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}†	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i			4.5 V to 5.5 V		3	10		10*		10	pF

* On products compliant to MIL-STD-883C, Class B, this parameter is not production tested.
† This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT125		SN74HCT125		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5 V		15	26		39		33	ns
			5.5 V		12	23		35		30	
t_{en}	$\overline{OE}$	Y	4.5 V		18	28		42		35	ns
			5.5 V		15	25		38		31	
t_{dis}	$\overline{OE}$	Y	4.5 V		15	26		39		33	ns
			5.5 V		13	23		35		30	
t_t		Any	4.5 V		8	15		22		19	ns
			5.5 V		7	14		21		17	

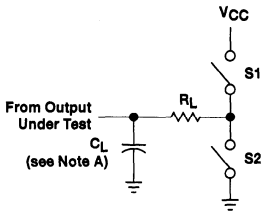
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT125		SN74HCT125		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5 V		19	36		58		46	ns
			5.5 V		16	32		48		42	
t_{en}	$\overline{OE}$	Y	4.5 V		25	40		60		50	ns
			5.5 V		21	35		53		43	
t_t		Any	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

operating characteristics, T_A = 25°C

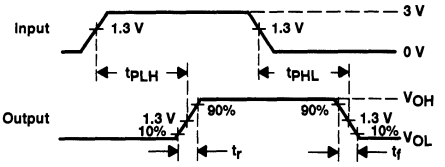
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	35	pF

PARAMETER MEASUREMENT INFORMATION

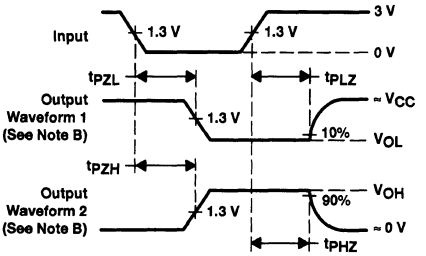


LOAD CIRCUIT

PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



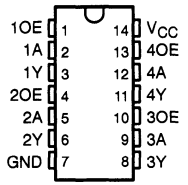
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

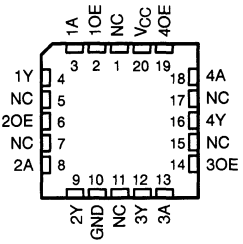
Figure 1. Load Circuit and Voltage Waveforms

- **High-Current 3-State Outputs Interface Directly With System Bus or Can Drive up to 15 LSTTL Loads**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC126 . . . J OR W PACKAGE
SN74HC126 . . . D, DB, OR N PACKAGE
(TOP VIEW)



SN54HC126 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

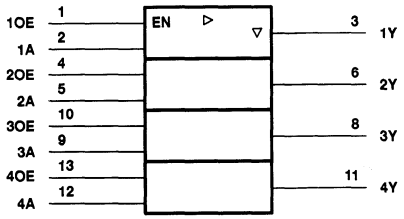
These quadruple bus buffer gates feature independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low.

The SN54HC126 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC126 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

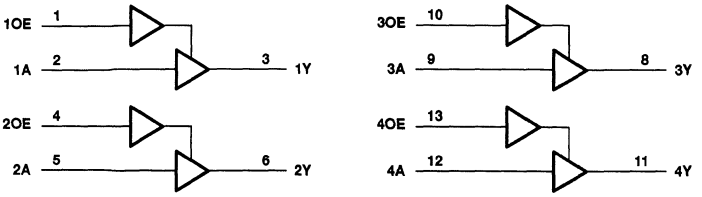
INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC126			SN74HC126			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC126		SN74HC126		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	$V_O = V_{CC}$ or 0		6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	$V_I = V_{CC}$ or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC126		SN74HC126		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		47	120		180		150	ns
			4.5 V		14	24		36		30	
			6 V		11	20		31		26	
t_{en}	OE	Y	2 V		57	120		180		150	ns
			4.5 V		16	24		36		30	
			6 V		12	20		31		26	
t_{dis}	OE	Y	2 V		35	120		180		150	ns
			4.5 V		17	24		36		30	
			6 V		15	20		31		26	
t_t		Any	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

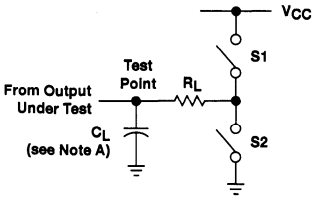
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC126		SN74HC126		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		67	150		225		188	ns
			4.5 V		19	30		45		38	
			6 V		15	25		39		33	
t_{en}	OE	Y	2 V		100	135		202		169	ns
			4.5 V		20	27		40		36	
			6 V		17	23		36		30	
t_t		Any	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

operating characteristics, T_A = 25°C

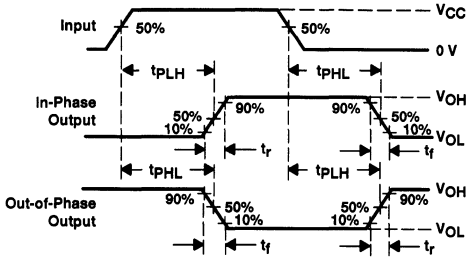
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	45	pF

PARAMETER MEASUREMENT INFORMATION

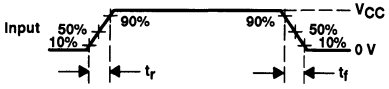


LOAD CIRCUIT

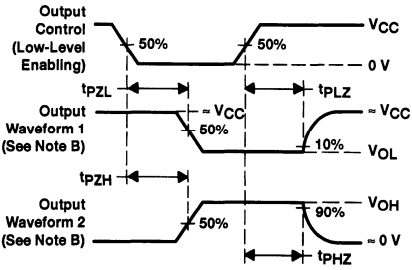
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



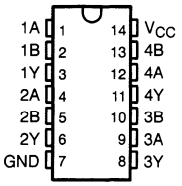
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

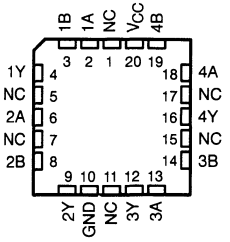
Figure 1. Load Circuit and Voltage Waveforms

- **Operation From Very Slow Input Transitions**
- **Temperature-Compensated Threshold Levels**
- **High Noise Immunity**
- **Same Pinouts as 'HC00**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC132 . . . J OR W PACKAGE
SN74HC132 . . . D, DB, OR N PACKAGE
(TOP VIEW)



SN54HC132 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

Each circuit functions as a NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals. The 'HC132 perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

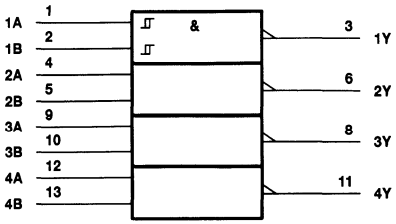
These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

The SN54HC132 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC132 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

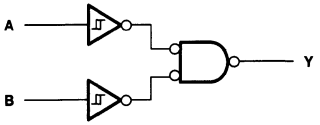
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, and W packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
DB package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC132			SN74HC132			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC132		SN74HC132		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
V_{T+}			2 V	0.7	1.2	1.5	0.7	1.5	0.7	1.5	V
			4.5 V	1.55	2.5	3.15	1.55	3.15	1.55	3.15	
			6 V	2.1	3.3	4.2	2.1	4.2	2.1	4.2	
V_{T-}			2 V	0.3	0.6	1	0.3	1	0.3	1	V
			4.5 V	0.9	1.6	2.45	0.9	2.45	0.9	2.45	
			6 V	1.2	2	3.2	1.2	3.2	1.2	3.2	
$V_{T+} - V_{T-}$			2 V	0.2	0.6	1.2	0.2	1.2	0.2	1.2	V
			4.5 V	0.4	0.9	2.1	0.4	2.1	0.4	2.1	
			6 V	0.5	1.3	2.5	0.5	2.5	0.5	2.5	
I_I	V_I = V_{CC} or 0		6 V			±0.1		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			2		40		20	μA
C_i			2 V to 6 V		3	10		10		10	pF

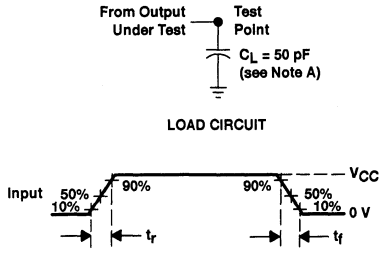
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC132		SN74HC132		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		60	120		186		156	ns
			4.5 V		18	25		37		31	
			6 V		14	21		32		27	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

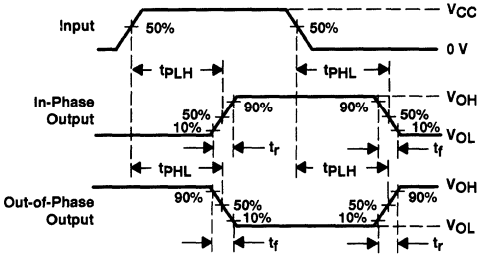
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	20	pF

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

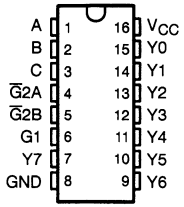
NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

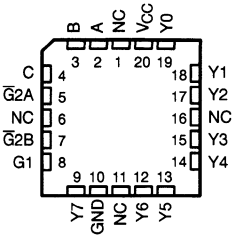
SCLS107B – DECEMBER 1982 – REVISED JULY 1996

- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporate Three Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Plastic Small-Outline (D), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC138 . . . J OR W PACKAGE
SN74HC138 . . . D, N, OR PW PACKAGE
(TOP VIEW)



SN54HC138 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'HC138 are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

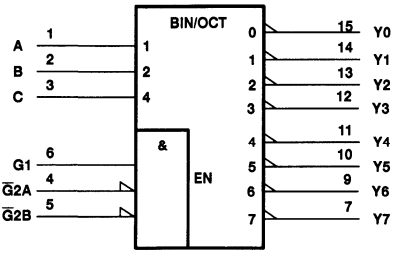
The conditions at the binary-select inputs at the three enable inputs select one of eight output lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

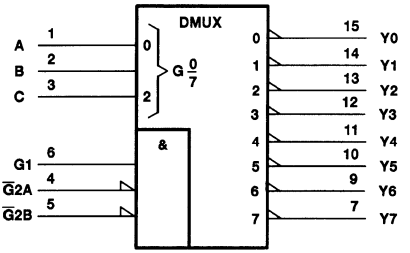
The SN54HC138 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC138 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

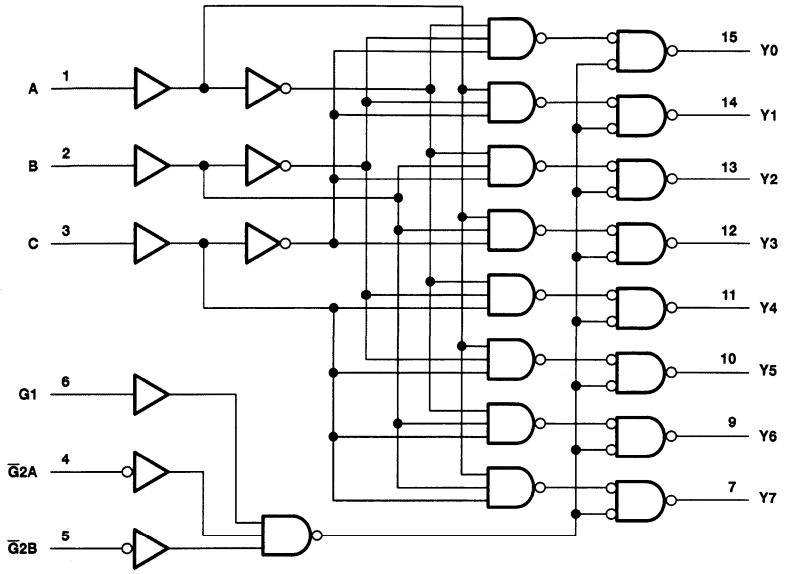
logic symbols (alternatives)†





† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.3 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC138			SN74HC138			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC138		SN74HC138		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

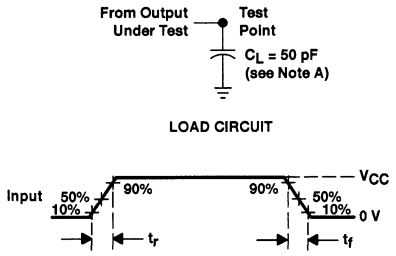
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC138		SN74HC138		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	Any Y	2 V		67	180		270		225	ns
			4.5 V		18	36		54		45	
			6 V		15	31		46		38	
	Enable	Any Y	2 V		66	155		235		195	
			4.5 V		18	31		47		39	
			6 V		15	26		40		33	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

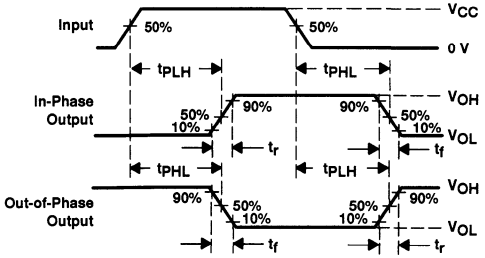
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	85	pF

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

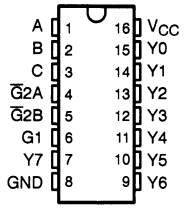
NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

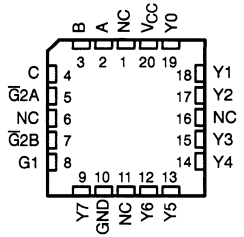
SCLS171B – MARCH 1984 – REVISED JULY 1996

- **Inputs Are TTL-Voltage Compatible**
- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporate Three Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Plastic Small-Outline (D), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HCT138 . . . J OR W PACKAGE
SN74HCT138 . . . D, N, OR PW PACKAGE
(TOP VIEW)



SN54HCT138 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'HCT138 are designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

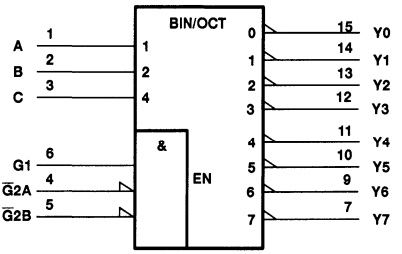
The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low ($\overline{G}$) and one active-high (G) enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

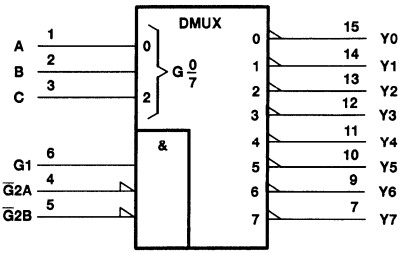
The SN54HCT138 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT138 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

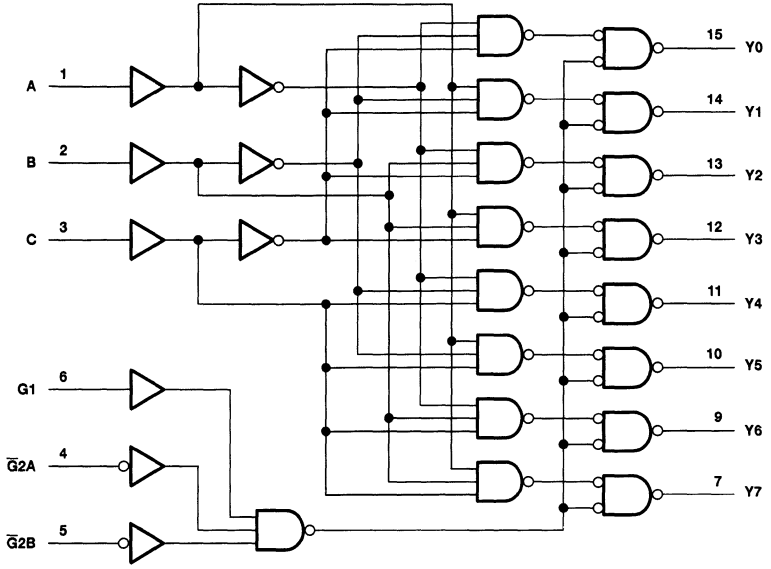
logic symbols (alternatives)†





† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HCT138			SN74HCT138			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time		0		500	0		500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT138		SN74HCT138		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	4.5 V	4.4	4.499		4.4		4.4		V
		I_{OH} = –4 mA		3.98	4.3		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
		I_{OL} = 4 mA			0.17	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}†	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i			4.5 V to 5.5 V		3	10		10		10	pF

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

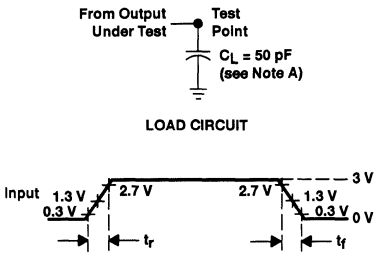
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

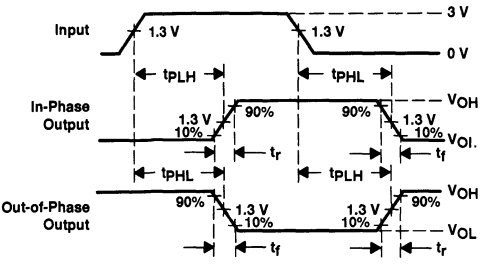
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT138		SN74HCT138		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	Any Y	4.5 V		23	36		54		45	ns
			5.5 V		17	32		49		34	
	Enable	Any Y	4.5 V		22	33		50		42	
			5.5 V		18	30		45		38	
t_t		Y	4.5 V		12	15		22		19	ns
			5.5 V		11	14		20		17	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	85	pF

PARAMETER MEASUREMENT INFORMATION





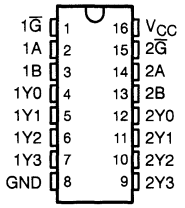
NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

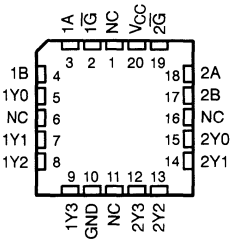
SCLS108A – DECEMBER 1982 – REVISED JANUARY 1996

- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporate Two Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Plastic Small-Outline (D), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC139 . . . J OR W PACKAGE
SN74HC139 . . . D, N, OR PW PACKAGE
(TOP VIEW)



SN54HC139 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'HC139 are designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay time of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

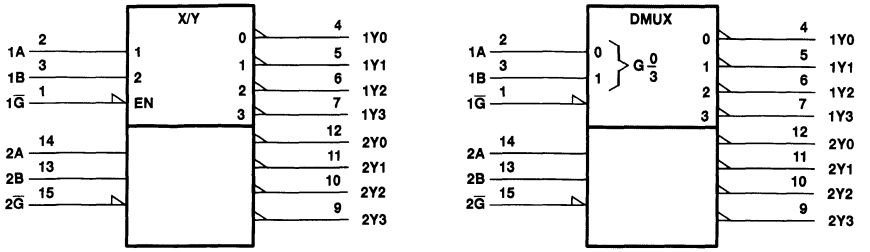
The 'HC139 comprise two individual 2-line to 4-line decoders in a single package. The active-low enable ($\overline{G}$) input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

The SN54HC139 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC139 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

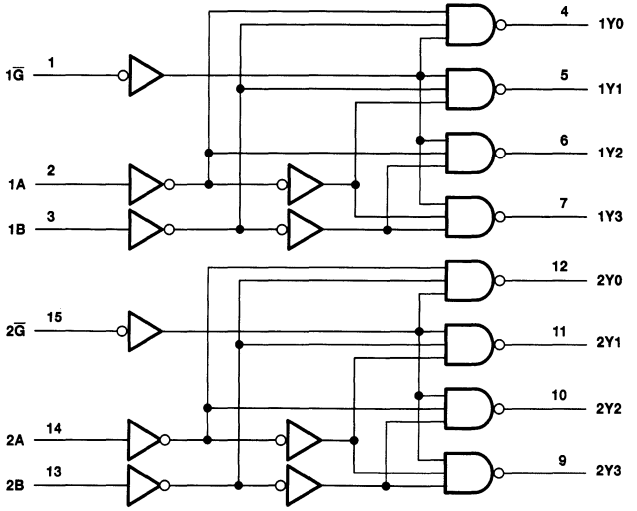
INPUTS			OUTPUTS			
$\overline{G}$	SELECT					
	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

logic symbols (alternatives)†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.3 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC139			SN74HC139			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC139		SN74HC139		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

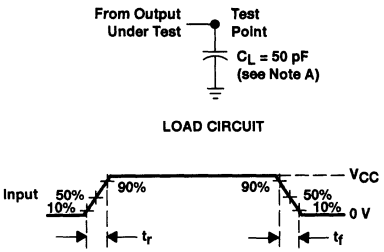
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC139		SN74HC139		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		47	175		255		220	ns
			4.5 V		14	35		51		44	
			6 V		12	30		44		38	
	$\overline{G}$	Y	2 V		39	175		255		220	
			4.5 V		11	35		51		44	
			6 V		10	30		44		38	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

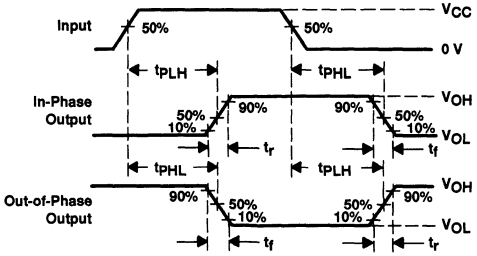
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per decoder	No load	25	pF

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

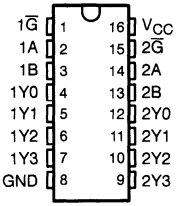
NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

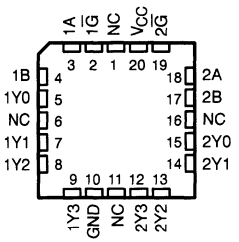
SCLS066A – MARCH 1982 – REVISED JANUARY 1996

- **Inputs Are TTL-Voltage Compatible**
- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporate Two Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HCT139 . . . J OR W PACKAGE
SN74HCT139 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54HCT139 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'HCT139 are designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay time of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

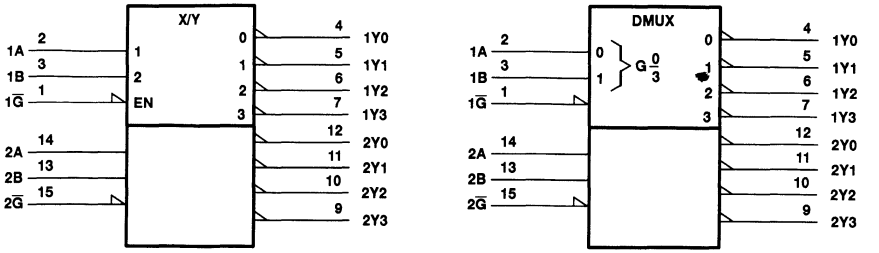
The 'HCT139 comprise two individual 2-line to 4-line decoders in a single package. The active-low enable ($\overline{G}$) input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

The SN54HCT139 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT139 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

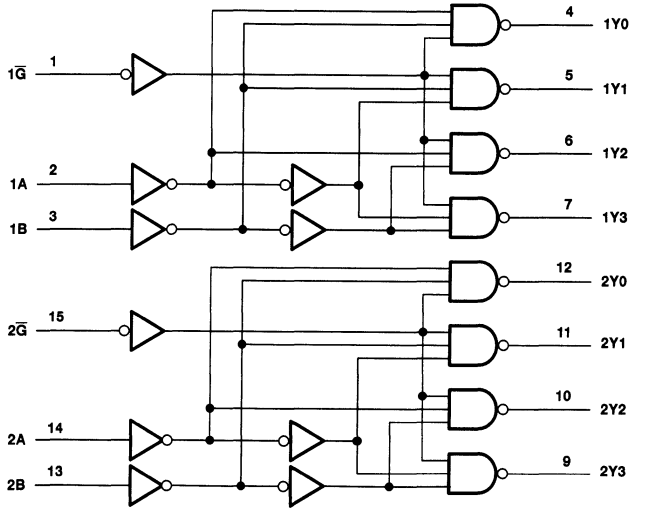
INPUTS			OUTPUTS			
$\overline{G}$	SELECT					
	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

logic symbols (alternatives)†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.3 W
DB package ..... 0.55 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HCT139			SN74HCT139			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time		0		500	0		500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT139		SN74HCT139		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 μA	4.5 V	4.4	4.499		4.4		4.4		V
		I_{OH} = –4 mA		3.98	4.3		3.7		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
		I_{OL} = 4 mA			0.17	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0,	I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i			4.5 V to 5.5 V		3	10		10		10	pF

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

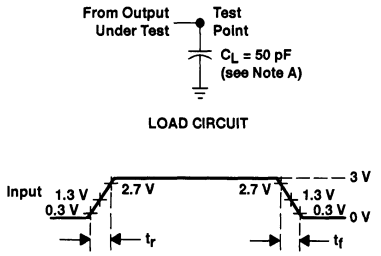
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

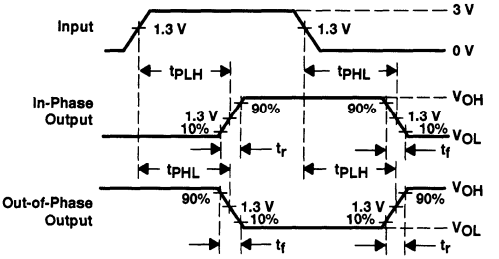
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT139		SN74HCT139		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	4.5 V		14	34		51		43	ns
			5.5 V		12	30		50		40	
	$\overline{G}$	Y	4.5 V		11	34		51		43	
			5.5 V		10	30		50		40	
t_t		Y	4.5 V		8	15		22		19	ns
			5.5 V		6	14		21		17	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per decoder	No load	25	pF

PARAMETER MEASUREMENT INFORMATION



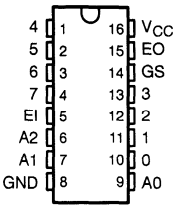


NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

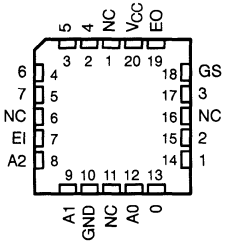
Figure 1. Load Circuit and Voltage Waveforms

- **Encode Eight Data Lines to 3-Line Binary (Octal)**
- **Applications Include:**
  - **n-Bit Encoding**
  - **Code Converters and Generators**
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC148 . . . J OR W PACKAGE
SN74HC148 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC148 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

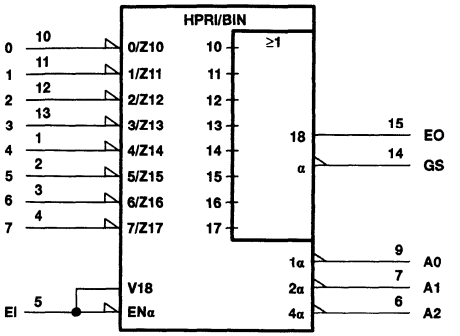
The 'HC148 feature priority decoding of the inputs to ensure that only the highest-order data line is encoded. These devices encode eight data lines to 3-line (4-2-1) binary (octal). Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion without the need for external circuitry. Data inputs and outputs are active at the low logic level.

The SN54HC148 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC148 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

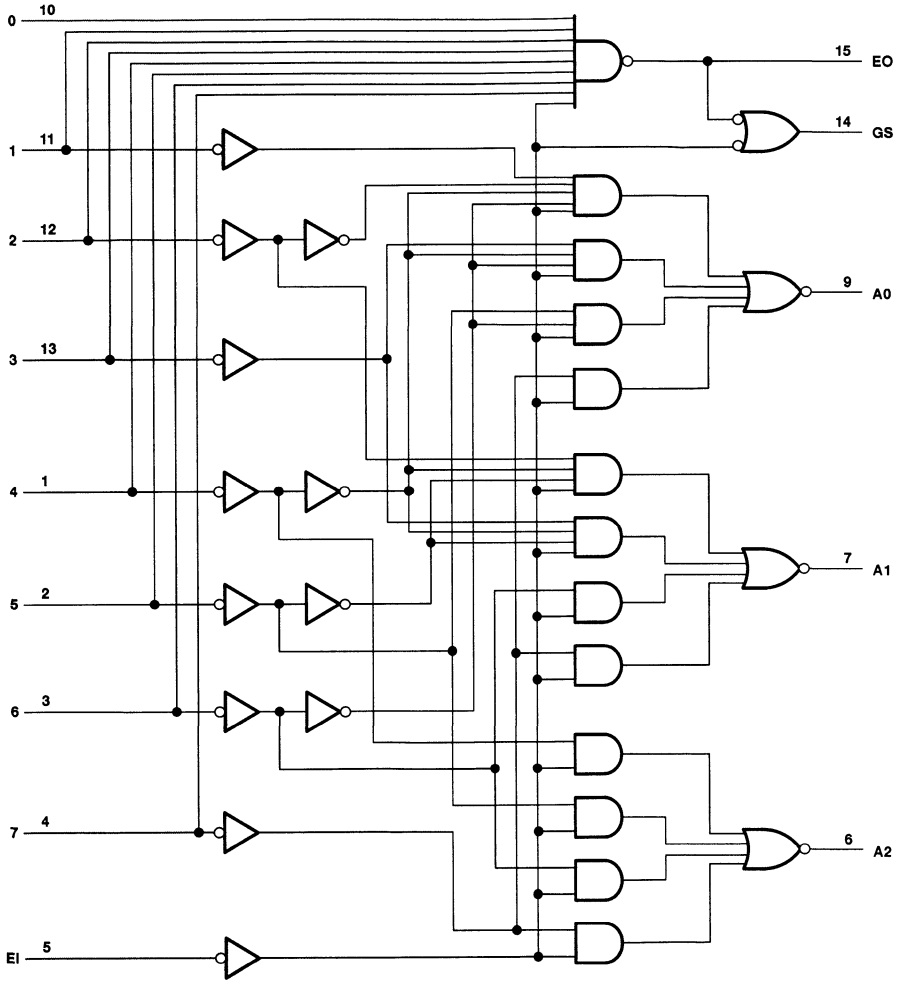
INPUTS									OUTPUTS				
EI	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**A2**	**A1**	**A0**	**GS**	**EO**
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC148			SN74HC148			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC148		SN74HC148		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

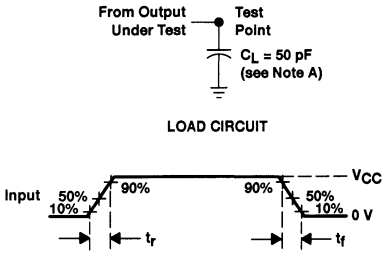
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC148		SN74HC148		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	1–7	A0, A1, or A2	2 V		69	180		270		225	ns
			4.5 V		23	36		54		45	
			6 V		21	31		46		38	
	0–7	EO	2 V		60	150		225		190	
			4.5 V		20	30		45		38	
			6 V		17	26		38		33	
		GS	2 V		75	190		285		240	
			4.5 V		25	38		57		48	
			6 V		21	32		48		41	
	EI	A0, A1, or A2	2 V		78	195		295		245	
			4.5 V		26	39		59		49	
			6 V		22	33		50		42	
		GS	2 V		57	145		220		180	
			4.5 V		19	29		44		36	
			6 V		16	25		38		31	
		EO	2 V		66	165		250		205	
			4.5 V		22	33		50		41	
			6 V		19	28		43		35	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

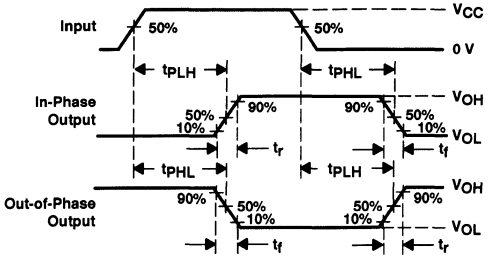
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	35	pF

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

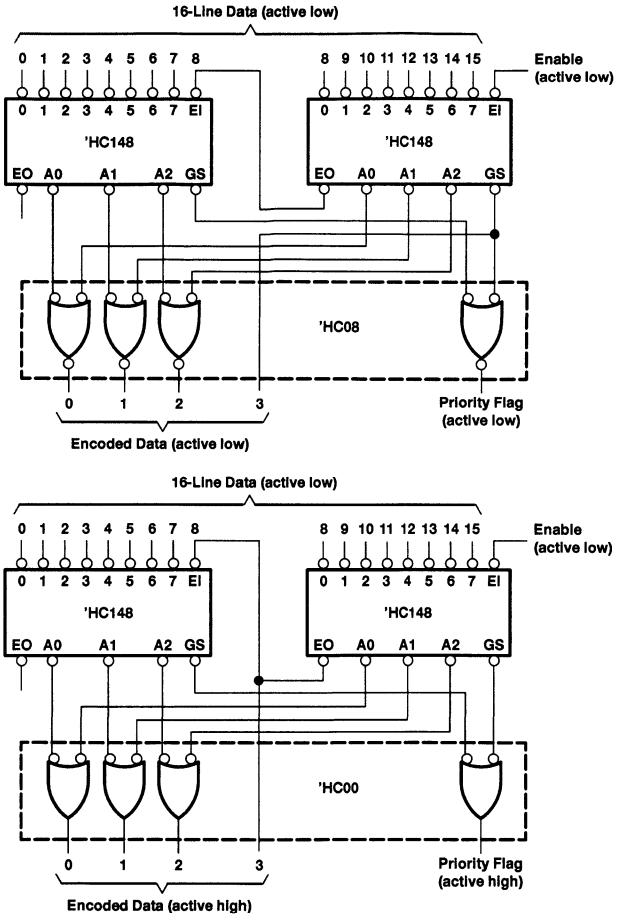


Figure 2. Priority Encoder for 16 Bits

Since the 'HC148 is a combinational logic circuit, wrong addresses can appear during input transients. Moreover, a change from high to low at EI can cause a transient low on GS when all inputs are high. This must be considered when strobing the outputs.

SCLS110B – DECEMBER 1982 – JULY 1996

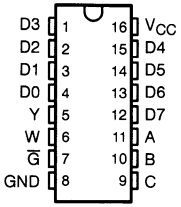
- **8-Line to 1-Line Multiplexers Can Perform as:**
  - **Boolean Function Generators**
  - **Parallel-to-Serial Converters**
  - **Data Source Selectors**
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

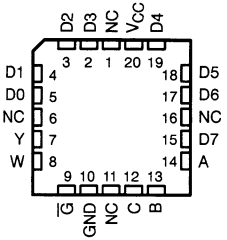
These monolithic data selectors/multiplexers provide full binary decoding to select one of eight data sources. The strobe ($\overline{G}$) input must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the W output high and the Y output low.

The SN54HC151 is characterized for operation over the full military temperature range of –55°C to125°C. The SN74HC151 is characterized for operation from –40°C to 85°C.

SN54HC151 . . . J OR W PACKAGE
SN74HC151 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC151 . . . FK PACKAGE
(TOP VIEW)



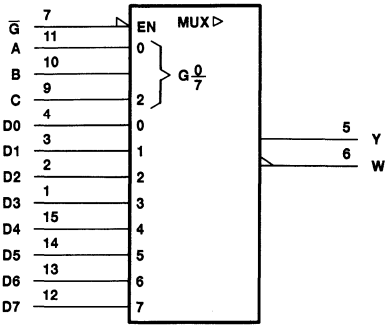
NC – No internal connection

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	$\overline{G}$	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

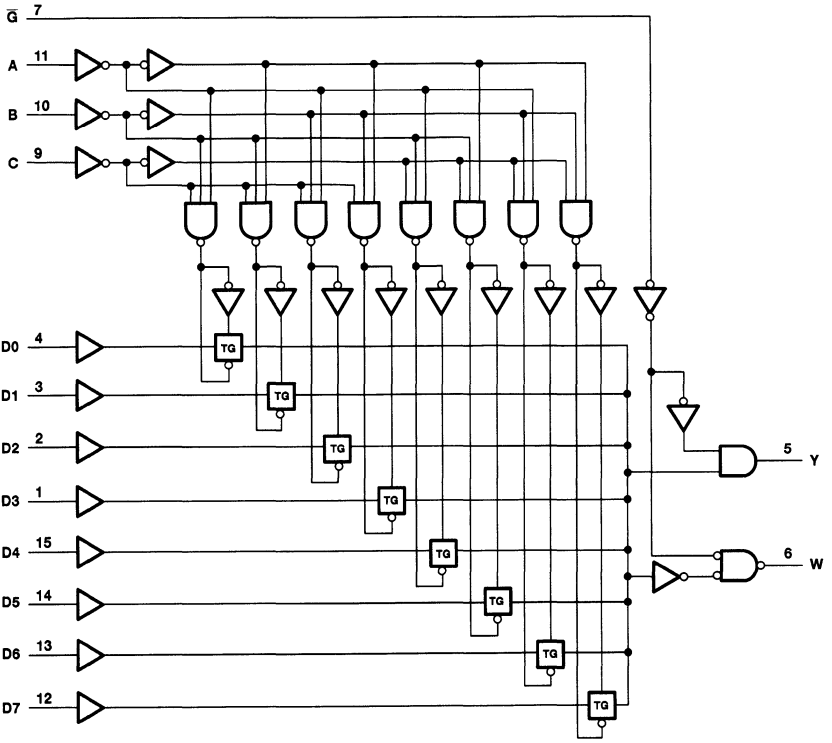
D0, D1 . . . D7 = the level of the respective D input

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC151			SN74HC151			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC151		SN74HC151		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC151		SN74HC151		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y or W	2 V		94	250		360		312	ns
			4.5 V		30	50		73		63	
			6 V		25	43		62		54	
	Any D	Y or W	2 V		74	195		283		244	
			4.5 V		23	39		57		49	
			6 V		20	33		48		41	
	$\overline{G}$	Y or W	2 V		49	127		185		159	
			4.5 V		15	25		37		32	
			6 V		13	22		32		28	
t_t		Y or W	2 V		22	75		110		95	ns
			4.5 V		9	15		22		19	
			6 V		8	13		19		16	

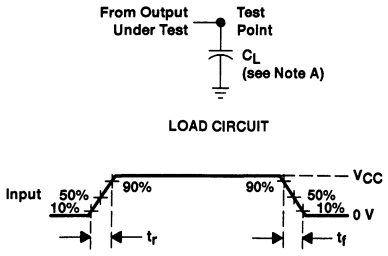
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC151		SN74HC151		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y or W	2 V		107	350		525		440	ns
			4.5 V		33	70		105		88	
			6 V		30	59		89		76	
	Any D	Y or W	2 V		90	275		415		345	
			4.5 V		29	51		83		69	
			6 V		25	47		72		59	
	$\overline{G}$	Y or W	2 V		67	205		310		255	
			4.5 V		21	41		62		51	
			6 V		18	35		53		43	
t_t		Y or W	2 V		51	210		315		265	ns
			4.5 V		16	42		63		53	
			6 V		14	36		53		45	

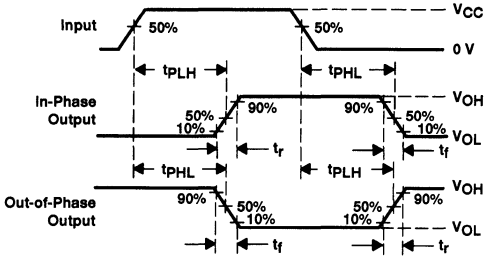
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	70	pF

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

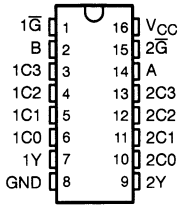
NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

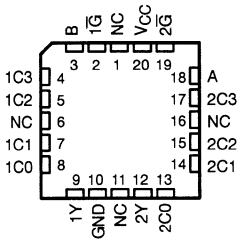
SCLS112A – DECEMBER 1982 – REVISED JANUARY 1996

- **Permit Multiplexing from n Lines to One Line**
- **Perform Parallel-to-Serial Conversion**
- **Strobe (Enable) Line Provided for Cascading (N Lines to n Lines)**
- **Package Options Include Plastic Small-Outline (D), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC153 . . . J OR W PACKAGE
SN74HC153 . . . D, N, OR PW PACKAGE
(TOP VIEW)



SN54HC153 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate strobe ($\overline{G}$) inputs are provided for each of the two 4-line sections.

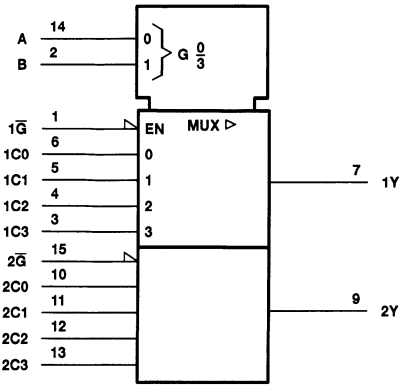
The SN54HC153 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC153 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS							OUTPUT
SELECT†		DATA				$\overline{G}$	Y
B	A	C0	C1	C2	C3		
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

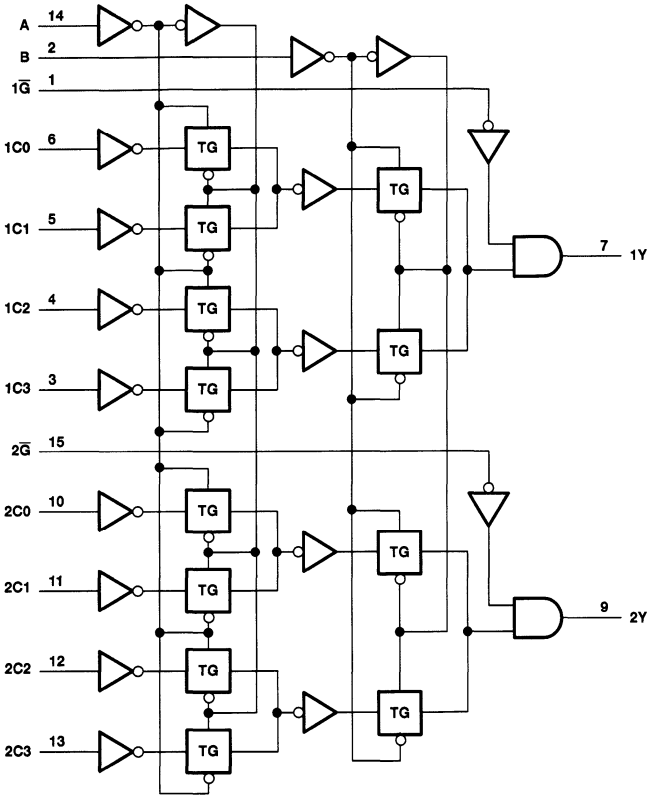
† Select inputs A and B are common to both sections.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC153			SN74HC153			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC153		SN74HC153		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC153		SN74HC153		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		90	150		225		190	ns
			4.5 V		21	30		45		38	
			6 V		17	26		38		32	
	Data (Any C)	Y	2 V		73	126		189		158	
			4.5 V		17	28		42		35	
			6 V		14	23		35		29	
	$\overline{G}$	Y	2 V		38	95		150		125	
			4.5 V		11	19		28		24	
			6 V		9	16		24		20	
t_t		Y	2 V		20	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

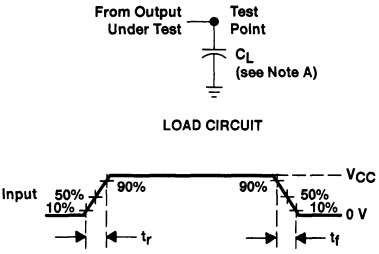
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC153		SN74HC153		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		105	235		355		295	ns
			4.5 V		27	47		71		59	
			6 V		21	41		60		51	
	Data (Any C)	Y	2 V		93	220		335		274	
			4.5 V		23	44		67		55	
			6 V		19	38		57		48	
	$\overline{G}$	Y	2 V		60	185		280		230	
			4.5 V		17	37		56		46	
			6 V		14	32		48		40	
t_t		Y	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

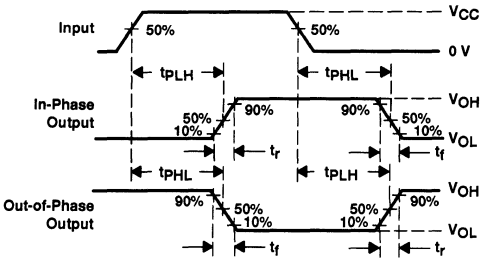
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per multiplexer	No load	40	pF

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



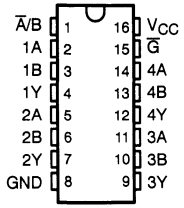
VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

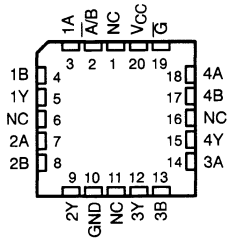
Figure 1. Load Circuit and Voltage Waveforms

- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC157 . . . J OR W PACKAGE
SN74HC157 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC157 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

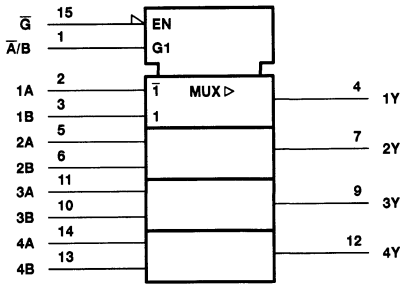
These monolithic data selectors/multiplexers contain inverters and drivers to supply full data selection to the four output gates. A separate strobe ($\overline{G}$) input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The 'HC157 present true data.

The SN54HC157 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC157 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

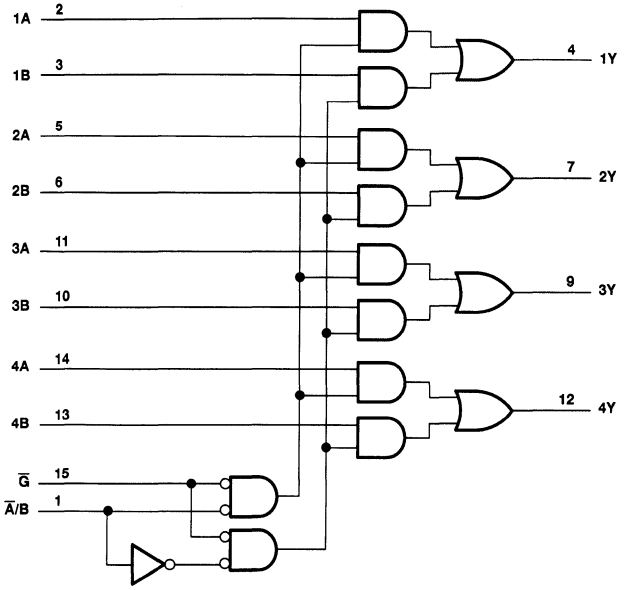
INPUTS				OUTPUT
$\overline{G}$	SELECT $\overline{A}$/B	DATA A	DATA B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC157			SN74HC157			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC157		SN74HC157		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC157		SN74HC157		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		63	125		190		160	ns
			4.5 V		13	25		38		32	
			6 V		11	21		32		27	
	$\overline{A}$/B	Y	2 V		67	125		190		160	
			4.5 V		18	25		38		31	
			6 V		14	21		32		27	
	$\overline{G}$	Y	2 V		59	115		170		145	
			4.5 V		16	23		34		29	
			6 V		13	20		29		25	
t_t		Y	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

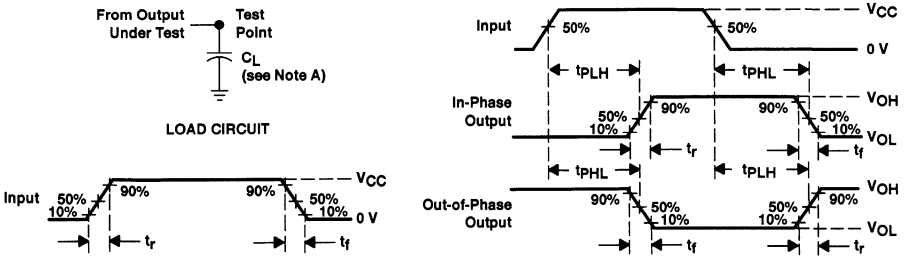
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC157		SN74HC157		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		81	190		290		235	ns
			4.5 V		23	38		58		47	
			6 V		18	33		49		41	
	$\overline{A}$/B	Y	2 V		81	210		320		260	
			4.5 V		23	42		64		52	
			6 V		18	36		54		45	
	$\overline{G}$	Y	2 V		91	190		290		235	
			4.5 V		24	38		58		47	
			6 V		18	33		49		41	
t_t		Y	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	40	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

SN54HCT157, SN74HCT157
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

SCLS071A – NOVEMBER 1988 – REVISED MARCH 1996

- **Inputs Are TTL-Voltage Compatible**
- **Buffered Inputs and Outputs**
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

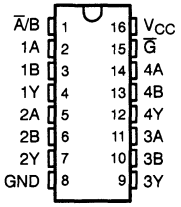
These monolithic data selectors/multiplexers contain inverters and drivers to supply full data selection to the four output gates. A separate strobe ($\overline{G}$) input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs.

The SN54HCT157 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT157 is characterized for operation from –40°C to 85°C.

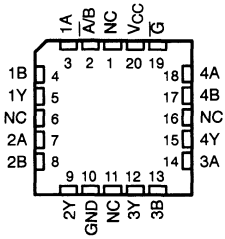
FUNCTION TABLE

INPUTS				OUTPUT
STROBE $\overline{G}$	SELECT $\overline{A}$/B	DATA A	DATA B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

SN54HCT157 . . . J OR W PACKAGE
SN74HCT157 . . . D OR N PACKAGE
(TOP VIEW)

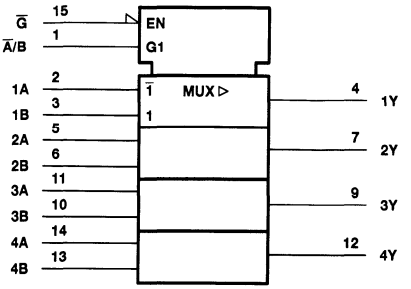


SN54HCT157 . . . FK PACKAGE
(TOP VIEW)



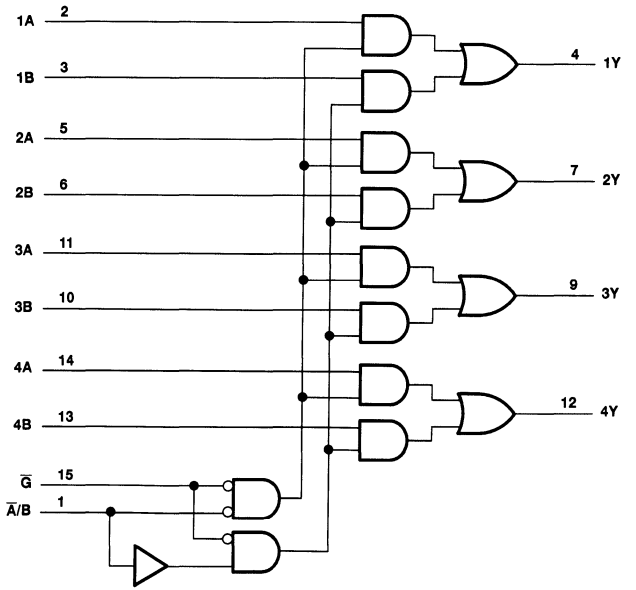
NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HCT157			SN74HCT157			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time		0		500	0		500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT157		SN74HCT157		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 μA	4.5 V	4.4	4.499		4.4		4.4		V
		I_{OH} = –6 mA		3.98	4.3		3.7		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
		I_{OL} = 6 mA			0.17	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0		5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i			4.5 V to 5.5 V		3	10		10*		10	pF

* On products compliant to MIL-STD-883C, Class B, this parameter is not production tested.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT157		SN74HCT157		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	4.5 V		18	28		42		35	ns
			5.5 V		15	25		38		32	
	$\overline{A}$/B	Y	4.5 V		20	32		48		40	
			5.5 V		17	29		43		36	
	$\overline{G}$	Y	4.5 V		18	26		39		33	
			5.5 V		15	23		35		30	
t_t		Any	4.5 V		8	15		22		19	ns
			5.5 V		7	14		21		17	

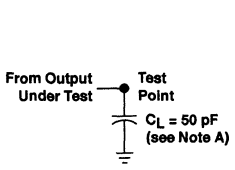
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT157		SN74HCT157		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	4.5 V		23	42		63		52	ns
			5.5 V		19	38		52		46	
	$\overline{A}$/B	Y	4.5 V		24	46		72		58	
			5.5 V		21	41		61		52	
	$\overline{G}$	Y	4.5 V		21	39		58		48	
			5.5 V		19	35		49		43	
t_t		Any	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

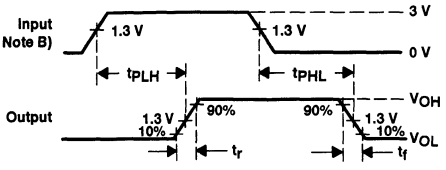
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	12	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

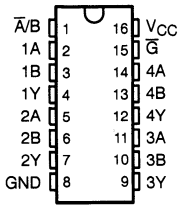
These monolithic data selectors/multiplexers contain inverters and drivers to supply full data selection to the four output gates. A separate strobe ($\overline{G}$) input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The 'HC158 present inverted data.

The SN54HC158 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC158 is characterized for operation from –40°C to 85°C.

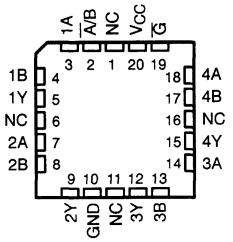
FUNCTION TABLE

INPUTS				OUTPUT
$\overline{G}$	SELECT $\overline{A}$/B	DATA A	DATA B	Y
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

SN54HC158 . . . J OR W PACKAGE
SN74HC158 . . . D OR N PACKAGE
(TOP VIEW)

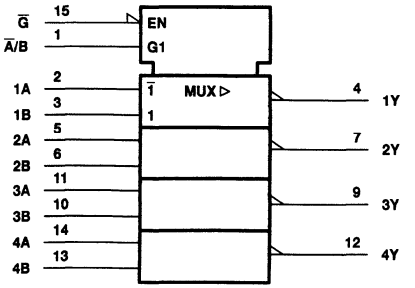


SN54HC158 . . . FK PACKAGE
(TOP VIEW)



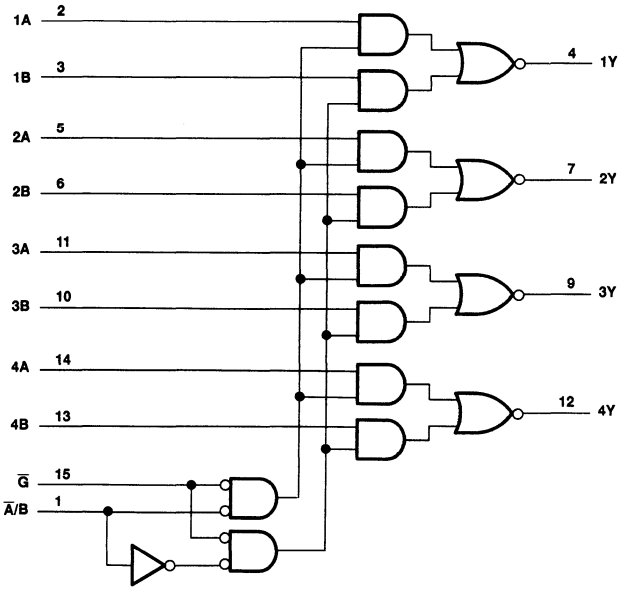
NC – No internal connection

logic symbol†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC158			SN74HC158			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC158		SN74HC158		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC158		SN74HC158		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		63	125		190		160	ns
			4.5 V		13	25		38		32	
			6 V		11	21		32		27	
	$\overline{A}$/B	Y	2 V		67	125		190		160	
			4.5 V		18	25		38		31	
			6 V		14	21		32		27	
	$\overline{G}$	Y	2 V		59	115		170		145	
			4.5 V		16	23		34		29	
			6 V		13	20		29		25	
t_t		Y	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

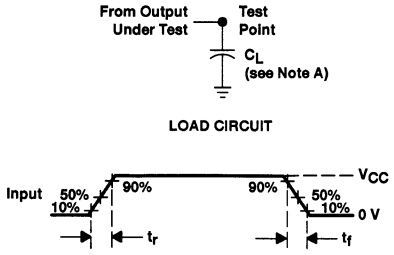
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC158		SN74HC158		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		81	190		290		235	ns
			4.5 V		23	38		58		47	
			6 V		18	33		49		41	
	$\overline{A}$/B	Y	2 V		81	210		320		260	
			4.5 V		23	42		64		52	
			6 V		18	36		54		45	
	$\overline{G}$	Y	2 V		91	190		290		235	
			4.5 V		24	38		58		47	
			6 V		18	33		49		41	
t_t		Y	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

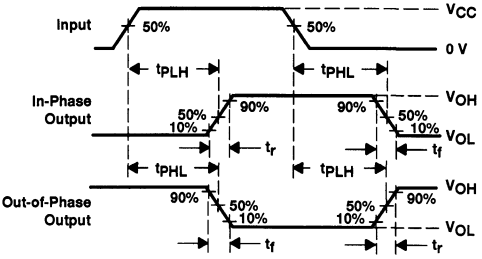
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	40	pF

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



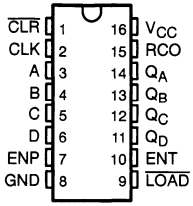
VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

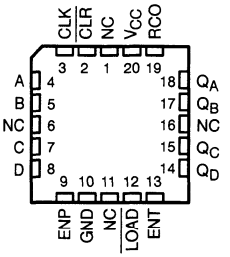
Figure 1. Load Circuit and Voltage Waveforms

- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Synchronous Counting**
- **Synchronously Programmable**
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC161 . . . J OR W PACKAGE
SN74HC161 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC161 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 'HC161 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with synchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, they can be preset to any number between 0 and 9 or 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

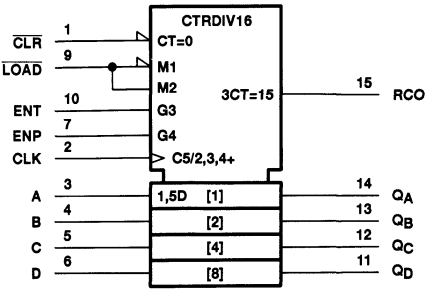
The clear function for the 'HC161 is asynchronous. A low level at the clear ($\overline{CLR}$) input sets all four of the flip-flop outputs low, regardless of the levels of the CLK, load ($\overline{LOAD}$), or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are ENP, ENT, and a ripple-carry (RCO) output. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. Enabling RCO produces a high-level pulse while the count is maximum (9 or 15 with Q_A high). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{LOAD}$) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

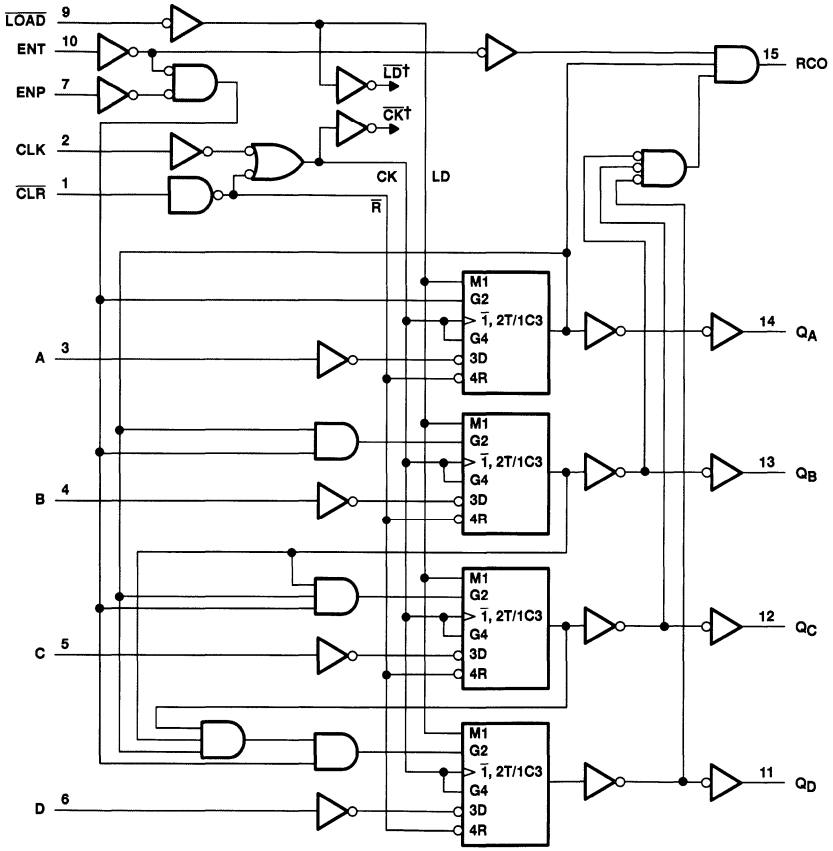
The SN54HC161 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC161 is characterized for operation from –40°C to 85°C.

logic symbol†



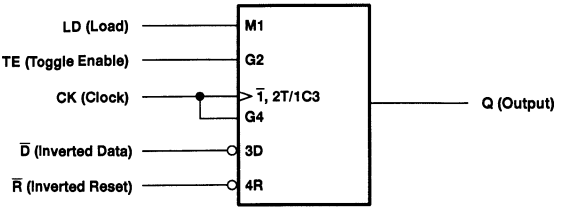
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)

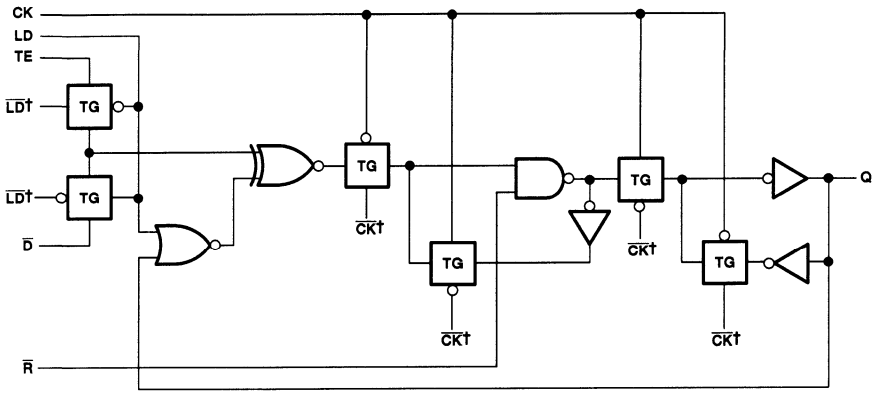


† For simplicity, routing of complementary signals $\overline{LD}$ and $\overline{CK}$ is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.
Pin numbers shown are for the D, J, N, and W packages.

logic symbol, each D/T flip-flop



logic diagram, each D/T flip-flop (positive logic)

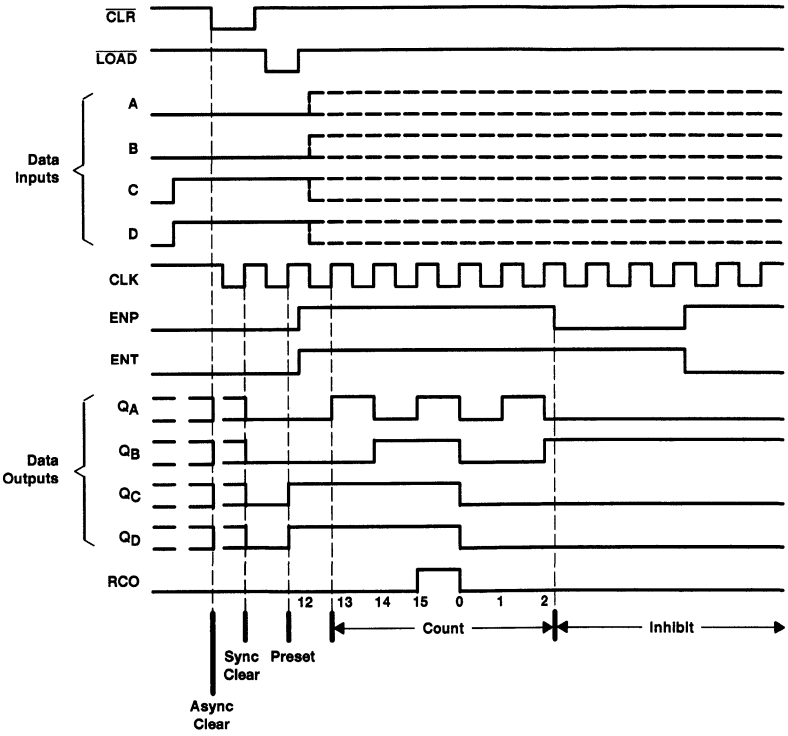


† The origins of $\overline{LD}$ and $\overline{CK}$ are shown in the logic diagram of the overall device.

typical clear, preset, count, and inhibit sequence

The following sequence is illustrated below:

1. Clear outputs to zero (asynchronous)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC161			SN74HC161			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t‡	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

‡ If this device is used in the threshold region (from V_{IL}max = 0.5 V to V_{IH}min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC161		SN74HC161		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC161		SN74HC161		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	2 V	0	6	0	4.2	0	5	MHz
		4.5 V	0	31	0	21	0	25	
		6 V	0	36	0	25	0	29	
t_w	Pulse duration, CLK high or low	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
	Pulse duration, $\overline{CLR}$ low	2 V	80		120		100		
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su}	Setup time before CLK↑, A, B, C, or D	2 V	150		225		190		ns
		4.5 V	30		45		38		
		6 V	26		38		32		
	Setup time before CLK↑, $\overline{LOAD}$ low	2 V	135		205		170		
		4.5 V	27		41		34		
		6 V	23		35		29		
	Setup time before CLK↑, ENP, ENT	2 V	170		255		215		
		4.5 V	34		51		43		
		6 V	29		43		37		
	Setup time before CLK↑, $\overline{CLR}$ inactive	2 V	125		190		155		
		4.5 V	25		38		31		
		6 V	21		32		26		
t_h	Hold time, all synchronous inputs after CLK↑	2 V	0		0		0		ns
		4.5 V	0		0		0		
		6 V	0		0		0		

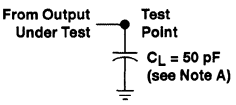
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC161		SN74HC161		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	14		4.2		5		MHz
			4.5 V	31	40		21		25		
			6 V	36	44		25		29		
t_{pd}	CLK	RCO	2 V		83	215		325		270	ns
			4.5 V		24	43		65		54	
			6 V		20	37		55		46	
		Any Q	2 V		80	205		310		255	
			4.5 V		25	41		62		51	
			6 V		21	35		53		43	
	ENT	RCO	2 V		62	195		295		245	
			4.5 V		17	39		59		49	
			6 V		14	33		50		42	
t_{PHL}	$\overline{CLR}$	Any Q	2 V		105	210		315		265	ns
			4.5 V		21	42		63		53	
			6 V		18	36		54		45	
		RCO	2 V		110	220		330		275	
			4.5 V		22	44		66		55	
			6 V		19	37		56		47	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

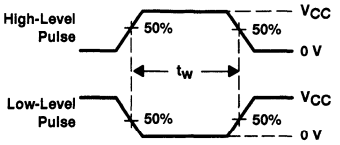
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	60	pF

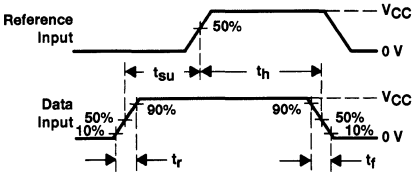
PARAMETER MEASUREMENT INFORMATION



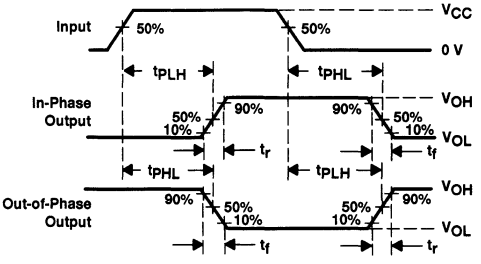
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

n-bit synchronous counters

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 'HC161 count in binary. Virtually any count mode (modulo-N, N_1-to-N_2, N_1-to-maximum) can be used with this fast look-ahead circuit.

The application circuit shown in Figure 2 is not valid for clock frequencies above 18 MHz (at 25°C and 4.5-V V_{CC}). The reason for this is that there is a glitch that is produced on the second stage's RCO and every succeeding stage's RCO. This glitch is common to all HC vendors that Texas Instruments has evaluated, in addition to the bipolar equivalents (LS, ALS, AS).

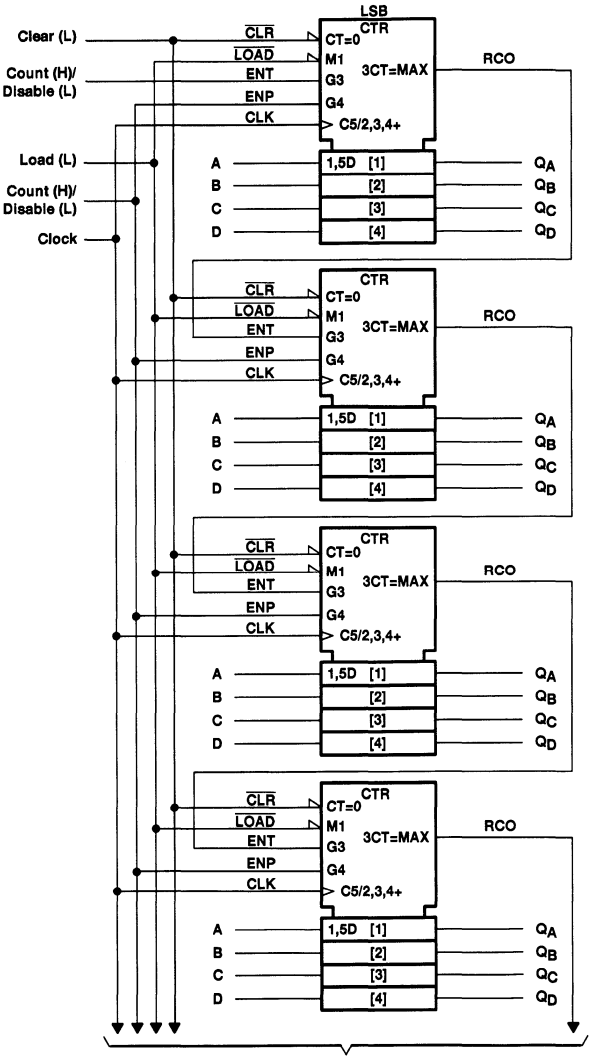

LSB
Clear (L)
Count (H)/
Disable (L)
Load (L)
Count (H)/
Disable (L)
Clock
CLR
LOAD
ENT
ENP
CLK
CTR
CT=0
M1
G3
G4
C5/2,3,4+
3CT=MAX
RCO
A
B
C
D
1,5D [1]
[2]
[3]
[4]
QA
QB
QC
QD
To More Significant Stages

Figure 2

The glitch on RCO is caused because the propagation delay of the rising edge of Q_A of the second stage is shorter than the propagation delay of the falling edge of ENT. RCO is the product of ENT, Q_A, Q_B, Q_C, and Q_D (ENT × Q_A × Q_B × Q_C × Q_D). The resulting glitch is about 7–12 ns in duration. Figure 3 shows the condition in which the glitch occurs. For simplicity, only two stages are being considered, but the results can be applied to other stages. Q_B, Q_C, and Q_D of the first and second stage are at logic one, and Q_A of both stages are at logic zero (1110 1110) after the first clock pulse. On the rising edge of the second clock pulse, Q_A and RCO of the first stage go high. On the rising edge of the third clock pulse, Q_A and RCO of the first stage return to a low level, and Q_A of the second stage goes to a high level. At this time, the glitch on RCO of the second stage appears because of the race condition inside the chip.

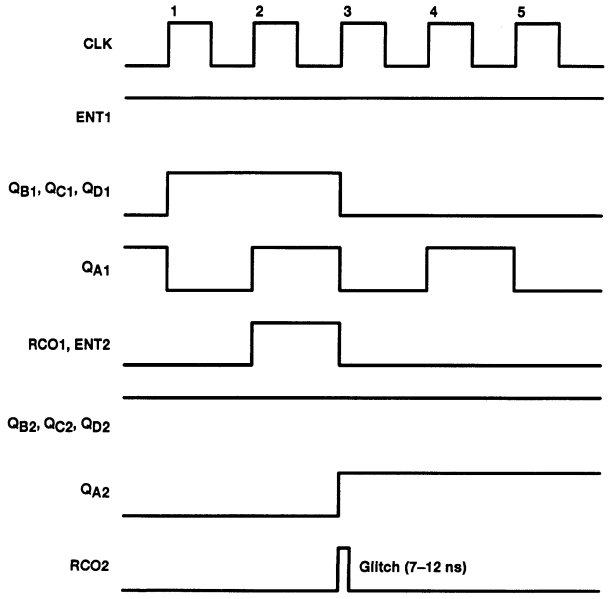


Figure 3

The glitch causes a problem in the next stage (stage three) if the glitch is still present when the next rising clock edge appears (clock pulse 4). To ensure that this does not happen, the clock frequency must be less than the inverse of the sum of the clock-to-RCO propagation delay and the glitch duration (t_g). In other words, $f_{max} = 1/(t_{pd}$ CLK-to-RCO + $t_g)$. For example, at 25°C at 4.5-V V_{CC}, the clock-to-RCO propagation delay is 43 ns and the maximum duration of the glitch is 12 ns. Therefore, the maximum clock frequency that the cascaded counters can use is 18 MHz. The following tables contain the f_{clock}, t_w, and f_{max} specifications for applications that use more than two 'HC161 devices cascaded together.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC161		SN74HC161		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	2 V	0	3.6	0	2.5	0	2.9	MHz
		4.5 V	0	18	0	12	0	14	
		6 V	0	21	0	14	0	17	
t_w	Pulse duration, CLK high or low	2 V	140		200		170		ns
		4.5 V	28		40		36		
		6 V	24		36		30		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C		SN54HC161		SN74HC161		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	3.6		2.5		2.9		MHz
			4.5 V	18		12		14		
			6 V	21		14		17		

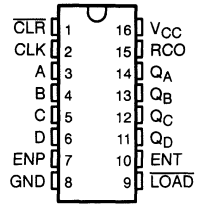
NOTE 3: These limits apply only to applications that use more than two 'HC161 devices cascaded together.

If the 'HC161 are used as a single unit, or only two cascaded together, then the maximum clock frequency that the device can use is not limited because of the glitch. In these situations, the device can be operated at the maximum specifications.

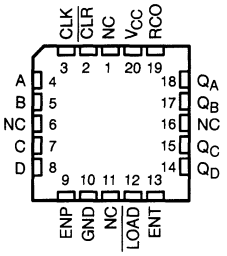
A glitch can appear on RCO of a single 'HC161 device, depending on the relationship of ENT to CLK. Any application that uses RCO to drive any input except an ENT of another cascaded 'HC161 must take this into consideration.

- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Synchronous Counting**
- **Synchronously Programmable**
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC163 . . . J OR W PACKAGE
SN74HC163 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC163 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 'HC163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes normally associated with synchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, they can be preset to any number between 0 and 9 or 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

The clear function for the 'HC163 is synchronous. A low level at the clear ($\overline{CLR}$) input sets all four of the flip-flop outputs low after the next low-to-high transition of CLK, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to $\overline{CLR}$ to synchronously clear the counter to 0000 (LLLL).

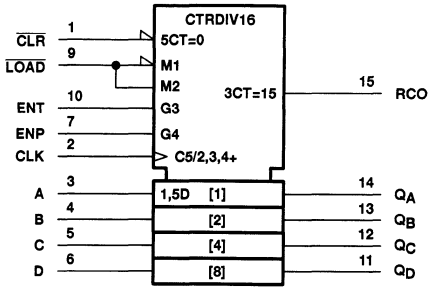
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. ENP, ENT, and a ripple-carry (RCO) output are instrumental in accomplishing this function. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. Enabling RCO produces a high-level pulse while the count is maximum (9 or 15 with Q_A high). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

description (continued)

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

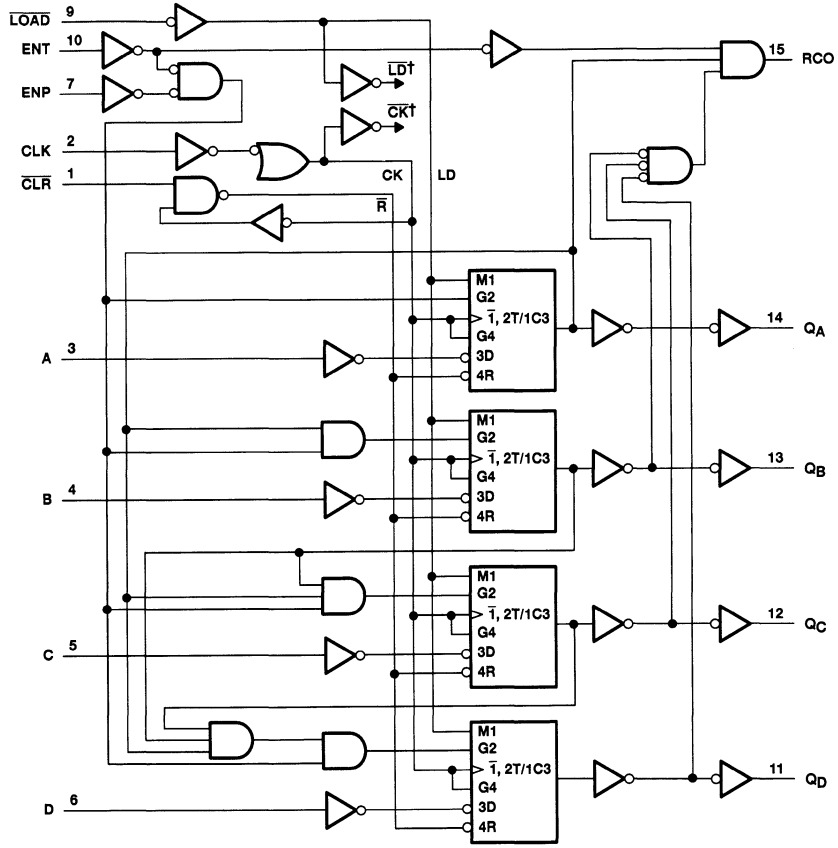
The SN54HC163 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC163 is characterized for operation from –40°C to 85°C.

logic symbol†



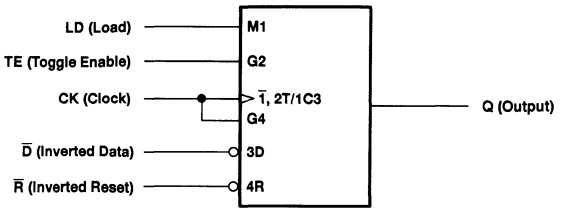
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)

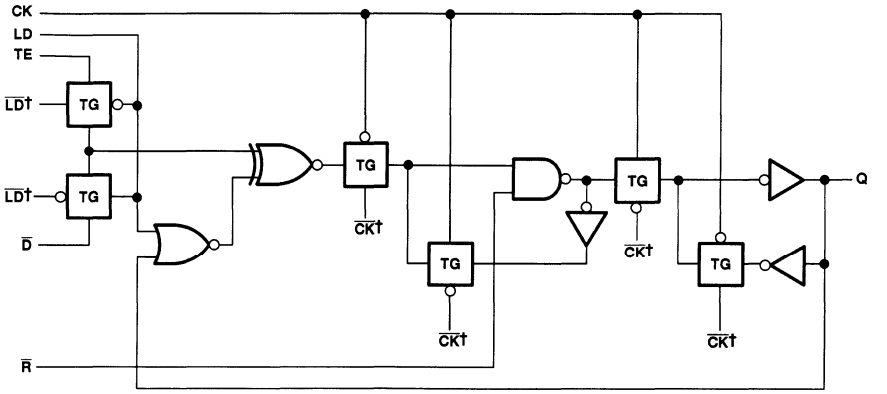


† For simplicity, routing of complementary signals $\overline{LD}$ and $\overline{CK}$ is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.
Pin numbers shown are for the D, J, N, and W packages.

logic symbol, each D/T flip-flop



logic diagram, each D/T flip-flop (positive logic)

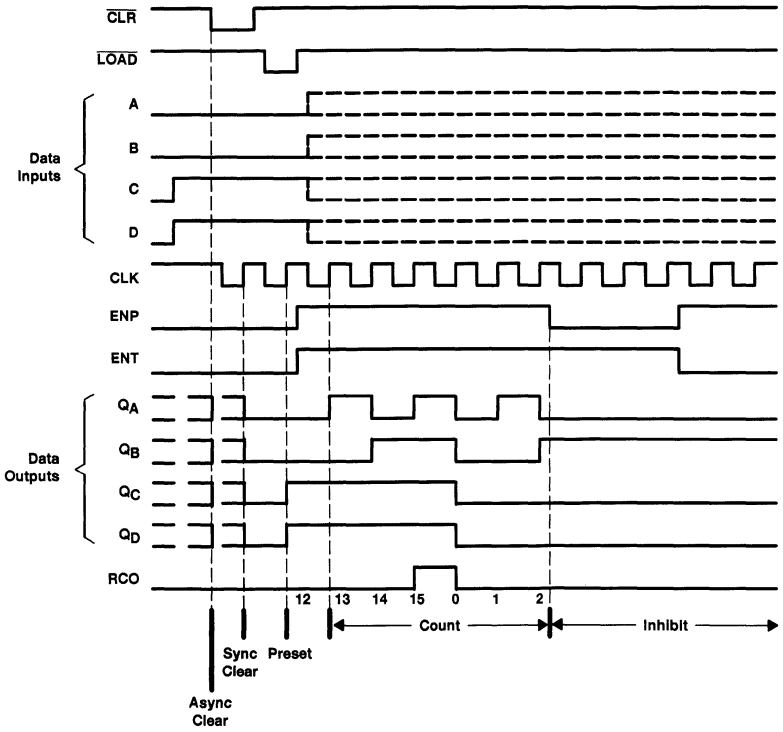


† The origins of $\overline{LD}$ and $\overline{CK}$ are shown in the logic diagram of the overall device.

typical clear, preset, count, and inhibit sequence

The following sequence is illustrated below:

1. Clear outputs to zero (synchronous)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC163			SN74HC163			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t‡	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

‡ If this device is used in the threshold region (from V_{IL}max = 0.5 V to V_{IH}min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC163		SN74HC163		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC163		SN74HC163		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	29	
t_w	Pulse duration	CLK high or low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time before CLK↑	A, B, C, or D	2 V	150		225		190		ns
			4.5 V	30		45		38		
			6 V	26		38		32		
		$\overline{LOAD}$ low	2 V	135		205		170		
			4.5 V	27		41		34		
			6 V	23		35		29		
		ENP, ENT	2 V	170		255		215		
			4.5 V	34		51		43		
			6 V	29		43		37		
		$\overline{CLR}$ low	2 V	160		240		200		
			4.5 V	32		48		40		
			6 V	27		41		34		
		$\overline{CLR}$ inactive	2 V	160		240		200		
			4.5 V	32		48		40		
			6 V	27		41		34		
t_h	Hold time, all synchronous inputs after CLK↑		2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		

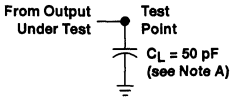
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC163		SN74HC163		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	14		4.2		5		MHz
			4.5 V	31	40		21		25		
			6 V	36	44		25		29		
t_{pd}	CLK	RCO	2 V		83	215		325		270	ns
			4.5 V		24	43		65		54	
			6 V		20	37		55		46	
		Any Q	2 V		80	205		310		255	
			4.5 V		25	41		62		51	
			6 V		21	35		53		43	
	ENT	RCO	2 V		62	195		295		245	
			4.5 V		17	39		59		49	
			6 V		14	33		50		42	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

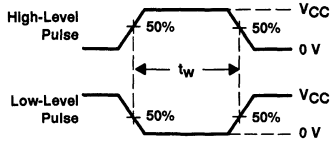
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	60	pF

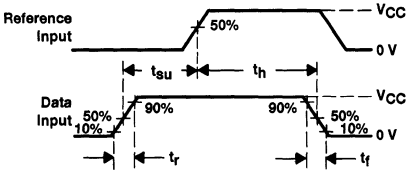
PARAMETER MEASUREMENT INFORMATION



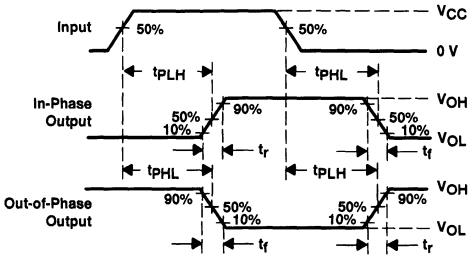
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

n-bit synchronous counters

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 'HC163 count in binary. Virtually any count mode (modulo-N, N_1-to-N_2, N_1-to-maximum) can be used with this fast look-ahead circuit.

The application circuit shown in Figure 2 is not valid for clock frequencies above 18 MHz (at 25°C and 4.5-V V_{CC}). The reason for this is that there is a glitch that is produced on the second stage's RCO and every succeeding stage's RCO. This glitch is common to all HC vendors that Texas Instruments has evaluated, in addition to the bipolar equivalents (LS, ALS, AS).

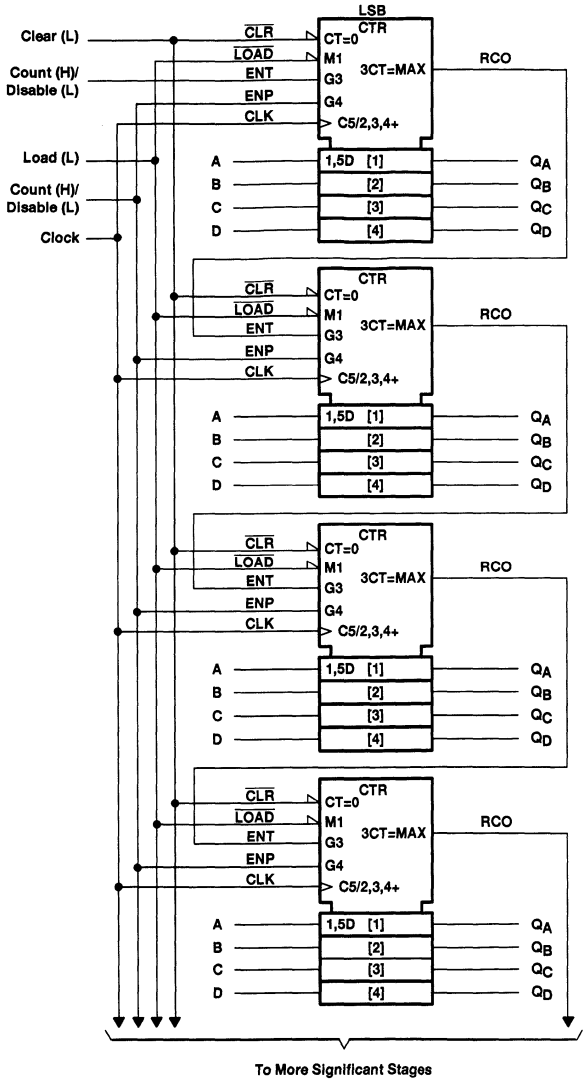

LSB
Clear (L)
Count (H)/
Disable (L)
Load (L)
Count (H)/
Disable (L)
Clock
CLR
LOAD
ENT
ENP
CLK
CTR
CT=0
M1
G3
G4
C5/2,3,4+
3CT=MAX
RCO
A
B
C
D
1,5D [1]
[2]
[3]
[4]
QA
QB
QC
QD
To More Significant Stages

Figure 2

The glitch on RCO is caused because the propagation delay of the rising edge of Q_A of the second stage is shorter than the propagation delay of the falling edge of ENT. RCO is the product of ENT, Q_A, Q_B, Q_C, and Q_D (ENT × Q_A × Q_B × Q_C × Q_D). The resulting glitch is about 7–12 ns in duration. Figure 3 shows the condition in which the glitch occurs. For simplicity, only two stages are being considered, but the results can be applied to other stages. Q_B, Q_C, and Q_D of the first and second stage are at logic one, and Q_A of both stages are at logic zero (1110 1110) after the first clock pulse. On the rising edge of the second clock pulse, Q_A and RCO of the first stage go high. On the rising edge of the third clock pulse, Q_A and RCO of the first stage return to a low level, and Q_A of the second stage goes to a high level. At this time, the glitch on RCO of the second stage appears because of the race condition inside the chip.

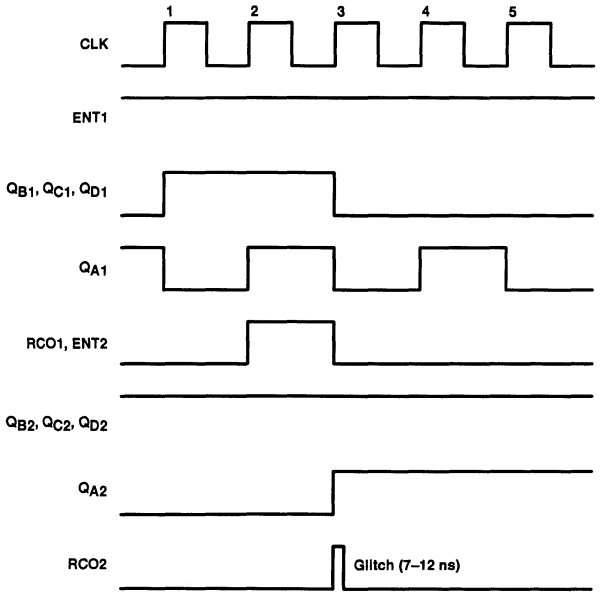


Figure 3

The glitch causes a problem in the next stage (stage three) if the glitch is still present when the next rising clock edge appears (clock pulse 4). To ensure that this does not happen, the clock frequency must be less than the inverse of the sum of the clock-to-RCO propagation delay and the glitch duration (t_g). In other words, $f_{max} = 1/(t_{pd}$ CLK-to-RCO + $t_g)$. For example, at 25°C at 4.5-V V_{CC}, the clock-to-RCO propagation delay is 43 ns and the maximum duration of the glitch is 12 ns. Therefore, the maximum clock frequency that the cascaded counters can use is 18 MHz. The following tables contain the f_{clock}, t_w, and f_{max} specifications for applications that use more than two 'HC163 devices cascaded together.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC163		SN74HC163		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	2 V	0	3.6	0	2.5	0	2.9	MHz
		4.5 V	0	18	0	12	0	14	
		6 V	0	21	0	14	0	17	
t_w	Pulse duration, CLK high or low	2 V	140		200		170		ns
		4.5 V	28		40		36		
		6 V	24		36		30		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C		SN54HC163		SN74HC163		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	3.6		2.5		2.9		MHz
			4.5 V	18		12		14		
			6 V	21		14		17		

NOTE 3: These limits apply only to applications that use more than two 'HC163 devices cascaded together.

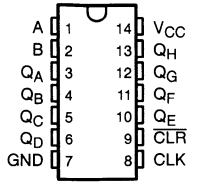
If the 'HC163 are used as a single unit, or only two cascaded together, then the maximum clock frequency that the device can use is not limited because of the glitch. In these situations, the device can be operated at the maximum specifications.

A glitch can appear on RCO of a single 'HC163 device, depending on the relationship of ENT to CLK. Any application that uses RCO to drive any input except an ENT of another cascaded 'HC163 must take this into consideration.

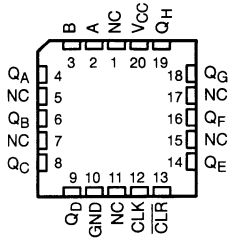
SCLS115A – DECEMBER 1982 – REVISED JANUARY 1996

- **AND-Gated (Enable/Disable) Serial Inputs**
- **Fully Buffered Clock and Serial Inputs**
- **Direct Clear**
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC164 . . . J OR W PACKAGE
SN74HC164 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC164 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These 8-bit shift registers feature AND-gated serial inputs and an asynchronous clear ($\overline{CLR}$) input. The gated serial (A and B) inputs permit complete control over incoming data; a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock (CLK) pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs can be changed while CLK is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of CLK.

The SN54HC164 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC164 is characterized for operation from –40°C to 85°C.

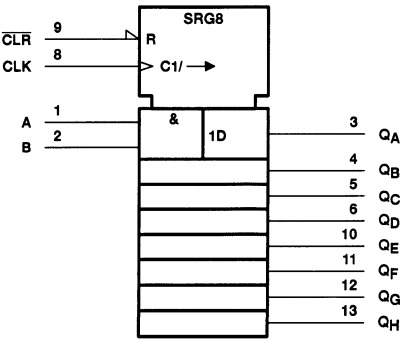
FUNCTION TABLE

INPUTS				OUTPUTS		
$\overline{CLR}$	CLK	A	B	Q_A	$Q_B \ldots Q_H$	
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established

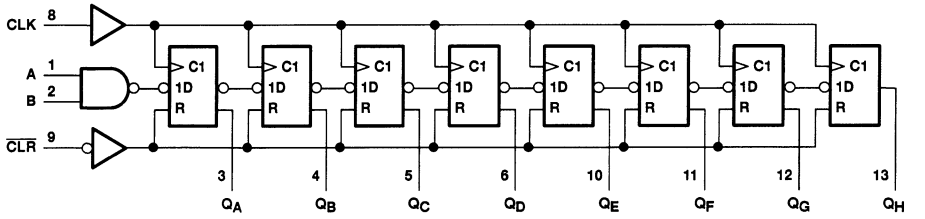
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most recent ↑ transition of CLK: indicates a 1-bit shift

logic symbol†



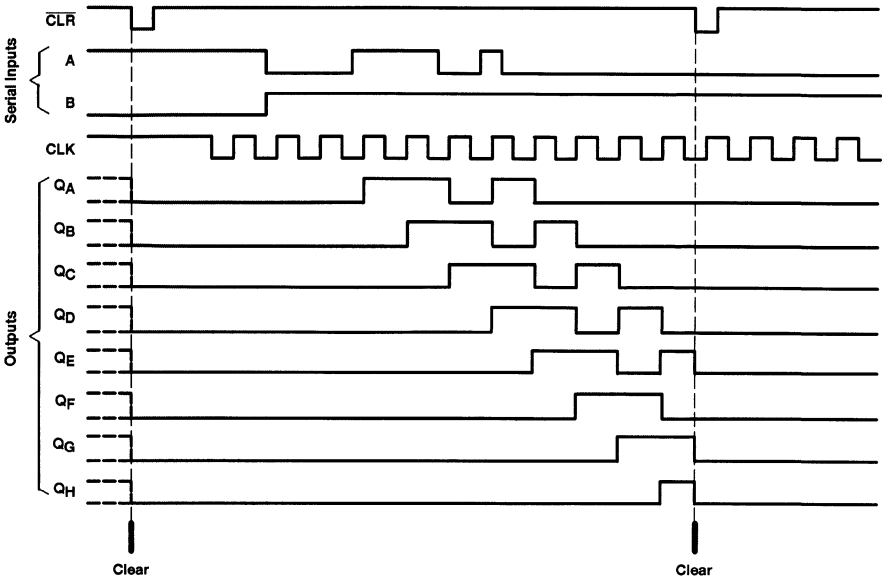
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, and W packages.

typical clear, shift, and clear sequence



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC164			SN74HC164			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t†	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

† If this device is used in the threshold region (from V_{IL}max = 0.5 V to V_{IH}min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC164		SN74HC164		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC164		SN74HC164		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	28	
t_w	Pulse duration	$\overline{CLR}$ low	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		CLK high or low	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		18		
t_{su}	Setup time before CLK↑	Data	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		$\overline{CLR}$ inactive	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		25		21		
t_h	Hold time, data after CLK↑		2 V	5		5		5		ns
			4.5 V	5		5		5		
			6 V	5		5		5		

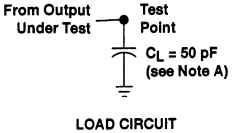
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC164		SN74HC164		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	10		4.2		5		MHz
			4.5 V	31	54		21		25		
			6 V	36	62		25		28		
t_{PHL}	$\overline{CLR}$	Any Q	2 V		140	205		295		255	ns
			4.5 V		28	41		59		51	
			6 V		24	35		51		46	
t_{pd}	CLK	Any Q	2 V		115	175		265		220	
			4.5 V		23	35		53		44	
			6 V		20	30		45		38	
t_t			2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

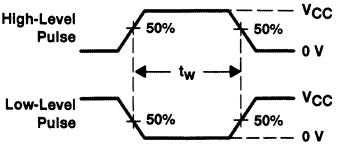
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	135	pF

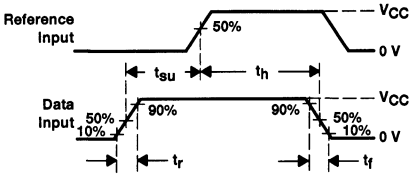
PARAMETER MEASUREMENT INFORMATION



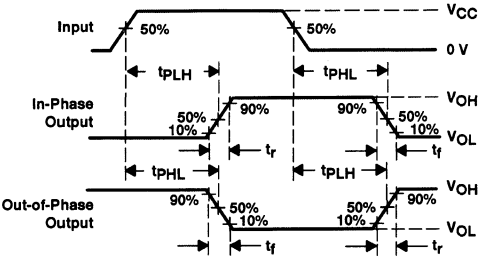
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



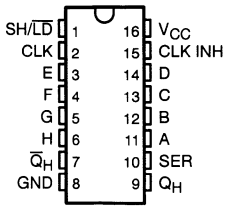
VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

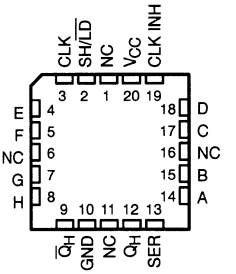
Figure 1. Load Circuit and Voltage Waveforms

- **Complementary Outputs**
- **Direct Overriding Load (Data) Inputs**
- **Gated Clock Inputs**
- **Parallel-to-Serial Data Conversion**
- **Package Options Include Plastic Small-Outline (D), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC165 . . . J OR W PACKAGE
SN74HC165 . . . D, N, OR PW PACKAGE
(TOP VIEW)



SN54HC165 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'HC165 are 8-bit parallel-load shift registers that, when clocked, shift the data toward a serial (Q_H) output. Parallel-in access to each stage is provided by eight individual direct data (A–H) inputs that are enabled by a low level at the shift/load (SH/$\overline{LD}$) input. The 'HC165 also feature a clock-inhibit (CLK INH) function and a complementary serial ($\overline{Q}_H$) output.

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while SH/$\overline{LD}$ is held high and CLK INH is held low. The functions of CLK and CLK INH are interchangeable. Since a low CLK and a low-to-high transition of CLK INH also accomplish clocking, CLK INH should be changed to the high level only while CLK is high. Parallel loading is inhibited when SH/$\overline{LD}$ is held high. While SH/$\overline{LD}$ is low, the parallel inputs to the register are enabled independently of the levels of the CLK, CLK INH, or serial (SER) inputs.

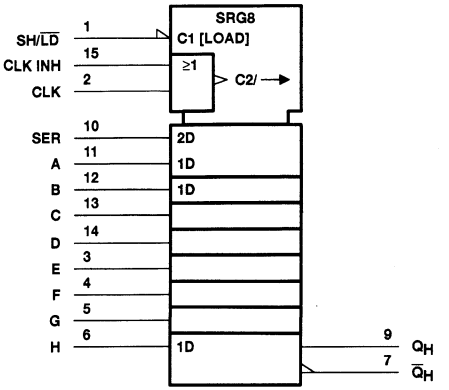
The SN54HC165 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC165 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS			FUNCTION
SH/$\overline{LD}$	CLK	CLK INH	
L	X	X	Parallel load
H	H	X	No change
H	X	H	No change
H	L	↑	Shift†
H	↑	L	Shift†

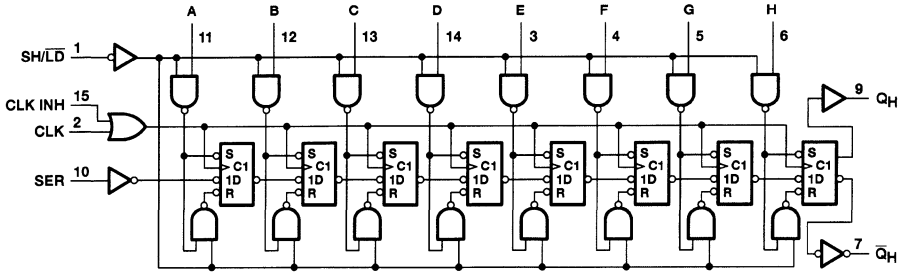
† Shift = content of each internal register shifts toward serial output Q_H. Data at SER is shifted into the first register.

logic symbol†



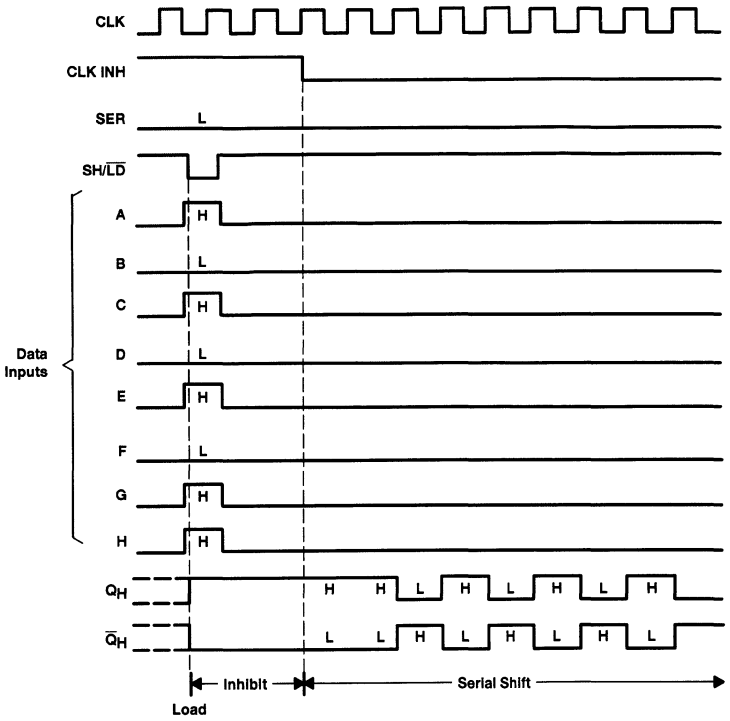
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, PW, and W packages.

typical shift, load, and inhibit sequence



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.3 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC165			SN74HC165			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t†	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

† If this device is used in the threshold region (from V_{IL} max = 0.5 V to V_{IH} min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC165		SN74HC165		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC165		SN74HC165		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	2 V	0	6	0	4.2	0	5	MHz
		4.5 V	0	31	0	21	0	25	
		6 V	0	36	0	25	0	29	
t_w	Pulse duration, SH/$\overline{LD}$ low	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
	Pulse duration, CLK high or low	2 V	80		120		100		
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su}	Setup time, SH/$\overline{LD}$ high before CLK↑	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
	Setup time, SER before CLK↑	2 V	40		60		50		
		4.5 V	8		12		10		
		6 V	7		10		9		
	Setup time, CLK INH low before CLK↑	2 V	100		150		125		
		4.5 V	20		30		25		
		6 V	17		25		21		
	Setup time, CLK INH high before CLK↑	2 V	40		60		50		
		4.5 V	8		12		10		
		6 V	7		10		9		
	Setup time, Data before SH/$\overline{LD}$↓	2 V	100		150		125		
		4.5 V	20		30		25		
		6 V	17		26		21		
t_h	Hold time, SER data after CLK↑	2 V	5		5		5		ns
		4.5 V	5		5		5		
		6 V	5		5		5		
	Hold time, PAR data after SH/$\overline{LD}$↓	2 V	5		5		5		
		4.5 V	5		5		5		
		6 V	5		5		5		

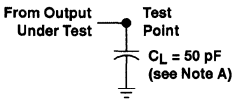
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC165		SN74HC165		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	13		4.2		5		MHz
			4.5 V	31	50		21		25		
			6 V	36	62		25		29		
t_{pd}	SH/$\overline{LD}$	Q_H or $\overline{Q}_H$	2 V		80	150		225		190	ns
			4.5 V		20	30		45		38	
			6 V		16	26		38		32	
	CLK	Q_H or $\overline{Q}_H$	2 V		75	150		225		190	
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
	H	Q_H or $\overline{Q}_H$	2 V		75	150		225		190	
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

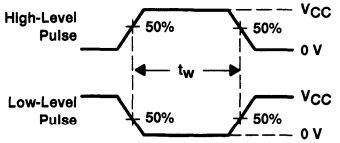
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	75	pF

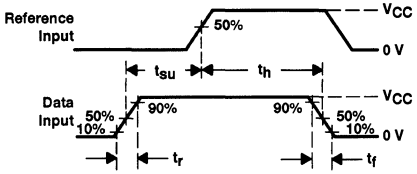
PARAMETER MEASUREMENT INFORMATION



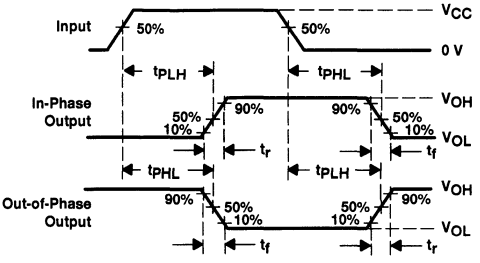
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



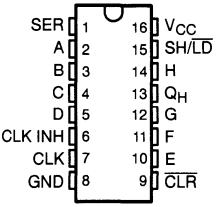
VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

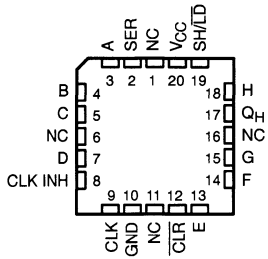
Figure 1. Load Circuit and Voltage Waveforms

- **Synchronous Load**
- **Direct Overriding Clear**
- **Parallel-to-Serial Conversion**
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC166 . . . J OR W PACKAGE
SN74HC166 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC166 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

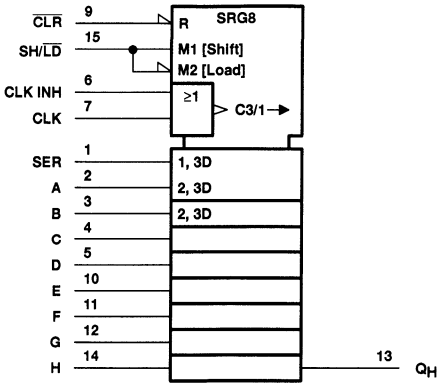
The 'HC166 parallel-in or serial-in, serial-out registers feature gated clock (CLK, CLK INH) inputs and an overriding clear ($\overline{CLR}$) input. The parallel-in or serial-in modes are established by the shift/load (SH/$\overline{LD}$) input. When high, SH/$\overline{LD}$ enables the serial (SER) data input and couples the eight flip-flops for serial shifting with each clock (CLK) pulse. When low, the parallel (broadside) data inputs are enabled, and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of CLK through a 2-input positive-NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either CLK or CLK INH high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free running, and the register can be stopped on command with the other clock input. CLK INH should be changed to the high level only when CLK is high. $\overline{CLR}$ overrides all other inputs, including CLK, and resets all flip-flops to zero.

The SN54HC166 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC166 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

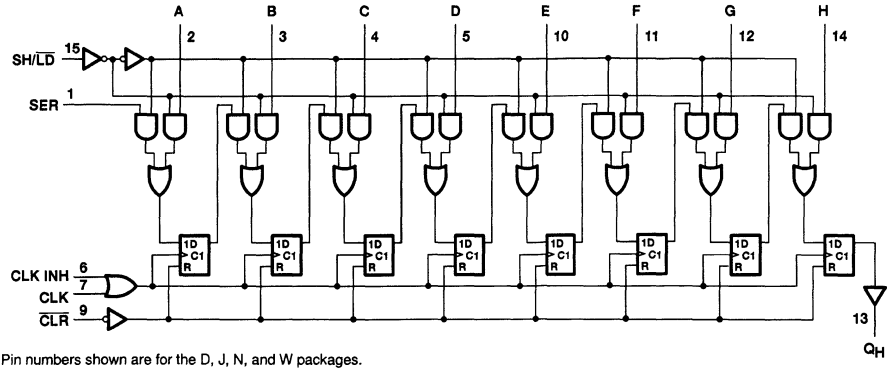
INPUTS						OUTPUTS		
						INTERNAL		
$\overline{CLR}$	SH/$\overline{LD}$	CLK INH	CLK	SER	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

logic symbol†



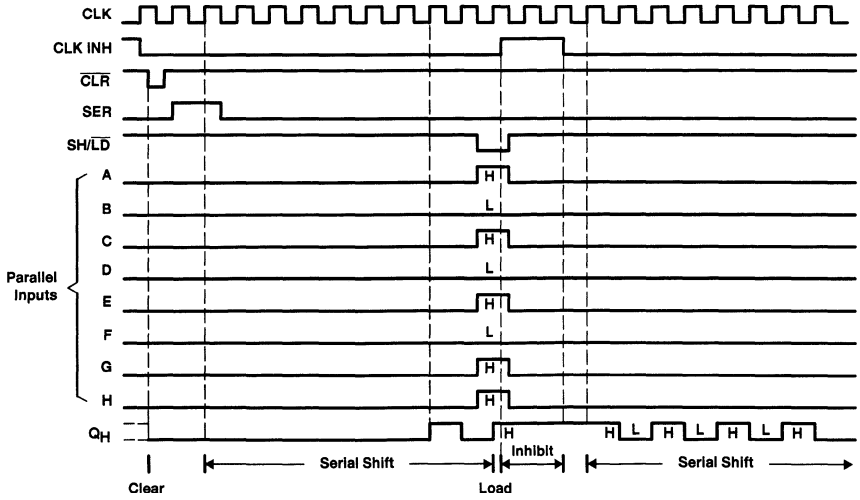
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, and W packages.

typical clear, shift, load, inhibit, and shift sequence



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC166			SN74HC166			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t‡	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

‡ If this device is used in the threshold region (from V_{IL}max = 0.5 V to V_{IH}min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC166		SN74HC166		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC166		SN74HC166		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	29	
t_w	Pulse duration	$\overline{CLR}$ low	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		26		21		
		CLK high or low	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time	SH/$\overline{LD}$ high before CLK↑	2 V	145		220		180		ns
			4.5 V	29		44		36		
			6 V	25		38		31		
		SER before CLK↑	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		
		CLK INH low before CLK↑	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		26		21		
		Data before CLK↑	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		
		$\overline{CLR}$ inactive before CLK↑	2 V	40		60		50		
			4.5 V	8		12		10		
			6 V	7		10		9		
t_h	Hold time	SH/$\overline{LD}$ high after CLK↑	2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		
		SER after CLK↑	2 V	5		5		5		
			4.5 V	5		5		5		
			6 V	5		5		5		
		CLK INH high after CLK↑	2 V	0		0		0		
			4.5 V	0		0		0		
			6 V	0		0		0		
		Data after CLK↑	2 V	5		5		5		
			4.5 V	5		5		5		
			6 V	5		5		5		

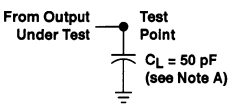
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC166		SN74HC166		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	11		4.2		5		MHz
			4.5 V	31	36		21		25		
			6 V	36	45		25		29		
t_{PHL}	$\overline{CLR}$	Q_H	2 V		62	120		180		150	ns
			4.5 V		18	24		36		30	
			6 V		13	20		31		26	
t_{pd}	CLK	Q_H	2 V		75	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

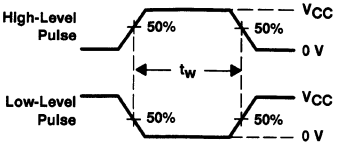
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	50	pF

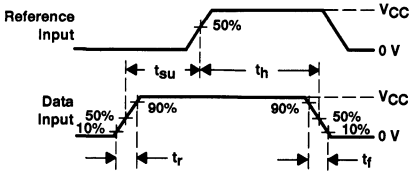
PARAMETER MEASUREMENT INFORMATION



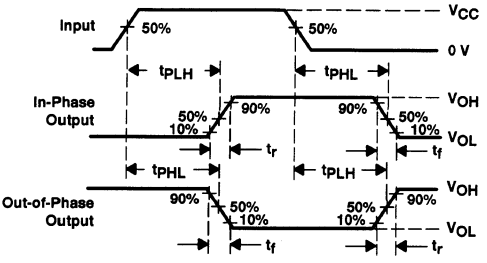
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



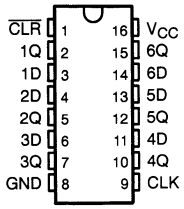
VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

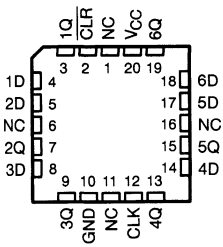
Figure 1. Load Circuit and Voltage Waveforms

- **Contain Six Flip-Flops With Single-Rail Outputs**
- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC174 . . . J OR W PACKAGE
SN74HC174 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC174 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These monolithic positive-edge-triggered D-type flip-flops have a direct clear ($\overline{CLR}$) input.

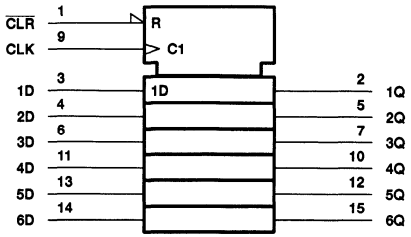
Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

The SN54HC174 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC174 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

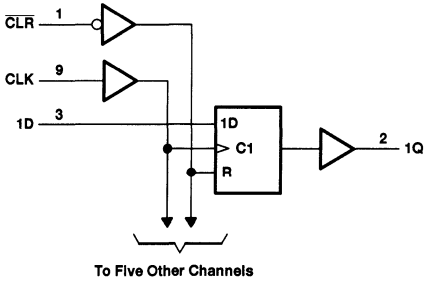
INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC174			SN74HC174			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC174		SN74HC174		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC174		SN74HC174		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	29	
t_w	Pulse duration	$\overline{CLR}$ low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
		CLK high or low	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time before CLK↑	Data	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		$\overline{CLR}$ inactive	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		25		21		
t_h	Hold time, data after CLK↑		2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		

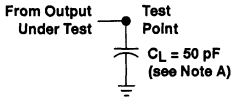
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC174		SN74HC174		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	9		4.2		5		MHz
			4.5 V	31	44		21		25		
			6 V	36	50		25		29		
t_{pd}	$\overline{CLR}$	Any	2 V		58	160		240		200	ns
			4.5 V		17	32		48		40	
			6 V		14	27		41		34	
	CLK	Any	2 V		58	160		240		200	
			4.5 V		17	32		48		40	
			6 V		14	27		41		34	
t_t		Any	2 V		38	75		110		90	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

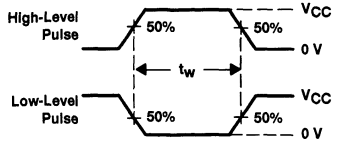
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	No load	27	pF

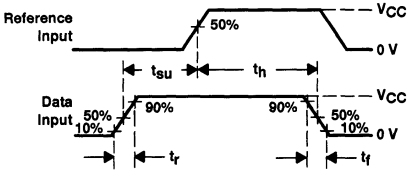
PARAMETER MEASUREMENT INFORMATION



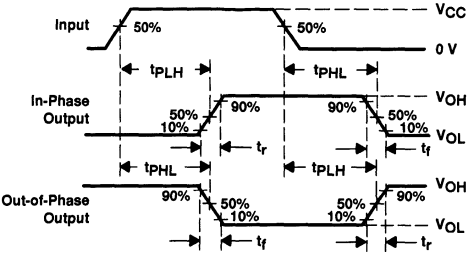
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



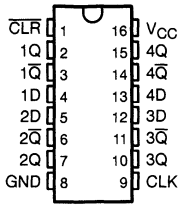
VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

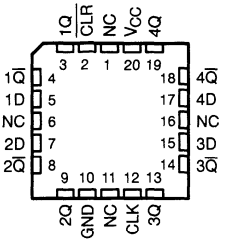
Figure 1. Load Circuit and Voltage Waveforms

- **Contain Four Flip-Flops With Double-Rail Outputs**
- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**
- **Package Options Include Plastic Small-Outline (D), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC175 . . . J OR W PACKAGE
SN74HC175 . . . D, N, OR PW PACKAGE
(TOP VIEW)



SN54HC175 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These monolithic positive-edge-triggered D-type flip-flops have a direct clear ($\overline{CLR}$) input. The 'HC175 feature complementary outputs from each flip-flop.

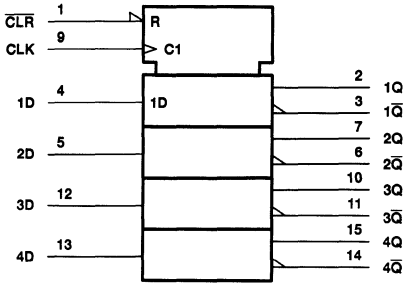
Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

The SN54HC175 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC175 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

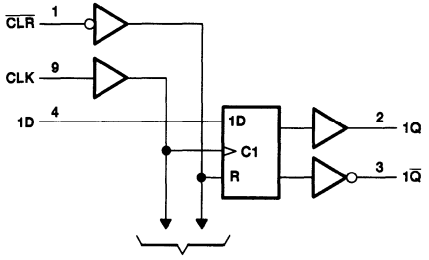
INPUTS			OUTPUTS	
$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.3 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC175			SN74HC175			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC175		SN74HC175		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC175		SN74HC175		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	29	
t_w	Pulse duration	$\overline{CLR}$ low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
		CLK high or low	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time before CLK↑	Data	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		$\overline{CLR}$ inactive	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		25		21		
t_h	Hold time, data after CLK↑		2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		

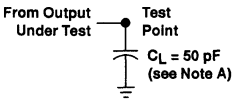
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC175		SN74HC175		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	12		4.2		5		MHz
			4.5 V	31	50		21		25		
			6 V	36	60		25		29		
t_{pd}	$\overline{CLR}$	Any	2 V		52	150		255		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
	CLK	Any	2 V		58	150		255		190	
			4.5 V		16	30		45		38	
			6 V		13	26		38		32	
t_t		Any	2 V		38	75		110		90	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

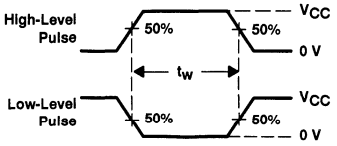
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	No load	30	pF

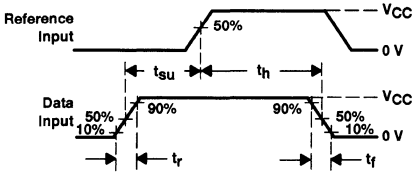
PARAMETER MEASUREMENT INFORMATION



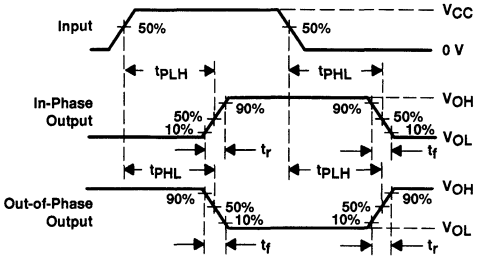
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

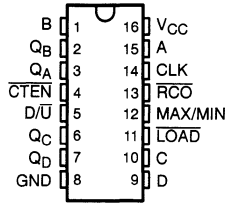
Figure 1. Load Circuit and Voltage Waveforms

SN54HC191, SN74HC191
4-BIT SYNCHRONOUS UP/DOWN BINARY COUNTERS

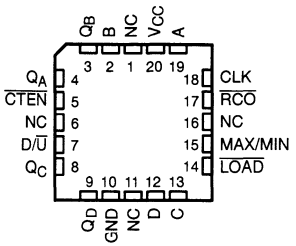
SCLS121A – DECEMBER 1982 – REVISED JANUARY 1996

- **Single Down/Up Count-Control Line**
- **Look-Ahead Circuitry Enhances Speed of Cascaded Counters**
- **Fully Synchronous in Count Modes**
- **Asynchronously Presettable With Load Control**
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC191 . . . J OR W PACKAGE
SN74HC191 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC191 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'HC191 are 4-bit synchronous, reversible, up/down binary counters. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock (CLK) input if the count-enable ($\overline{CTEN}$) input is low. A high at $\overline{CTEN}$ inhibits counting. The direction of the count is determined by the level of the down/up (D/$\overline{U}$) input. When D/$\overline{U}$ is low, the counter counts up, and when D/$\overline{U}$ is high, it counts down.

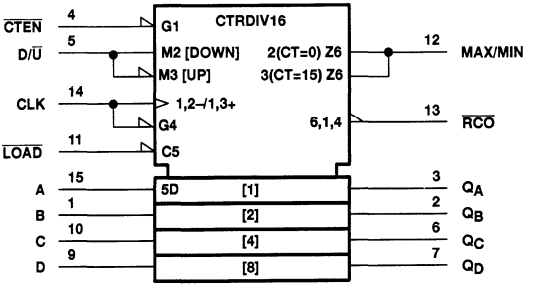
These counters feature a fully independent clock circuit. Change at the control ($\overline{CTEN}$ and D/$\overline{U}$) inputs that modifies the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter is dictated solely by the condition meeting the stable setup and hold times.

These counters are fully programmable; that is, each of the outputs can be preset to either level by placing a low on the load ($\overline{LOAD}$) input and entering the desired data at the data inputs. The output changes to agree with the data inputs independently of the level of CLK. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

Two outputs are available to perform the cascading function: ripple clock ($\overline{RCO}$) and maximum/minimum (MAX/MIN) count. MAX/MIN produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down, or maximum (9 or 15) counting up. $\overline{RCO}$ produces a low-level output pulse under those same conditions, but only while CLK is low. The counters can be easily cascaded by feeding $\overline{RCO}$ to $\overline{CTEN}$ of the succeeding counter if parallel clocking is used, or to CLK if parallel enabling is used. MAX/MIN can be used to accomplish look ahead for high-speed operation.

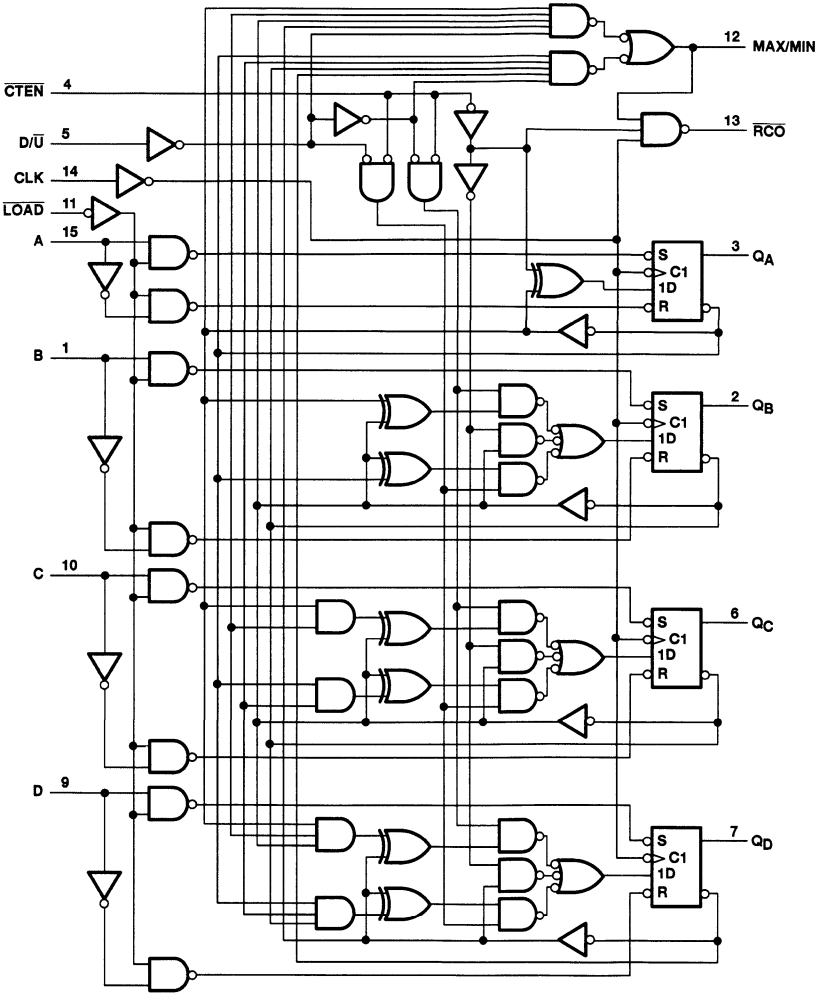
The SN54HC191 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC191 is characterized for operation from –40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)

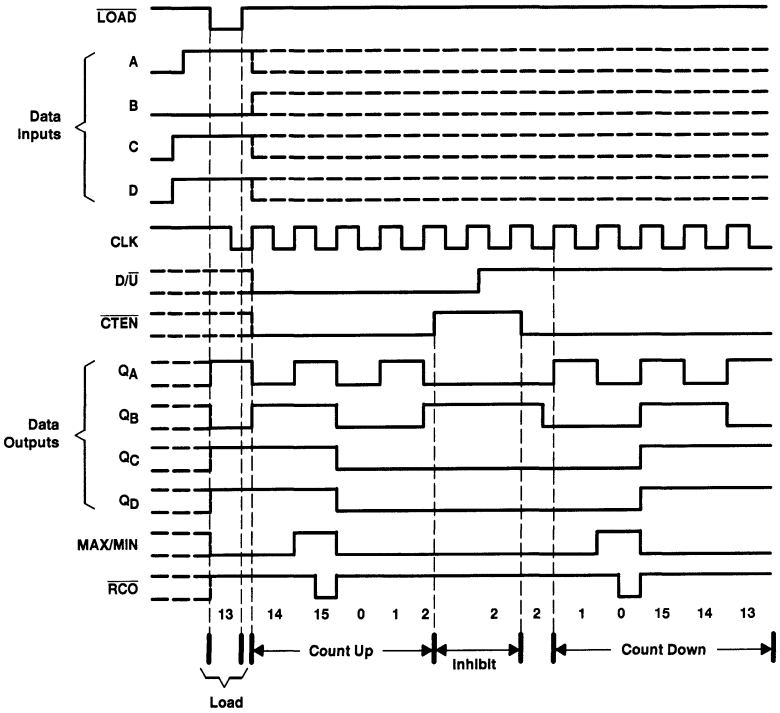


Pin numbers shown are for the D, J, N, and W packages.

typical load, count, and inhibit sequence

The following sequence is illustrated below:

1. Load (preset) to binary 13
2. Count up to 14, 15 (maximum), 0, 1, and 2
3. Inhibit
4. Count down to 1, 0 (minimum), 15, 14, and 13



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC191			SN74HC191			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t‡	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

‡ If this device is used in the threshold region (from V_{IL}max = 0.5 V to V_{IH}min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC191		SN74HC191		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC191		SN74HC191		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	4.2	0	2.8	0	3.3	MHz
			4.5 V	0	21	0	14	0	17	
			6 V	0	24	0	16	0	19	
t_w	Pulse duration	$\overline{LOAD}$ low	2 V	120		180		150		ns
			4.5 V	24		36		30		
			6 V	21		31		26		
		CLK high or low	2 V	120		180		150		
			4.5 V	24		36		30		
			6 V	21		31		26		
t_{su}	Setup time	Data before $\overline{LOAD}$↑	2 V	150		230		188		ns
			4.5 V	30		46		38		
			6 V	25		38		32		
		$\overline{CTEN}$ before CLK↑	2 V	205		306		255		
			4.5 V	41		61		51		
			6 V	35		53		44		
		D/$\overline{U}$ before CLK↑	2 V	205		306		255		
			4.5 V	41		61		51		
			6 V	35		53		44		
		$\overline{LOAD}$ inactive before CLK↑	2 V	150		225		190		
			4.5 V	30		45		38		
			6 V	25		38		32		
t_h	Hold time	Data after $\overline{LOAD}$↑	2 V	5		5		5		ns
			4.5 V	5		5		5		
			6 V	5		5		5		
		$\overline{CTEN}$ after CLK↑	2 V	5		5		5		
			4.5 V	5		5		5		
			6 V	5		5		5		
		D/$\overline{U}$ after CLK↑	2 V	5		5		5		
			4.5 V	5		5		5		
			6 V	5		5		5		

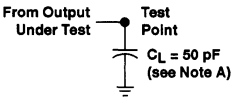
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC191		SN74HC191		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	4.2	8		2.8		3.3		MHz
			4.5 V	21	42		14		17		
			6 V	24	48		16		19		
t_{pd}	$\overline{LOAD}$	Any Q	2 V		130	264		396		330	ns
			4.5 V		40	53		79		66	
			6 V		33	45		67		56	
	A, B, C, or D	Q_A, Q_B, Q_C, or Q_D	2 V		135	240		360		300	
			4.5 V		36	48		72		60	
			6 V		30	41		61		51	
	CLK	$\overline{RCO}$	2 V		58	120		180		150	
			4.5 V		17	24		36		30	
			6 V		14	21		31		26	
		Any Q	2 V		107	192		288		240	
			4.5 V		31	38		58		48	
			6 V		26	32		49		41	
		MAX/MIN	2 V		123	252		378		315	
			4.5 V		39	50		76		63	
			6 V		32	43		65		54	
	D/$\overline{U}$	$\overline{RCO}$	2 V		102	228		342		285	
			4.5 V		29	46		68		57	
			6 V		24	38		59		49	
		MAX/MIN	2 V		86	192		288		240	
			4.5 V		24	38		58		48	
			6 V		20	32		49		41	
	$\overline{CTEN}$	$\overline{RCO}$	2 V		50	132		198		165	
			4.5 V		15	26		40		33	
			6 V		13	23		34		28	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

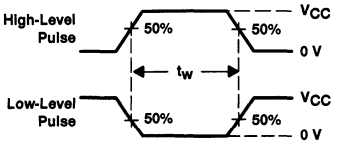
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	50	pF

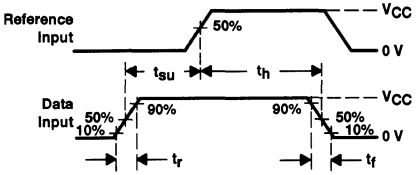
PARAMETER MEASUREMENT INFORMATION



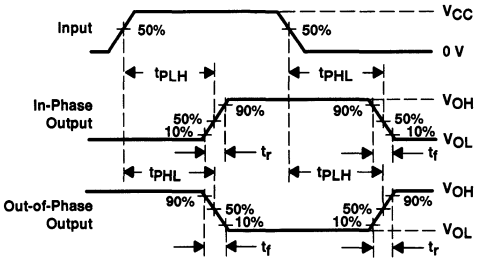
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



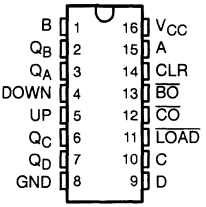
VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

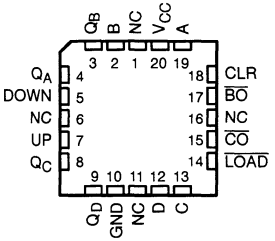
Figure 1. Load Circuit and Voltage Waveforms

- **Look-Ahead Circuitry Enhances Cascaded Counters**
- **Fully Synchronous in Count Modes**
- **Parallel Asynchronous Load for Modulo-N Count Lengths**
- **Asynchronous Clear**
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC193 . . . J OR W PACKAGE
SN74HC193 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC193 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'HC193 are 4-bit synchronous, reversible, up/down binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of either count (clock) input (UP or DOWN). The direction of counting is determined by which count input is pulsed while the other count input is high.

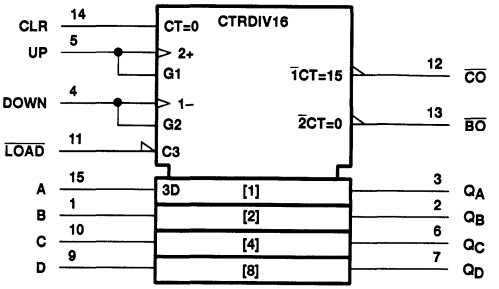
All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load ($\overline{LOAD}$) input and entering the desired data at the data inputs. The output changes to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear (CLR) input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and $\overline{LOAD}$ inputs.

These counters were designed to be cascaded without the need for external circuitry. The borrow ($\overline{BO}$) output produces a low-level pulse while the count is zero (all outputs low) and DOWN is low. Similarly, the carry ($\overline{CO}$) output produces a low-level pulse while the count is maximum (9 or 15) and UP is low. The counters can then be easily cascaded by feeding $\overline{BO}$ and $\overline{CO}$ to DOWN and UP, respectively, of the succeeding counter.

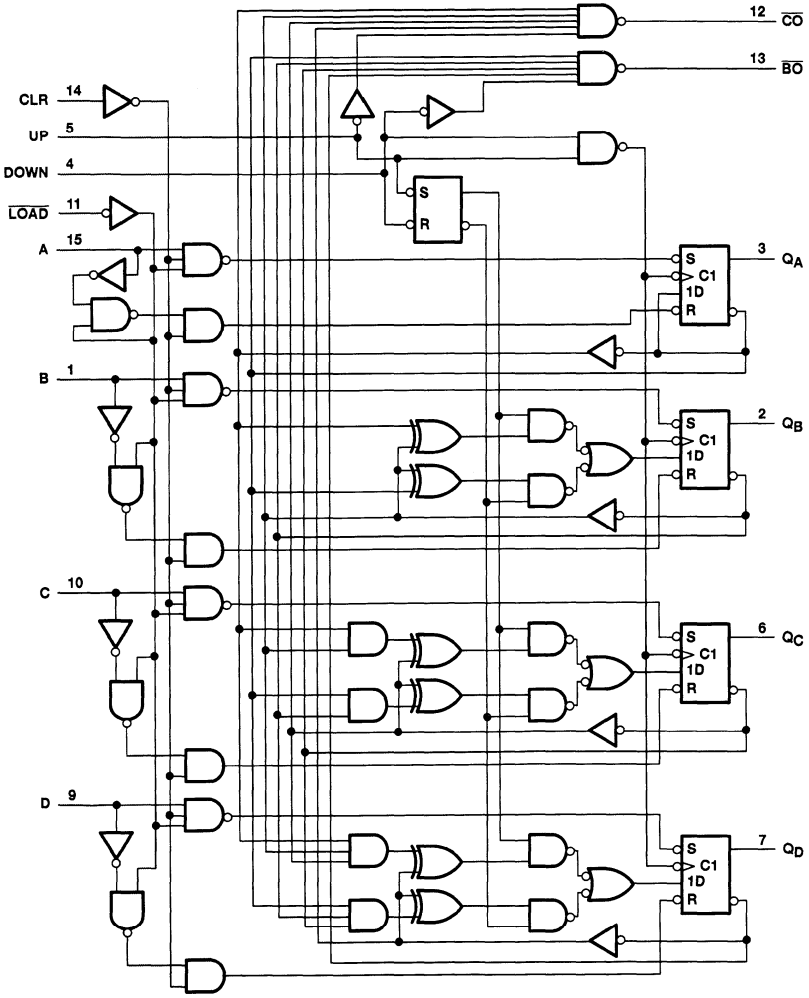
The SN54HC193 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC193 is characterized for operation from –40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)

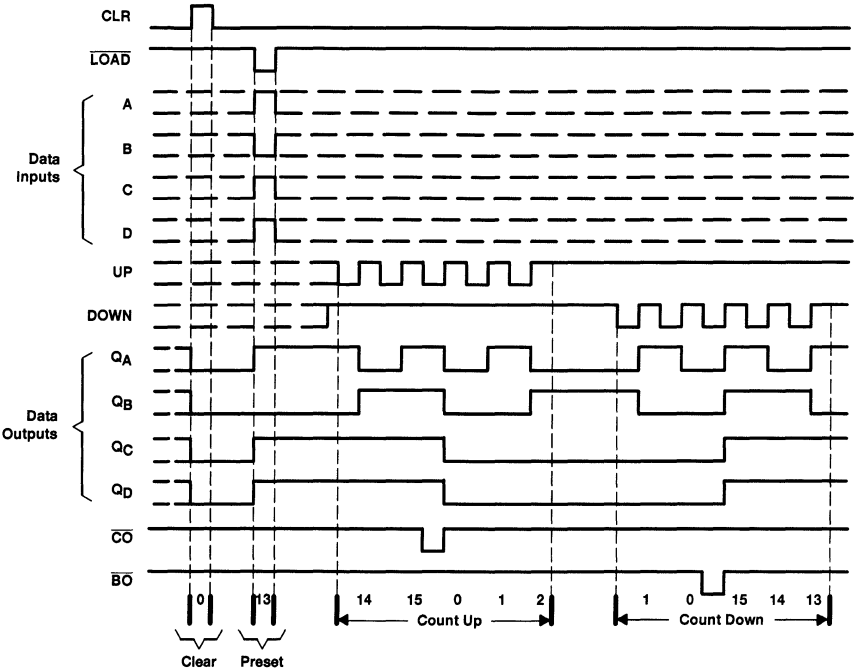


Pin numbers shown are for the D, J, N, and W packages.

typical clear, load, and count sequence

The following sequence is illustrated below:

1. Clear outputs to 0
2. Load (preset) to binary 13
3. Count up to 14, 15, carry, 0, 1, and 2
4. Count down to 1, 0, borrow, 15, 14, and 13



NOTES: A. CLR overrides $\overline{\text{LOAD}}$, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC193			SN74HC193			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t‡	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

‡ If this device is used in the threshold region (from V_{IL}max = 0.5 V to V_{IH}min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC193		SN74HC193		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V			±0.1		±100		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC193		SN74HC193		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	4.2	0	2.8	0	3.3	MHz
			4.5 V	0	21	0	14	0	17	
			6 V	0	24	0	16	0	19	
t_w	Pulse duration	CLR high	2 V	120		180		150		ns
			4.5 V	24		36		30		
			6 V	21		31		26		
		$\overline{LOAD}$ low	2 V	120		180		150		
			4.5 V	24		36		30		
			6 V	21		31		26		
		UP or DOWN high or low	2 V	120		180		150		
			4.5 V	24		36		30		
			6 V	21		31		26		
t_{su}	Setup time	Data before $\overline{LOAD}$ inactive	2 V	110		165		140		ns
			4.5 V	22		33		28		
			6 V	19		28		24		
		CLR inactive before UP↑ or DOWN↑	2 V	110		165		140		
			4.5 V	22		33		28		
			6 V	19		28		24		
		$\overline{LOAD}$ inactive before UP↑ or DOWN↑	2 V	110		165		140		
			4.5 V	22		33		28		
			6 V	19		28		24		
t_h	Hold time	Data after $\overline{LOAD}$ inactive	2 V	5		5		5		ns
			4.5 V	5		5		5		
			6 V	5		5		5		

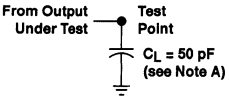
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC193		SN74HC193		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	4.2	8		2.8		3.3		MHz
			4.5 V	21	55		14		17		
			6 V	24	60		16		19		
t_{pd}	UP	$\overline{CO}$	2 V		75	165		250		205	ns
			4.5 V		24	33		50		41	
			6 V		20	28		43		35	
	DOWN	$\overline{BO}$	2 V		75	165		250		205	
			4.5 V		24	33		50		41	
			6 V		20	28		43		35	
	UP or DOWN	Any Q	2 V		190	250		375		315	
			4.5 V		40	50		75		63	
			6 V		35	43		64		54	
	$\overline{LOAD}$	Any Q	2 V		190	260		390		325	
			4.5 V		40	52		78		65	
			6 V		35	44		66		55	
t_{PHL}	CLR	Any Q	2 V		170	240		360		300	ns
			4.5 V		36	48		72		60	
			6 V		31	41		61		51	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

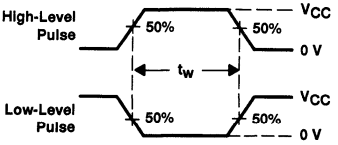
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	50	pF

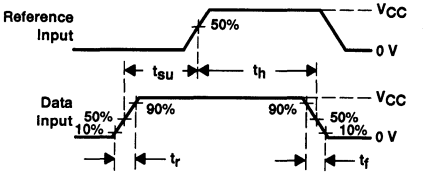
PARAMETER MEASUREMENT INFORMATION



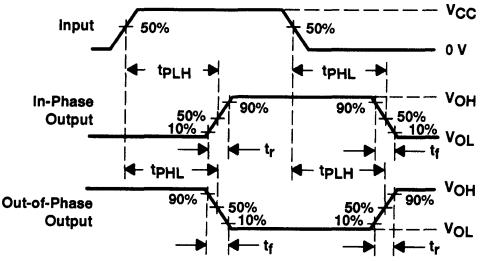
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

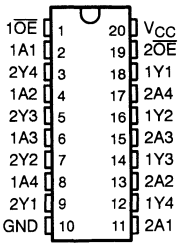
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **High-Current Outputs Drive up to 15 LSTTL Loads**
- **Package Options Include Plastic (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

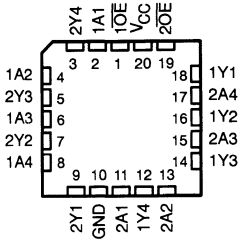
These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The 'HC240 are organized as two 4-bit buffers/drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes inverted data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The SN54HC240 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC240 is characterized for operation from –40°C to 85°C.

SN54HC240 . . . J OR W PACKAGE
SN74HC240 . . . DW OR N PACKAGE
(TOP VIEW)



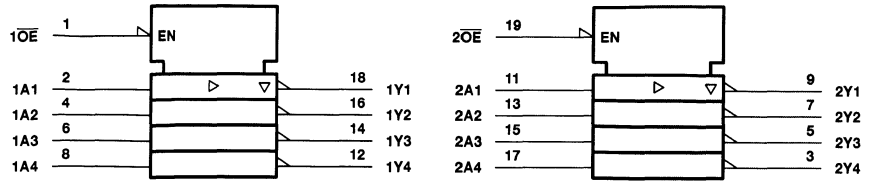
SN54HC240 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each buffer/driver)

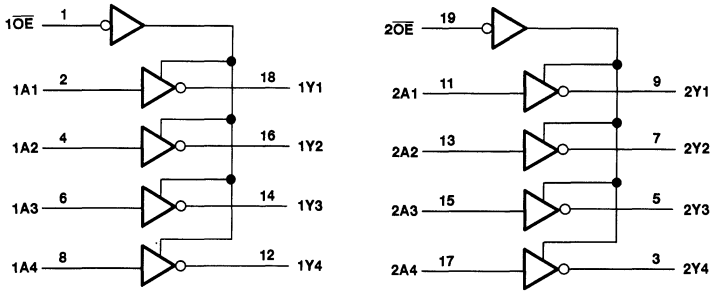
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DW package ..... 1.6 W
N package ..... 1.3 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC240			SN74HC240			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC240		SN74HC240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0		6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC240		SN74HC240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		50	100		150		125	ns
			4.5 V		10	20		30		25	
			6 V		9	17		25		21	
t_{en}	$\overline{OE}$	Y	2 V		75	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_{dis}	$\overline{OE}$	Y	2 V		44	150		225		190	ns
			4.5 V		22	30		45		38	
			6 V		21	26		38		32	
t_t		Y	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

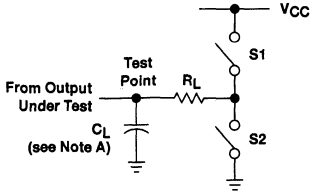
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC240		SN74HC240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		75	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_{en}	$\overline{OE}$	Y	2 V		100	200		300		250	ns
			4.5 V		20	40		60		50	
			6 V		17	34		51		43	
t_t		Y	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

operating characteristics, T_A = 25°C

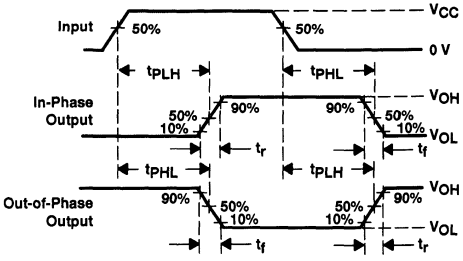
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	No load	35	pF

PARAMETER MEASUREMENT INFORMATION

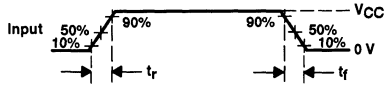


LOAD CIRCUIT

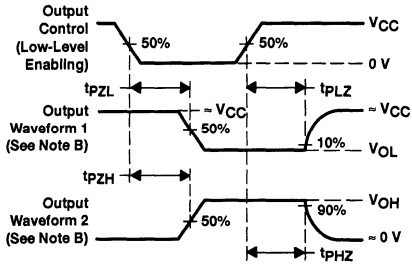
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



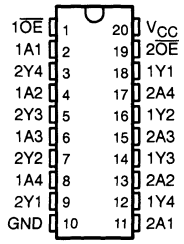
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

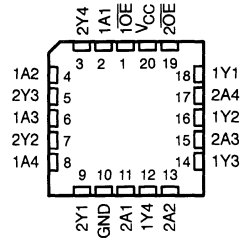
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **High-Current Outputs Drive up to 15 LSTTL Loads**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HCT240 . . . J OR W PACKAGE
SN74HCT240 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT240 . . . FK PACKAGE
(TOP VIEW)



description

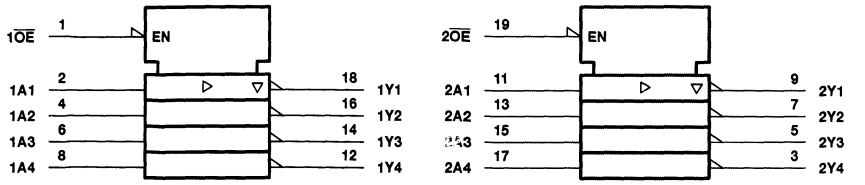
These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The 'HCT240 are organized as two 4-bit buffers/drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes inverted data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The SN54HCT240 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT240 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer/driver)

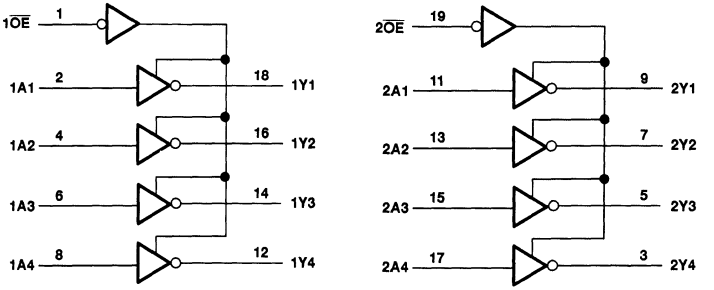
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DW package ..... 1.6 W
N package ..... 1.3 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HCT240			SN74HCT240			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time		0		500	0		500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT240		SN74HCT240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	4.5 V	4.4	4.499		4.4		4.4		V
		I_{OH} = –6 mA		3.98	4.3		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
		I_{OL} = 6 mA			0.17	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0,	V_I = V_{IH} or V_{IL}	5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}†	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i			4.5 V to 5.5 V		3	10		10		10	pF

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT240		SN74HCT240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5 V		13	25		37		32	ns
			5.5 V		12	23		33		29	
t_{en}	$\overline{OE}$	Y	4.5 V		21	35		53		44	ns
			5.5 V		19	32		48		40	
t_{dis}	$\overline{OE}$	Y	4.5 V		19	35		53		44	ns
			5.5 V		18	32		48		40	
t_t		Y	4.5 V		8	12		18		15	ns
			5.5 V		7	11		16		14	

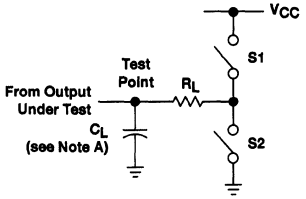
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT240		SN74HCT240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5 V		20	42		63		53	ns
			5.5 V		19	38		56		48	
t_{en}	$\overline{OE}$	Y	4.5 V		25	52		79		65	ns
			5.5 V		22	47		71		59	
t_t		Y	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

operating characteristics, T_A = 25°C

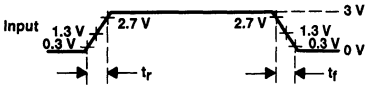
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	No load	40	pF

PARAMETER MEASUREMENT INFORMATION

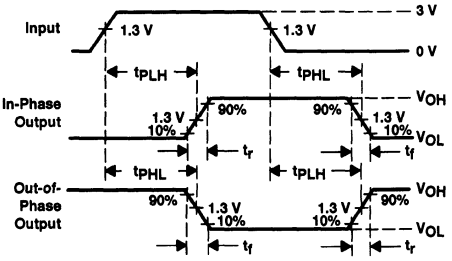


LOAD CIRCUIT

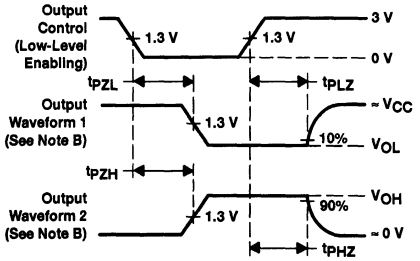
PARAMETER		RL	CL	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES



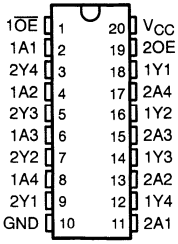
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

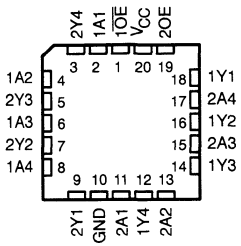
Figure 1. Load Circuit and Voltage Waveforms

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **High-Current Outputs Drive up to 15 LSTTL Loads**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC241 . . . J OR W PACKAGE
SN74HC241 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC241 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The 'HC241 are organized as two 4-bit buffers/drivers with separate output-enable ($1\overline{OE}$ and 2OE) inputs. When $1\overline{OE}$ is low or 2OE is high, the device passes noninverted data from the A inputs to the Y outputs. When $1\overline{OE}$ is high or 2OE is low, the outputs for the respective buffers/drivers are in the high-impedance state.

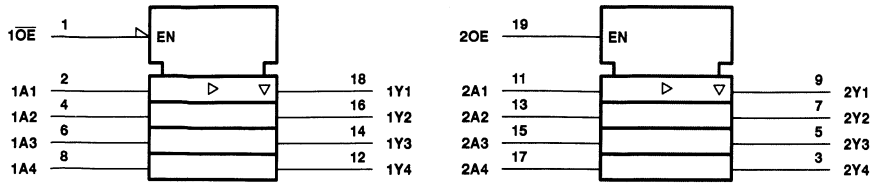
The SN54HC241 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC241 is characterized for operation from –40°C to 85°C.

FUNCTION TABLES

INPUTS		OUTPUT
$1\overline{OE}$	1A	1Y
L	H	H
L	L	L
H	X	Z

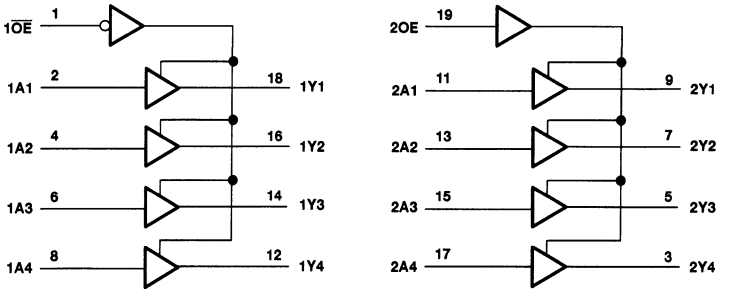
INPUTS		OUTPUT
2OE	2A	2Y
H	H	H
H	L	L
L	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DW package ..... 1.6 W
N package ..... 1.3 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC241			SN74HC241			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC241		SN74HC241		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0		6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC241		SN74HC241		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		39	115		170		145	ns
			4.5 V		12	23		34		29	
			6 V		11	20		29		25	
t_{en}	$\overline{OE}$ or OE	Y	2 V		60	150		225		190	ns
			4.5 V		17	30		45		38	
			6 V		15	26		38		32	
t_{dis}	$\overline{OE}$ or OE	Y	2 V		40	150		225		190	ns
			4.5 V		18	30		45		38	
			6 V		17	26		38		32	
t_t		Y	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

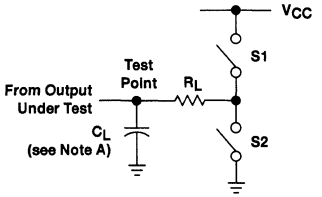
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC241		SN74HC241		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		50	165		245		210	ns
			4.5 V		16	33		49		42	
			6 V		14	28		42		35	
t_{en}	$\overline{OE}$ or OE	Y	2 V		100	200		300		250	ns
			4.5 V		20	40		60		50	
			6 V		17	34		51		43	
t_t		Y	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

operating characteristics, T_A = 25°C

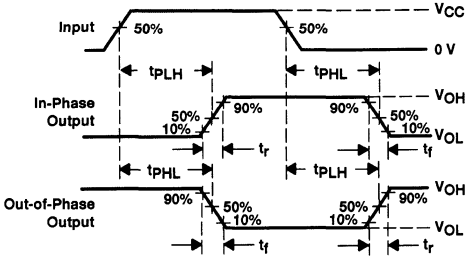
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	No load	35	pF

PARAMETER MEASUREMENT INFORMATION

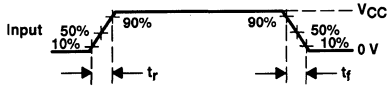


LOAD CIRCUIT

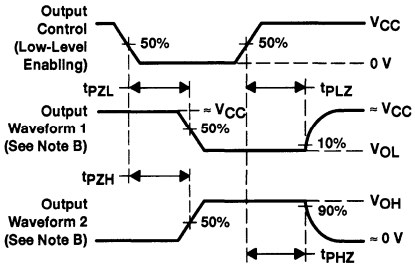
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

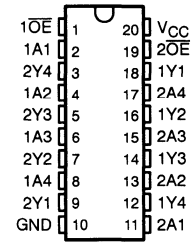
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **High-Current Outputs Drive up to 15 LSTTL Loads**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

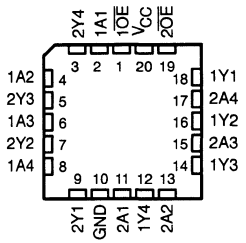
These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The 'HC244 are organized as two 4-bit buffers/drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes noninverted data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The SN54HC244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC244 is characterized for operation from –40°C to 85°C.

SN54HC244 . . . J OR W PACKAGE
SN74HC244 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



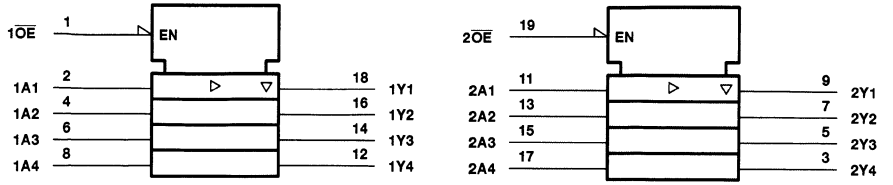
SN54HC244 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each buffer/driver)

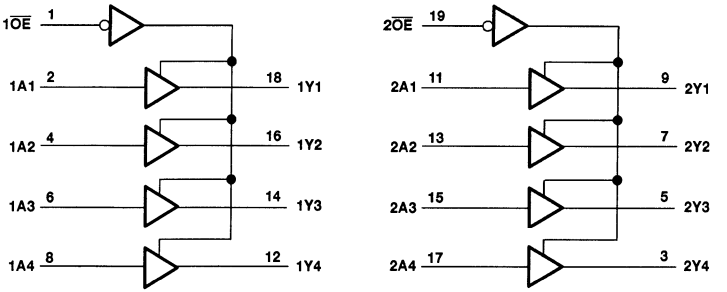
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC244			SN74HC244			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC244		SN74HC244		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0,	V_I = V_{IH} or V_{IL}	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC244		SN74HC244		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		40	115		170		145	ns
			4.5 V		13	23		34		29	
			6 V		11	20		29		25	
t_{en}	$\overline{OE}$	Y	2 V		75	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_{dis}	$\overline{OE}$	Y	2 V		75	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_t		Y	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

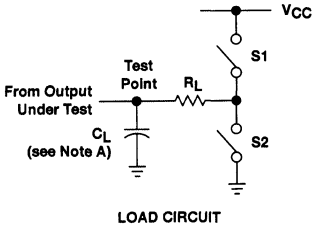
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC244		SN74HC244		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		56	165		245		210	ns
			4.5 V		18	33		49		42	
			6 V		15	28		42		35	
t_{en}	$\overline{OE}$	Y	2 V		100	200		300		250	ns
			4.5 V		20	40		60		50	
			6 V		17	34		51		43	
t_t		Y	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

operating characteristics, T_A = 25°C

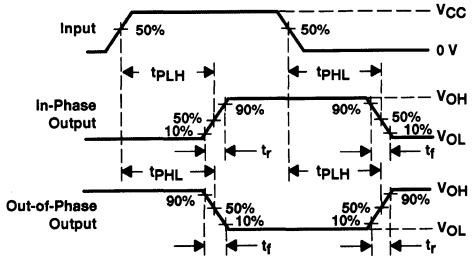
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	No load	35	pF

PARAMETER MEASUREMENT INFORMATION

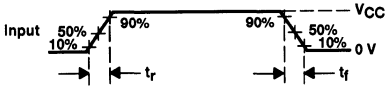


LOAD CIRCUIT

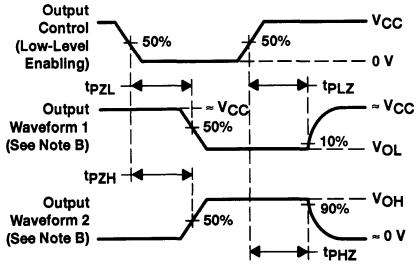
PARAMETER		RL	CL	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



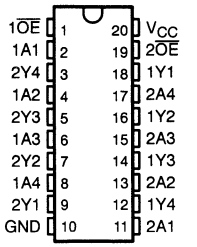
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

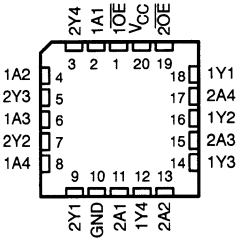
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **High-Current Outputs Drive up to 15 LSTTL Loads**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HCT244 . . . J OR W PACKAGE
SN74HCT244 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54HCT244 . . . FK PACKAGE
(TOP VIEW)



description

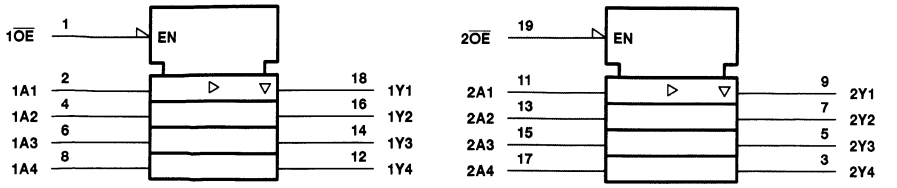
These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The 'HCT244 are organized as two 4-bit buffers/drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes noninverted data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The SN54HCT244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT244 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer/driver)

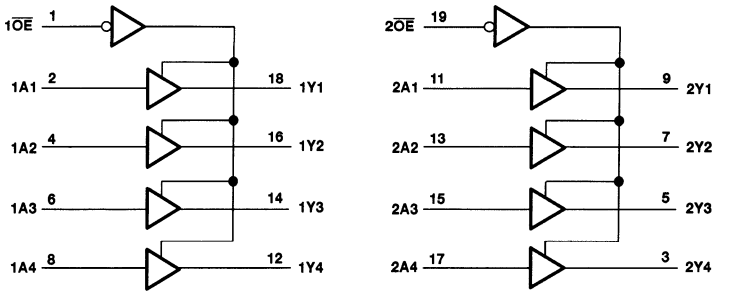
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HCT244			SN74HCT244			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time		0		500	0		500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT244		SN74HCT244		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	4.5 V	4.4	4.499		4.4		4.4		V
		I_{OH} = –6 mA		3.98	4.3		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
		I_{OL} = 6 mA			0.17	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0,	V_I = V_{IH} or V_{IL}	5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}†	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i			4.5 V to 5.5 V		3	10		10		10	pF

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT244		SN74HCT244		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5 V		15	28		42		35	ns
			5.5 V		13	25		38		32	
t_{en}	$\overline{OE}$	Y	4.5 V		21	35		53		44	ns
			5.5 V		19	32		48		40	
t_{dis}	$\overline{OE}$	Y	4.5 V		19	35		53		44	ns
			5.5 V		18	32		48		40	
t_t		Y	4.5 V		8	12		18		15	ns
			5.5 V		7	11		16		14	

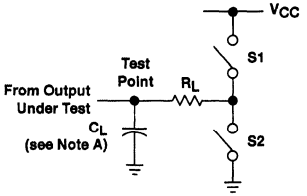
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT244		SN74HCT244		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5 V		21	45		68		56	ns
			5.5 V		18	40		61		51	
t_{en}	$\overline{OE}$	Y	4.5 V		25	52		79		65	ns
			5.5 V		22	47		71		59	
t_t		Y	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

operating characteristics, T_A = 25°C

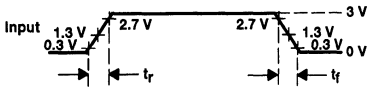
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	No load	40	pF

PARAMETER MEASUREMENT INFORMATION

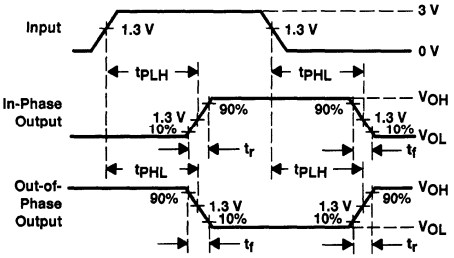


LOAD CIRCUIT

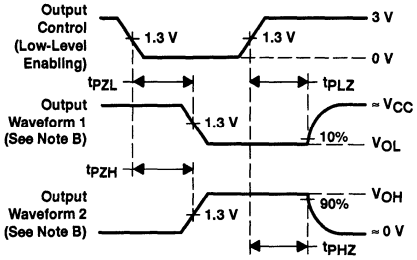
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **High-Current 3-State Outputs Drive Bus Lines Directly or up to 15 LSTTL Loads**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

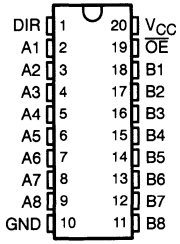
description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

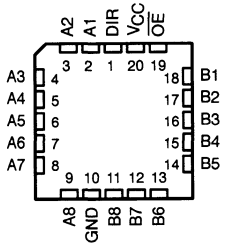
The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

The SN54HC245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC245 is characterized for operation from –40°C to 85°C.

SN54HC245 . . . J OR W PACKAGE
SN74HC245 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



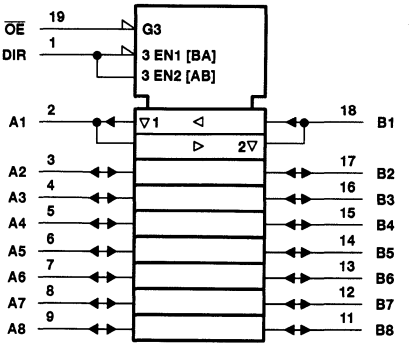
SN54HC245 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

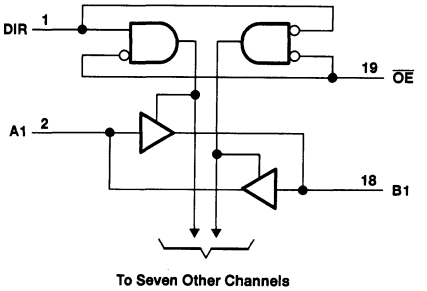
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC245			SN74HC245			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC245		SN74HC245		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
				4.5 V	4.4	4.499		4.4		4.4		
				6 V	5.9	5.999		5.9		5.9		
			I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
			I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}		V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
				4.5 V		0.001	0.1		0.1		0.1	
				6 V		0.001	0.1		0.1		0.1	
			I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
			I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	DIR or $\overline{OE}$	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	A or B	V_O = V_{CC} or 0		6 V		±0.01	±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i	DIR or $\overline{OE}$			2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC245		SN74HC245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		40	105		160		130	ns
			4.5 V		15	21		32		26	
			6 V		12	18		27		22	
t_{en}	$\overline{OE}$	A or B	2 V		125	230		340		290	ns
			4.5 V		23	46		68		58	
			6 V		20	39		58		49	
t_{dis}	$\overline{OE}$	A or B	2 V		74	200		300		250	ns
			4.5 V		25	40		60		50	
			6 V		21	34		51		43	
t_t		A or B	2 V		20	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

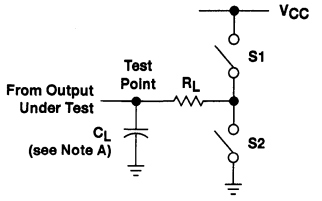
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC245		SN74HC245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		54	135		200		170	ns
			4.5 V		18	27		40		34	
			6 V		15	23		34		29	
t_{en}	$\overline{OE}$	A or B	2 V		150	270		405		335	ns
			4.5 V		31	54		81		67	
			6 V		25	46		69		56	
t_t		A or B	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

operating characteristics, T_A = 25°C

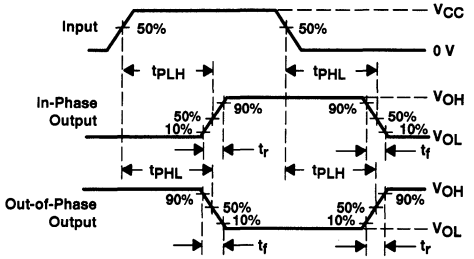
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	No load	40	pF

PARAMETER MEASUREMENT INFORMATION

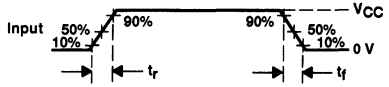


LOAD CIRCUIT

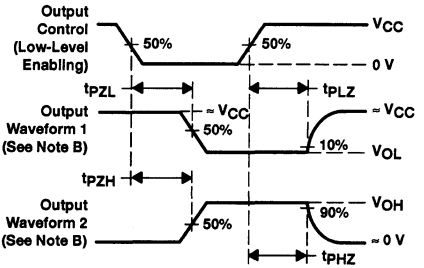
PARAMETER		RL	CL	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **High-Current 3-State Outputs Drive Bus Lines Directly or up to 15 LSTTL Loads**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

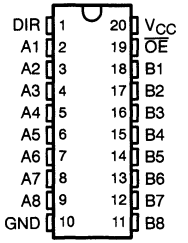
description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

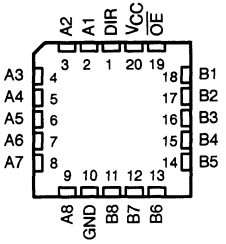
The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

The SN54HCT245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT245 is characterized for operation from –40°C to 85°C.

SN54HCT245 . . . J OR W PACKAGE
SN74HCT245 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



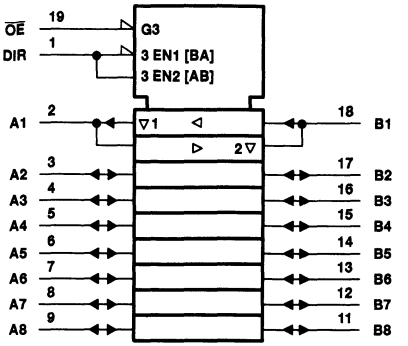
SN54HCT245 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

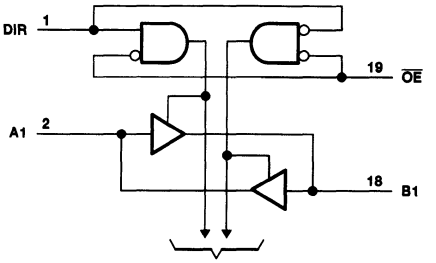
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HCT245			SN74HCT245			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time		0		500	0		500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT245		SN74HCT245		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 μA	4.5 V	4.4	4.499		4.4		4.4		V
			I_{OH} = –6 mA		3.98	4.3		3.7		3.84		
V_{OL}		$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
			I_{OL} = 6 mA			0.17	0.26		0.4		0.33	
I_I	DIR or $\overline{OE}$	$V_I = V_{CC}$ or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	A or B	$V_O = V_{CC}$ or 0		5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}		$V_I = V_{CC}$ or 0,	I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡		One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i§	DIR or $\overline{OE}$			4.5 V to 5.5 V		3	10		10		10	pF

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.
§ Parameter C_i does not apply to transceiver I/O ports.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT245		SN74HCT245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		16	22		33		28	ns
			5.5 V		14	20		30		25	
t_{en}	$\overline{OE}$	A or B	4.5 V		25	46		69		58	ns
			5.5 V		22	41		62		52	
t_{dis}	$\overline{OE}$	A or B	4.5 V		26	40		60		50	ns
			5.5 V		23	36		54		45	
t_t		A or B	4.5 V		9	12		18		15	ns
			5.5 V		8	11		16		14	

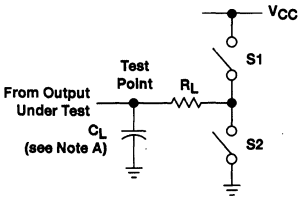
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT245		SN74HCT245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		20	30		45		38	ns
			5.5 V		18	27		41		34	
t_{en}	$\overline{OE}$	A or B	4.5 V		36	59		89		74	ns
			5.5 V		30	53		80		67	
t_t		A or B	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

operating characteristics, T_A = 25°C

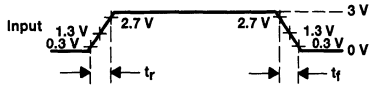
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	No load	40	pF

PARAMETER MEASUREMENT INFORMATION

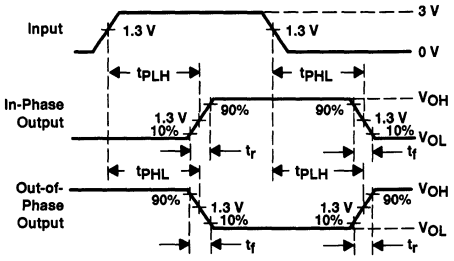


LOAD CIRCUIT

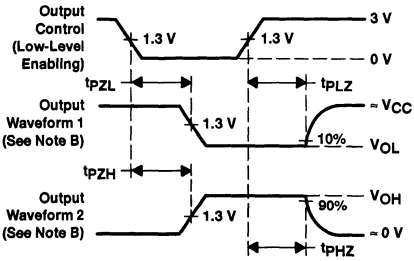
PARAMETER		RL	CL	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES



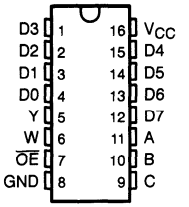
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

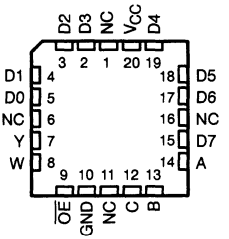
Figure 1. Load Circuit and Voltage Waveforms

- **3-State Version of 'HC151**
- **High-Current 3-State Outputs Interface Directly With System Bus or Can Drive up to 15 LSTTL Loads**
- **Perform Parallel-to-Serial Conversion**
- **Complementary Outputs Provide True and Inverted Data**
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC251 . . . J OR W PACKAGE
SN74HC251 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC251 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These data selectors/multiplexers contain full binary decoding to select 1-of-8 data sources and feature strobe-controlled complementary 3-state outputs.

The 3-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at the high-impedance state), the low impedance of the single enabled output drives the bus line to a high or low logic level. Both outputs are controlled by the output-enable ($\overline{OE}$) input. The outputs are disabled when $\overline{OE}$ is high.

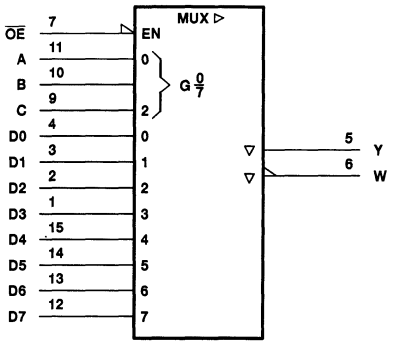
The SN54HC251 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC251 is characterized for operation from –40°C to 85 °C.

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			$\overline{OE}$		
C	B	A		Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

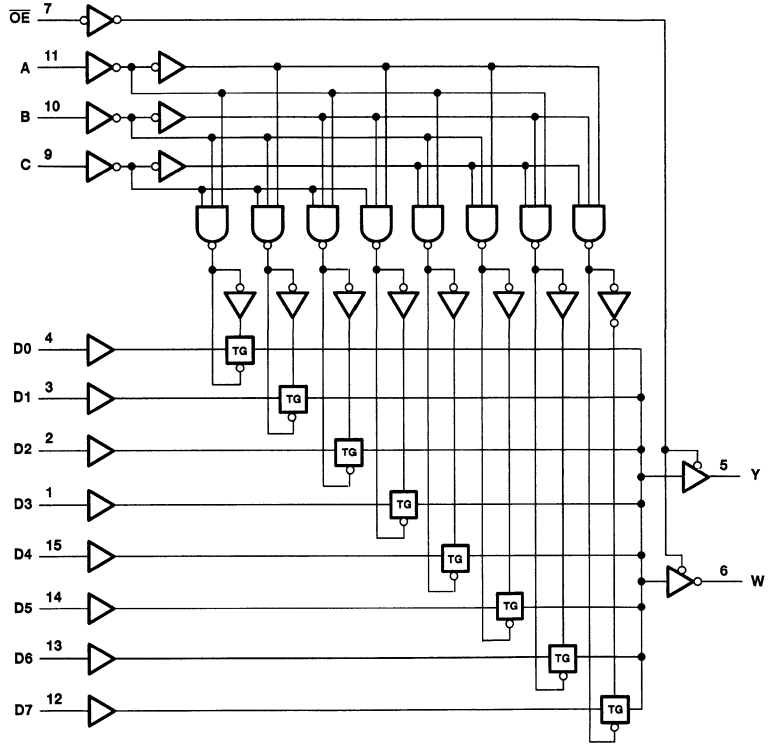
D0, D1 . . . D7 = the level of the respective D input

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC251			SN74HC251			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC251		SN74HC251		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0,	V_I = V_{IH} or V_{IL}	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC251		SN74HC251		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	W or Y	2 V		58	205		300		256	ns
			4.5 V		21	41		60		51	
			6 V		19	35		51		44	
	Any D	W or Y	2 V		44	195		283		244	
			4.5 V		17	39		57		49	
			6 V		15	33		48		41	
t_{en}	$\overline{OE}$	W or Y	2 V		30	145		210		181	ns
			4.5 V		10	29		42		36	
			6 V		9	25		36		31	
t_{dis}	$\overline{OE}$	W or Y	2 V		25	195		283		244	ns
			4.5 V		15	39		57		49	
			6 V		14	33		48		41	
t_t		W or Y	2 V		20	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

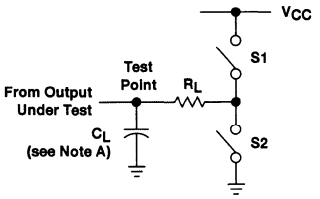
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC251		SN74HC251		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	W or Y	2 V		72	300		450		375	ns
			4.5 V		25	60		90		75	
			6 V		22	52		77		65	
	Any D	W or Y	2 V		59	300		450		375	
			4.5 V		21	60		90		75	
			6 V		18	52		77		65	
t_{en}	$\overline{OE}$	W or Y	2 V		50	230		340		285	ns
			4.5 V		17	46		68		57	
			6 V		15	40		58		50	
t_t		W or Y	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

operating characteristics, T_A = 25°C

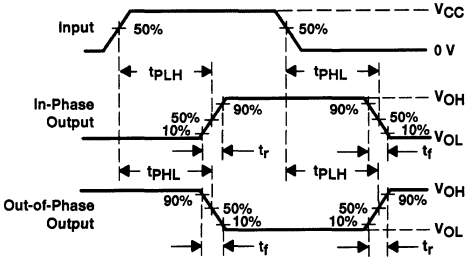
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	70	pF

PARAMETER MEASUREMENT INFORMATION

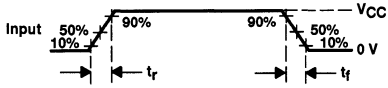


LOAD CIRCUIT

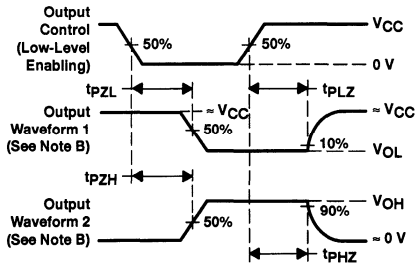
PARAMETER		RL	CL	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

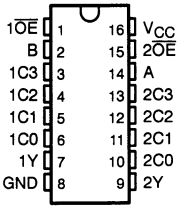
Figure 1. Load Circuit and Voltage Waveforms

SN54HC253, SN74HC253
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

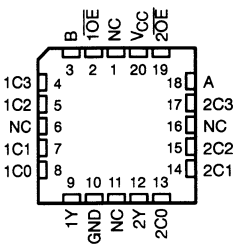
SCLS133A – DECEMBER 1982 – REVISED JANUARY 1996

- **3-State Version of 'HC153**
- **High-Current Inverting Outputs Drive up to 15 LSTTL Loads**
- **Permit Multiplexing from n Lines to One Line**
- **Perform Parallel-to-Serial Conversion**
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC253 . . . J OR W PACKAGE
SN74HC253 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC253 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

Each of these data selectors/multiplexers contain inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate output-control inputs are provided for each of the two 4-line sections.

The 3-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at the high-impedance state), the low impedance of the single enabled output drives the bus line to a high or low logic level. Each output has its own output-enable ($\overline{OE}$) input. The outputs are disabled when their respective $\overline{OE}$ is high.

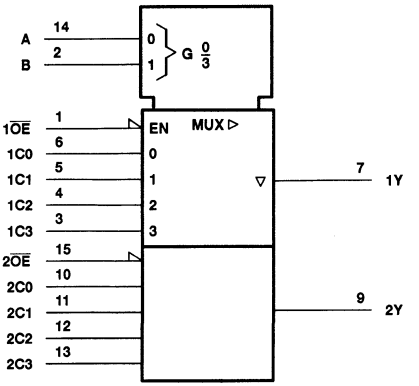
The SN54HC253 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC253 is characterized for operation from –40°C to 85 °C.

FUNCTION TABLE

INPUTS							OUTPUT
SELECT†		DATA				$\overline{OE}$	Y
B	A	C0	C1	C2	C3		
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

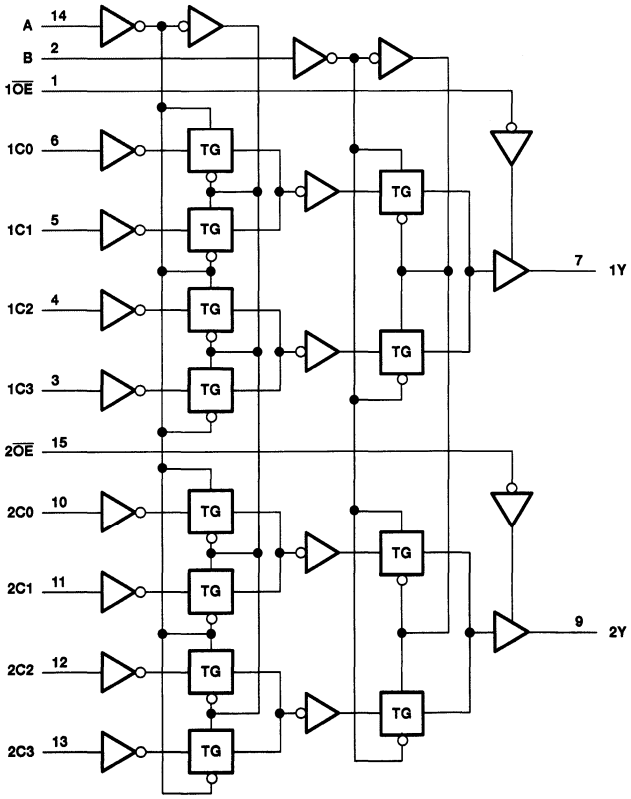
† Select inputs A and B are common to both sections.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC253			SN74HC253			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC253		SN74HC253		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0				±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC253		SN74HC253		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Any Y	2 V		62	150		225		190	ns
			4.5 V		19	30		45		38	
			6 V		16	26		38		32	
	Data (Any C)	Y	2 V		54	126		210		175	
			4.5 V		16	28		42		35	
			6 V		13	23		36		30	
t_{en}	$\overline{OE}$	Y	2 V		28	100		150		125	ns
			4.5 V		11	20		30		25	
			6 V		9	17		26		21	
t_{dis}	$\overline{OE}$	Y	2 V		21	135		203		170	ns
			4.5 V		14	30		45		38	
			6 V		12	35		38		31	
t_t		Y	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

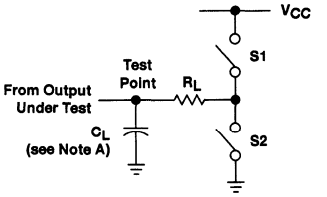
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC253		SN74HC253		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Any Y	2 V		76	235		355		295	ns
			4.5 V		23	47		71		59	
			6 V		20	41		60		51	
	Data (Any C)	Y	2 V		68	220		335		275	
			4.5 V		20	44		67		55	
			6 V		17	38		57		51	
t_{en}	$\overline{OE}$	Y	2 V		44	185		280		230	ns
			4.5 V		16	37		56		46	
			6 V		14	32		48		40	
t_t		Y	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

operating characteristics, T_A = 25°C

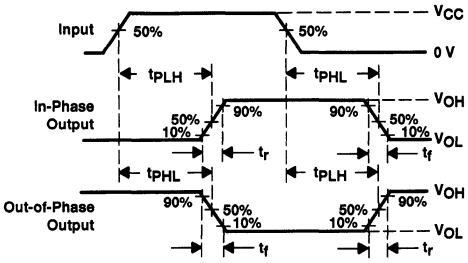
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per multiplexer	No load	45	pF

PARAMETER MEASUREMENT INFORMATION

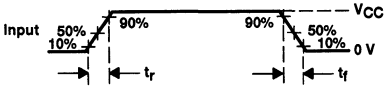


LOAD CIRCUIT

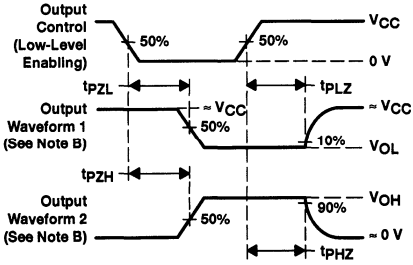
PARAMETER		RL	CL	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



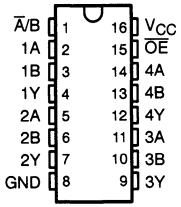
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

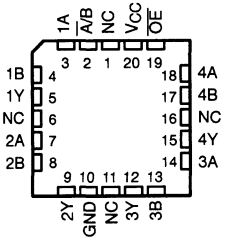
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Provide Bus Interface From Multiple Sources in High-Performance Systems**
- **High-Current 3-State Outputs Interface Directly With System Bus**
- **Buffered Inputs and Outputs**
- **Package Options Include Ceramic Chip Carriers (FK) and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HCT257 . . . J PACKAGE
SN74HCT257 . . . N PACKAGE
(TOP VIEW)



SN54HCT257 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

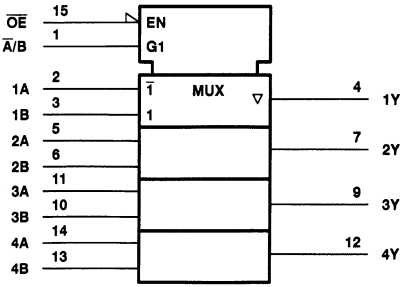
The 'HCT257 are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable ($\overline{OE}$) input is at the high logic level.

The SN54HCT257 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT257 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

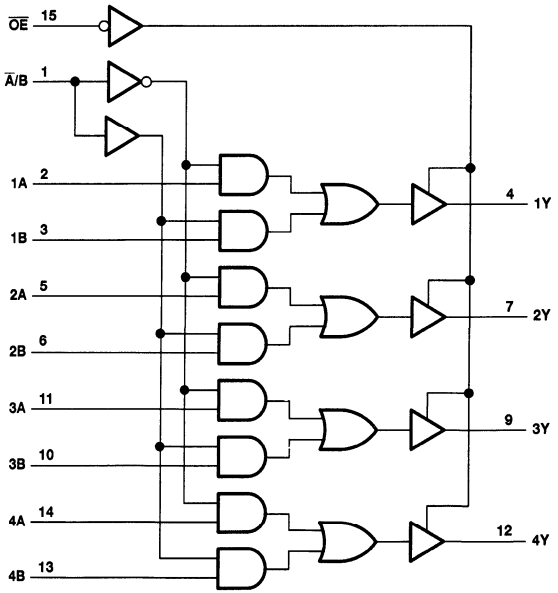
INPUTS				OUTPUT
$\overline{OE}$	SELECT $\overline{A}$/B	DATA A	DATA B	Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the J and N packages.

logic diagram (positive logic)



Pin numbers shown are for the J and N packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HCT257			SN74HCT257			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time		0		500	0		500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT257		SN74HCT257		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 µA	4.5 V	4.4	4.499		4.4		4.4		V
		I_{OH} = –6 mA		3.98	4.3		3.7		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	4.5 V		0.001	0.1		0.1		0.1	V
		I_{OL} = 6 mA			0.17	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	$V_O = V_{CC}$ or 0,	$V_I = V_{IH}$ or V_{IL}	5.5 V		±0.01	±0.5		±10		±5	µA
I_{CC}	$V_I = V_{CC}$ or 0,	I_O = 0	5.5 V			8		160		80	µA
ΔI_{CC}‡	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i			4.5 V to 5.5 V		3	10		10*		10	pF

* On products compliant to MIL-STD-883C, Class B, this parameter is not production tested.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT257		SN74HCT257		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	4.5 V		20	30		45		38	ns
			5.5 V		17	27		40		34	
	$\overline{A}$/B	Y	4.5 V		20	30		45		38	
			5.5 V		17	27		40		34	
t_{en}	$\overline{OE}$	Y	4.5 V		20	30		45		38	ns
			5.5 V		17	27		40		34	
t_{dis}	$\overline{OE}$	Y	4.5 V		20	30		45		38	ns
			5.5 V		17	27		40		34	
t_t		Any	4.5 V		8	15		22		19	ns
			5.5 V		7	14		21		17	

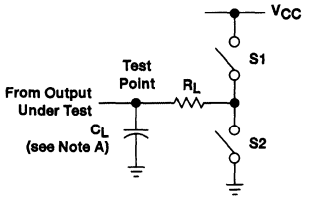
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT257		SN74HCT257		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	4.5 V		22	38		57		48	ns
			5.5 V		19	35		53		44	
	$\overline{A}$/B	Y	4.5 V		22	38		57		48	
			5.5 V		19	35		53		44	
t_{en}	$\overline{OE}$	Y	4.5 V		23	40		60		50	ns
			5.5 V		20	38		57		48	
t_t		Any	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

operating characteristics, T_A = 25°C

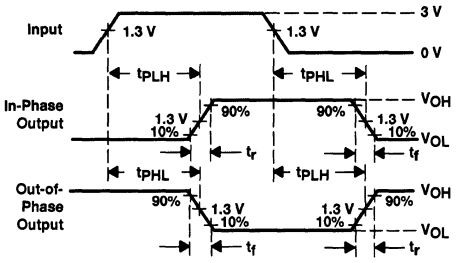
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	13	pF

PARAMETER MEASUREMENT INFORMATION

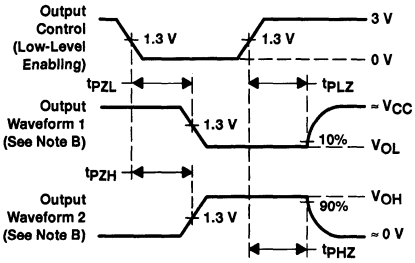


LOAD CIRCUIT

PARAMETER		RL	CL	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
OUTPUT AND 3-STATE BIDIRECTIONAL I/O
PROPAGATION DELAY TIME



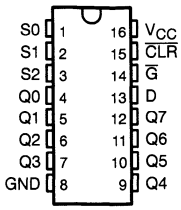
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

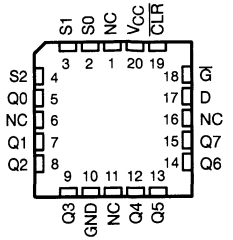
Figure 1. Load Circuit and Voltage Waveforms

- **8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion With Storage**
- **Asynchronous Parallel Clear**
- **Active-High Decoder**
- **Enable Input Simplifies Expansion**
- **Expandable for n-Bit Applications**
- **Four Distinct Functional Modes**
- **Package Options Include Plastic Small-Outline (D), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC259 . . . J OR W PACKAGE
SN74HC259 . . . D, N, OR PW PACKAGE
(TOP VIEW)



SN54HC259 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These 8-bit addressable latches are designed for general-purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

Four distinct modes of operation are selectable by controlling the clear ($\overline{CLR}$) and enable ($\overline{G}$) inputs. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch follows the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, $\overline{G}$ should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output follows the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

The SN54HC259 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC259 is characterized for operation from –40°C to 85°C.

Function Tables

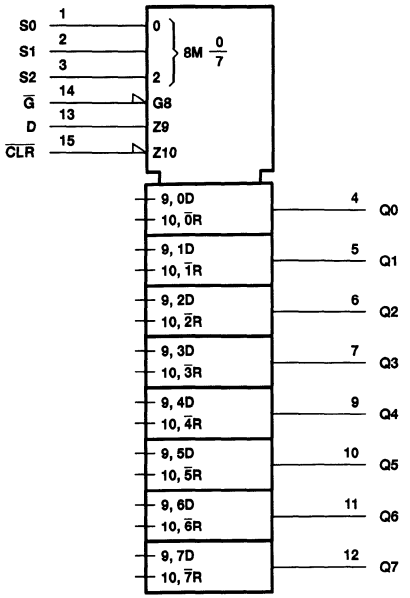
FUNCTION

INPUTS		OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
$\overline{CLR}$	$\overline{G}$			
H	L	D	Q_{iO}	Addressable latch
H	H	Q_{iO}	Q_{iO}	Memory
L	L	D	L	8-line demultiplexer
L	H	L	L	Clear

LATCH SELECTION

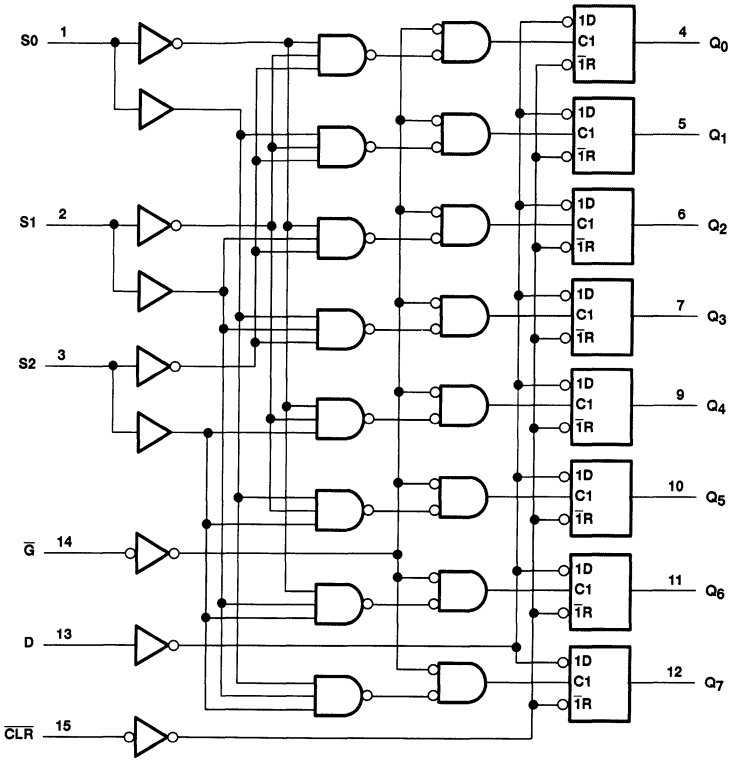
SELECT INPUTS			LATCH ADDRESSED
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

logic symbol†



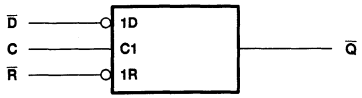
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, PW, and W packages.

logic diagram (positive logic)

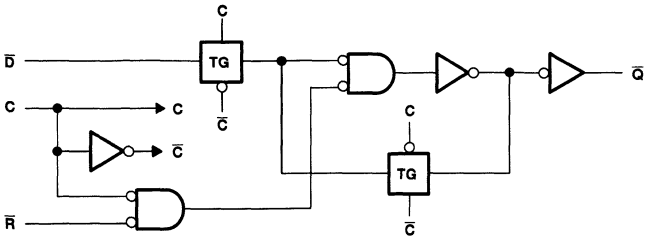


Pin numbers shown are for the D, J, N, PW, and W packages.

logic symbol, each internal latch



logic diagram, each internal latch (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.3 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC259			SN74HC259			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC259		SN74HC259		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC259		SN74HC259		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$ low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
		$\overline{G}$ low	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time, data or address before $\overline{G}\uparrow$		2 V	75		115		95		ns
			4.5 V	15		23		19		
			6 V	13		20		16		
t_h	Hold time, data or address after $\overline{G}\uparrow$		2 V	5		5		5		ns
			4.5 V	5		5		5		
			6 V	5		5		5		

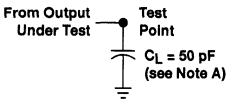
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC259		SN74HC259		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PHL}	$\overline{CLR}$	Any Q	2 V		60	150		225		190	ns
			4.5 V		18	30		45		38	
			6 V		14	26		38		32	
t_{pd}	Data	Any Q	2 V		56	130		195		165	ns
			4.5 V		17	26		39		33	
			6 V		13	22		33		28	
	Address	Any Q	2 V		74	200		300		250	
			4.5 V		21	40		60		50	
			6 V		17	34		51		43	
	$\overline{G}$	Any Q	2 V		66	170		255		215	
			4.5 V		20	34		51		43	
			6 V		16	29		43		37	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

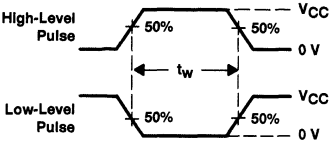
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	No load	33	pF

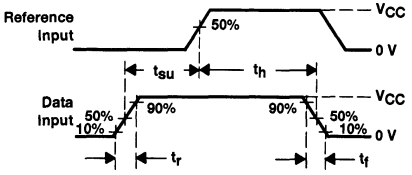
PARAMETER MEASUREMENT INFORMATION



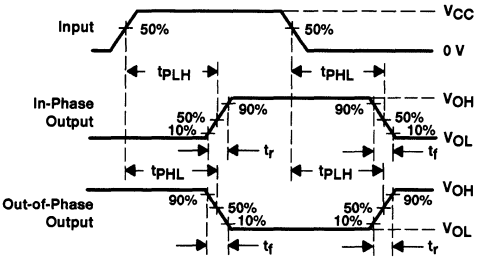
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



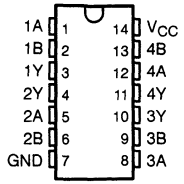
VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

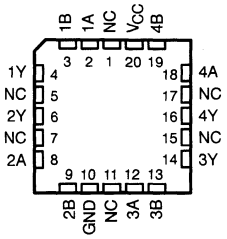
Figure 1. Load Circuit and Voltage Waveforms

- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC266 . . . J OR W PACKAGE
SN74HC266 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC266 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

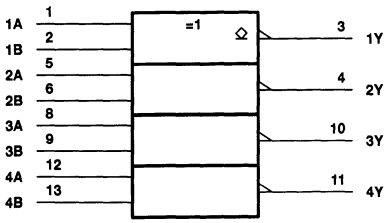
The 'HC266 are composed of four independent 2-input exclusive-NOR gates and feature open-drain outputs. They perform the Boolean function $Y = \overline{A \otimes B}$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

The SN54HC266 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC266 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram, each gate (positive logic)

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC266			SN74HC266			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC266	SN74HC266		UNIT
				MIN	TYP	MAX	MAX	MIN	MAX	
I_{OH}	$V_I = V_{IH}$ or V_{IL},	$V_O = V_{CC}$	6 V		0.01	0.5	10		5	µA
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	2 V		0.002	0.1	0.1		0.1	V
			4.5 V		0.001	0.1	0.1		0.1	
			6 V		0.001	0.1	0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26	0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26	0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		6 V		±0.1	±100	±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0,	$I_O = 0$	6 V			2	40		20	µA
C_i			2 V to 6 V		3	10	10		10	pF

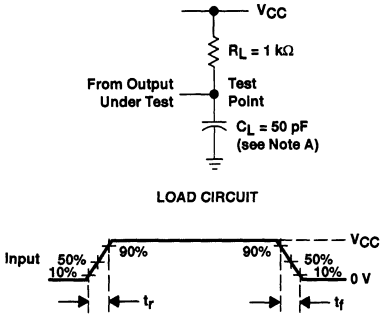
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC266		SN74HC266		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	2 V		60	125		190		155	ns
			4.5 V		13	25		38		31	
			6 V		10	23		32		26	
t_{PHL}	A or B	Y	2 V		60	100		150		125	ns
			4.5 V		13	20		30		25	
			6 V		10	17		25		21	
t_t		Y	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

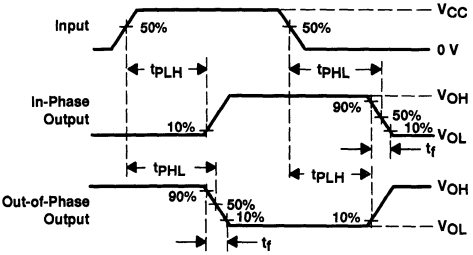
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	35	pF

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



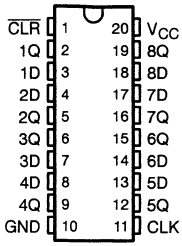
VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.

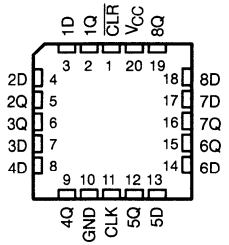
Figure 1. Load Circuit and Voltage Waveforms

- **Contain Eight Flip-Flops With Single-Rail Outputs**
- **Direct Clear Input**
- **Individual Data Input to Each Flip-Flop**
- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**
- **Package Options Include Plastic Small-Outline (DW), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC273 . . . J OR W PACKAGE
SN74HC273 . . . DW, N, OR PW PACKAGE
(TOP VIEW)



SN54HC273 . . . FK PACKAGE
(TOP VIEW)



description

These circuits are positive-edge-triggered D-type flip-flops with a direct clear ($\overline{CLR}$) input.

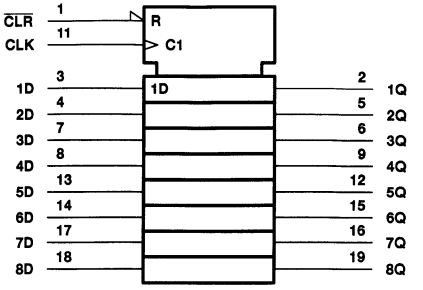
Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output.

The SN54HC273 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC273 is characterized for operation from –40°C to 85 °C.

FUNCTION TABLE
(each flip-flop)

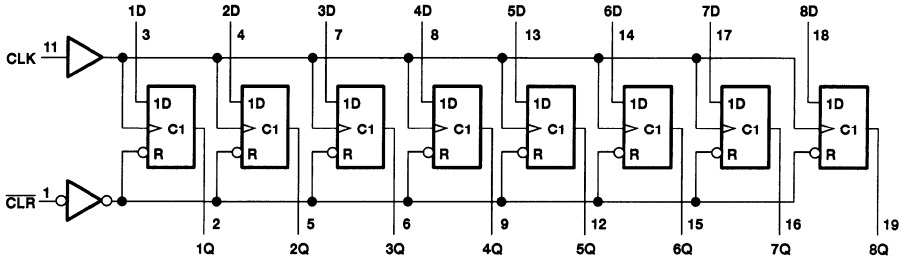
INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

logic symbol†

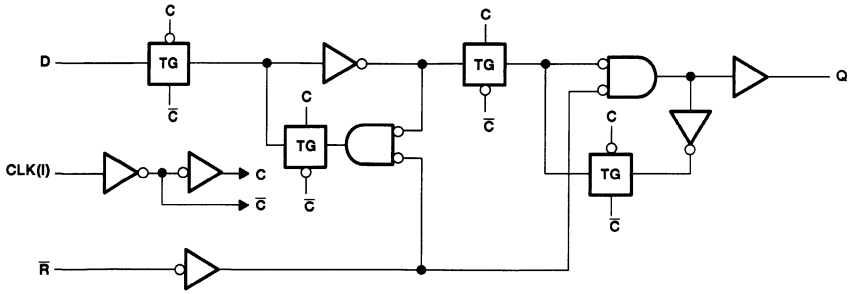


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



logic diagram, each flip-flop (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC273			SN74HC273			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC273		SN74HC273		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC273		SN74HC273		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	2 V	0	5	0	4	0	4	MHz
		4.5 V	0	27	0	18	0	21	
		6 V	0	32	0	21	0	25	
t_w	Pulse duration, $\overline{CLR}$ low	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
	Pulse duration, CLK high or low	2 V	80		120		100		
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su}	Setup time before CLK↑, Data	2 V	100		150		125		ns
		4.5 V	20		30		25		
		6 V	17		25		21		
	Setup time before CLK↑, $\overline{CLR}$ inactive	2 V	100		150		125		
		4.5 V	20		30		25		
		6 V	17		25		21		
t_h	Hold time, data after CLK↑	2 V	0		0		0		ns
		4.5 V	0		0		0		
		6 V	0		0		0		

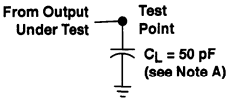
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC273		SN74HC273		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	5	11		4		4		MHz
			4.5 V	27	50		18		21		
			6 V	32	60		21		25		
t_{PHL}	$\overline{CLR}$	Any	2 V		55	160		240		200	ns
			4.5 V		15	32		48		40	
			6 V		12	27		41		34	
t_{pd}	CLK	Any	2 V		56	160		240		200	ns
			4.5 V		15	32		48		40	
			6 V		13	27		41		34	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

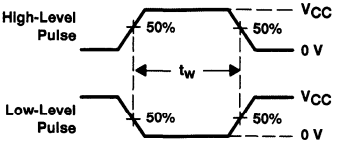
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	No load	35	pF

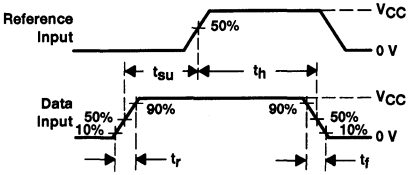
PARAMETER MEASUREMENT INFORMATION



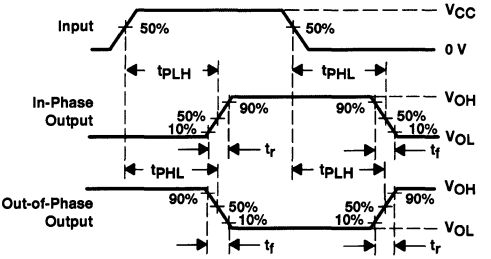
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



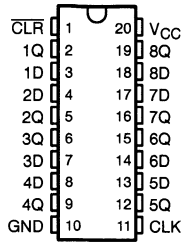
VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

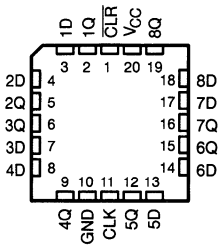
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Contain Eight D-Type Flip-Flops**
- **Direct Clear Input**
- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HCT273 . . . J OR W PACKAGE
SN74HCT273 . . . DW, N, OR PW PACKAGE
(TOP VIEW)



SN54HCT273 . . . FK PACKAGE
(TOP VIEW)



description

These devices are positive-edge-triggered D-type flip-flops with a common enable input. The 'HCT273 are similar to the 'HCT377, but feature a common clear enable ($\overline{CLR}$) input instead of a latched clock.

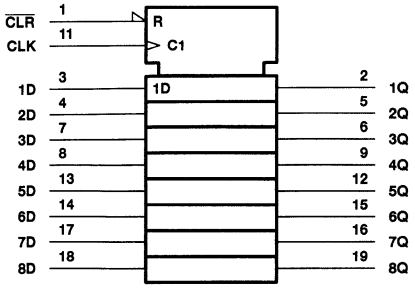
Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output. The circuits are designed to prevent false clocking by transitions at $\overline{CLR}$.

The SN54HCT273 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT273 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

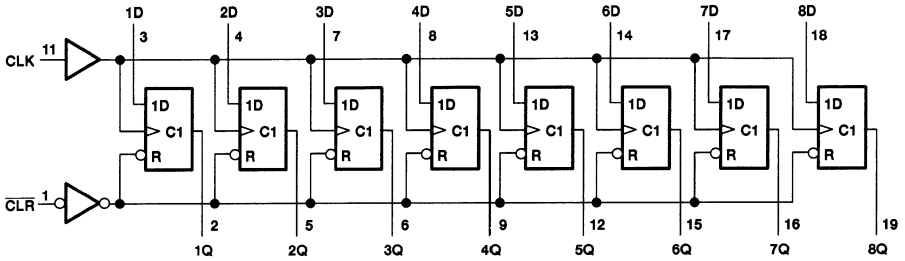
INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

logic symbol†

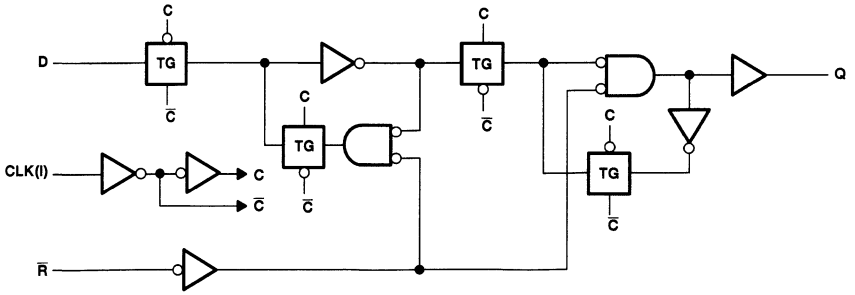


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HCT273			SN74HCT273			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT273		SN74HCT273		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 μA	4.5 V	4.4	4.499		4.4		4.4		V
		I_{OH} = –4 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0,	I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i			4.5 V to 5.5 V		3	10		10		10	pF

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HCT273		SN74HCT273		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		4.5 V	0	25	0	16	0	20	MHz
			5.5 V	0	28	0	19	0	23	
t_w	Pulse duration	CLK high or low	4.5 V	20		30		25		ns
			5.5 V	18		25		22		
		$\overline{CLR}$ low	4.5 V	16		24		20		
			5.5 V	14		20		17		
t_{su}	Setup time before CLK↑	Data	4.5 V	20		30		25		ns
			5.5 V	17		25		21		
		$\overline{CLR}$ inactive	4.5 V	20		30		25		
			5.5 V	17		25		21		
t_h	Hold time data after CLK↑		4.5 V	0		0		0		ns
			5.5 V	0		0		0		

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN54HCT273					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			4.5 V	25	31		16		MHz
			5.5 V	28	37		19		
t_{pd}	$\overline{CLR}$	Any	4.5 V		18	34		50	ns
			5.5 V		22	29		42	
t_{PHL}	$\overline{CLR}$	Any	4.5 V		17	15		50	ns
			5.5 V		15	34		42	
t_t		Any	4.5 V		8	18		22	ns
			5.5 V		7	19		21	

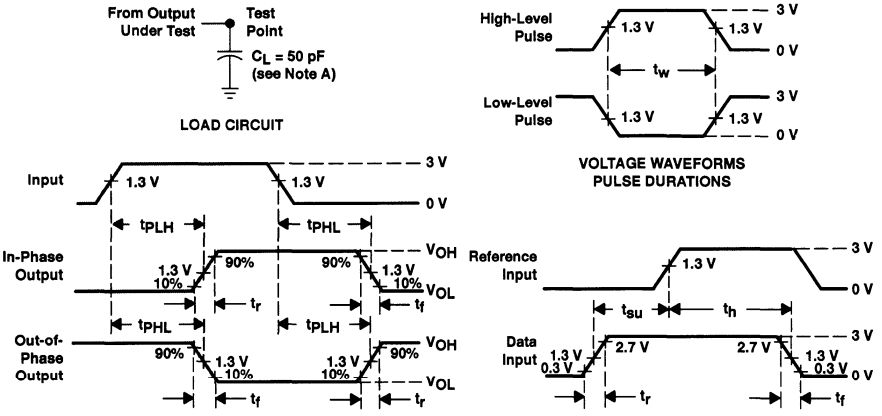
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN74HCT273					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			4.5 V	25	31		20		MHz
			5.5 V	28	37		23		
t_{pd}	$\overline{CLR}$	Any	4.5 V		18	34		42	ns
			5.5 V		22	29		36	
t_{PHL}	$\overline{CLR}$	Any	4.5 V		17	34		42	ns
			5.5 V		15	29		36	
t_t		Any	4.5 V		8	15		19	ns
			5.5 V		7	14		17	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	30	pF

PARAMETER MEASUREMENT INFORMATION

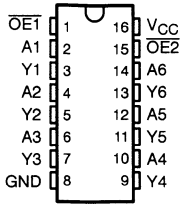


NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

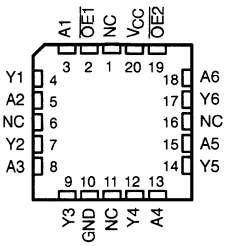
Figure 1. Load Circuit and Voltage Waveforms

- **High-Current 3-State Outputs Drive Bus Lines, Buffer Memory Address Registers, or Drive up to 15 LSTTL Loads**
- **True Outputs**
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC365 . . . J OR W PACKAGE
SN74HC365 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC365 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

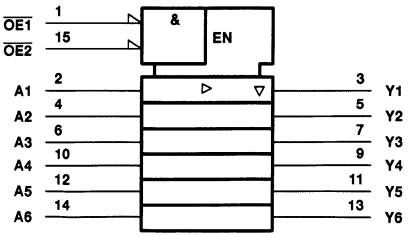
These hex buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The 'HC365 contain six independent buffers/drivers with dual-gated output-enable ($\overline{OE1}$ and $\overline{OE2}$) inputs. When $\overline{OE1}$ and $\overline{OE2}$ are both low, the device passes noninverted data from the A inputs to the Y outputs. If either (or both) output-enable terminal(s) is high, the outputs are in the high-impedance state.

The SN54HC365 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC365 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer/driver)

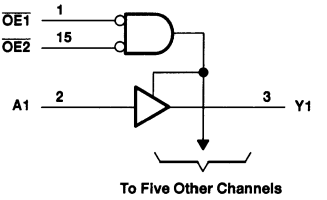
INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC365			SN74HC365			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC365		SN74HC365		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0		6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC365		SN74HC365		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		50	95		145		120	ns
			4.5 V		12	19		29		24	
			6 V		10	16		25		20	
t_{en}	$\overline{OE}$	Y	2 V		100	190		285		238	ns
			4.5 V		26	38		57		48	
			6 V		21	32		48		41	
t_{dis}	$\overline{OE}$	Y	2 V		50	175		265		240	ns
			4.5 V		21	35		53		48	
			6 V		19	30		45		41	
t_t		Any	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

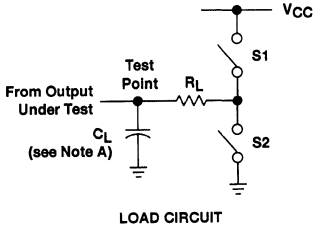
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC365		SN74HC365		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		70	120		180		150	ns
			4.5 V		17	24		36		30	
			6 V		14	20		31		25	
t_{en}	$\overline{OE}$	Y	2 V		140	230		345		285	ns
			4.5 V		30	46		69		57	
			6 V		28	39		59		48	
t_t		Any	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

operating characteristics, T_A = 25°C

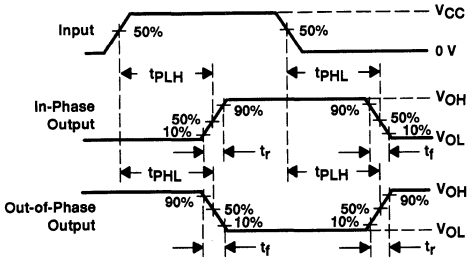
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	No load	35	pF

PARAMETER MEASUREMENT INFORMATION

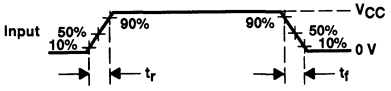


LOAD CIRCUIT

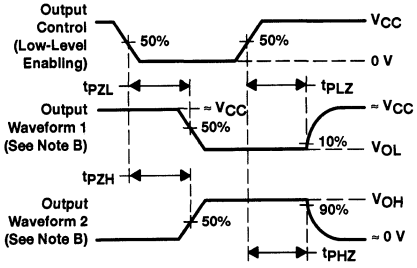
PARAMETER		RL	CL	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 1. Load Circuit and Voltage Waveforms

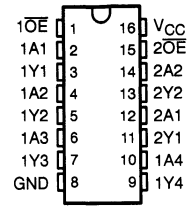
- **High-Current 3-State Outputs Drive Bus Lines, Buffer Memory Address Registers, or Drive up to 15 LSTTL Loads**
- **True Outputs**
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

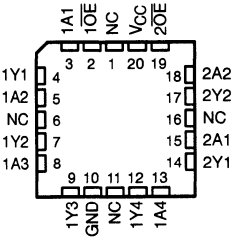
These hex buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The 'HC367 are organized as dual 4-line and 2-line buffers/drivers with active-low output-enable ($1\overline{OE}$ and $2\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes noninverted data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The SN54HC367 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC367 is characterized for operation from –40°C to 85°C.

SN54HC367 . . . J OR W PACKAGE
SN74HC367 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC367 . . . FK PACKAGE
(TOP VIEW)

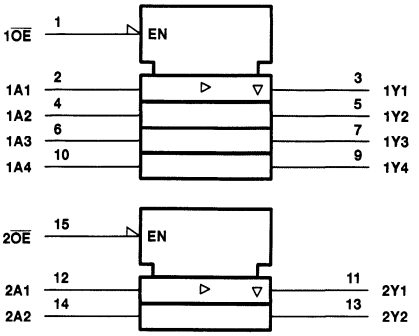


NC – No internal connection

FUNCTION TABLE
(each buffer/driver)

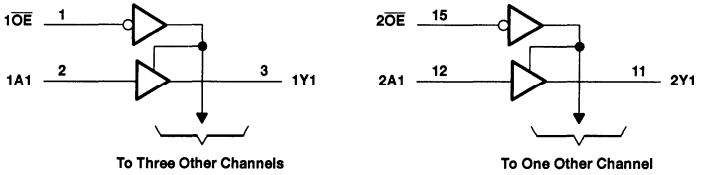
INPUTS		OUTPUT
$\overline{OE}$	A	Y
H	X	Z
L	H	H
L	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC367			SN74HC367			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC367		SN74HC367		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0		6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC367		SN74HC367		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		50	95		145		120	ns
			4.5 V		12	19		29		24	
			6 V		10	16		25		20	
t_{en}	$\overline{OE}$	Y	2 V		100	190		285		238	ns
			4.5 V		26	38		57		48	
			6 V		21	32		48		41	
t_{dis}	$\overline{OE}$	Y	2 V		50	175		265		240	ns
			4.5 V		21	35		53		48	
			6 V		19	30		45		41	
t_t		Any	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

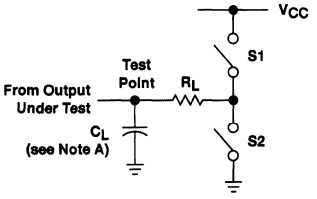
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC367		SN74HC367		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		70	120		180		150	ns
			4.5 V		17	24		36		30	
			6 V		14	20		31		25	
t_{en}	$\overline{OE}$	Y	2 V		140	230		345		285	ns
			4.5 V		30	46		69		57	
			6 V		28	39		59		48	
t_t		Any	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

operating characteristics, T_A = 25°C

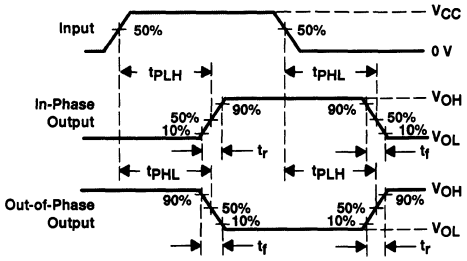
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	No load	35	pF

PARAMETER MEASUREMENT INFORMATION

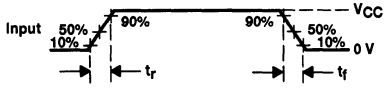


LOAD CIRCUIT

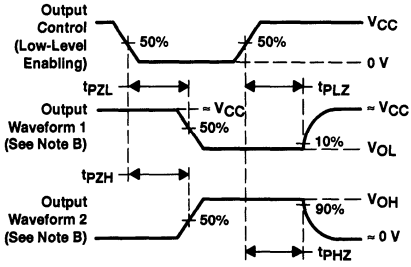
PARAMETER		RL	CL	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



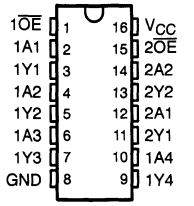
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.

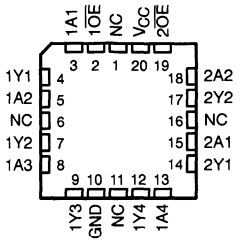
Figure 1. Load Circuit and Voltage Waveforms

- **High-Current 3-State Outputs Drive Bus Lines, Buffer Memory Address Registers, or Drive up to 15 LSTTL Loads**
- **Inverting Outputs**
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC368 . . . J OR W PACKAGE
SN74HC368 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC368 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

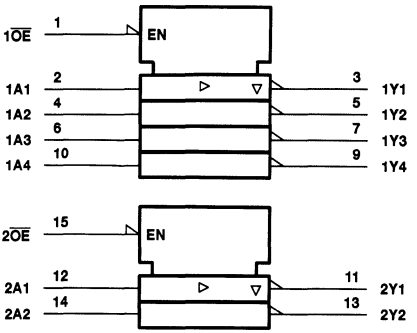
These hex buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The 'HC368 are organized as dual 4-line and 2-line buffers/drivers with active-low output-enable (1$\overline{OE}$ and 2$\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes inverted data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The SN54HC368 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC368 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer/driver)

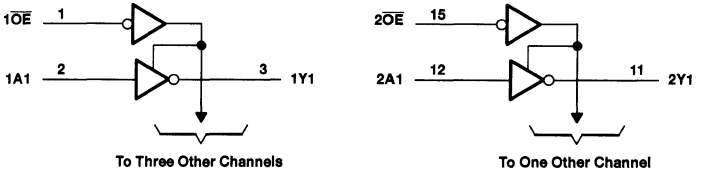
INPUTS		OUTPUT
$\overline{OE}$	A	Y
H	X	Z
L	H	L
L	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC368			SN74HC368			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC368		SN74HC368		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0		6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC368		SN74HC368		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		50	95		145		120	ns
			4.5 V		12	19		29		24	
			6 V		10	16		25		20	
t_{en}	$\overline{OE}$	Y	2 V		100	190		285		238	ns
			4.5 V		26	38		57		48	
			6 V		21	32		48		41	
t_{dis}	$\overline{OE}$	Y	2 V		50	175		265		240	ns
			4.5 V		21	35		53		48	
			6 V		19	30		45		41	
t_t		Any	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

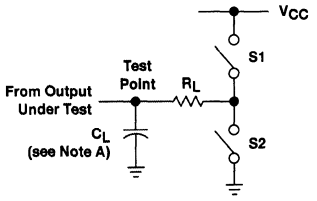
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC368		SN74HC368		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		70	120		180		150	ns
			4.5 V		17	24		36		30	
			6 V		14	20		31		25	
t_{en}	$\overline{OE}$	Y	2 V		140	230		345		285	ns
			4.5 V		30	46		69		57	
			6 V		28	39		59		48	
t_t		Any	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

operating characteristics, T_A = 25°C

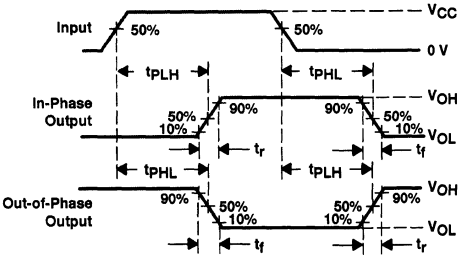
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	No load	35	pF

PARAMETER MEASUREMENT INFORMATION

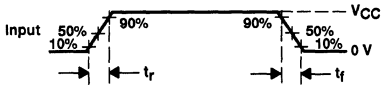


LOAD CIRCUIT

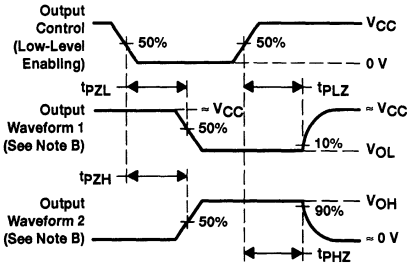
PARAMETER		RL	CL	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



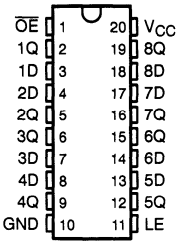
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O ≈ 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

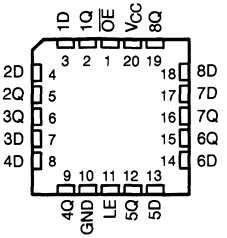
Figure 1. Load Circuit and Voltage Waveforms

- **Eight High-Current Latches In a Single Package**
- **High-Current 3-State True Outputs Can Drive up to 15 LSTTL Loads**
- **Full Parallel Access for Loading**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC373 . . . J OR W PACKAGE
SN74HC373 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54HC373 . . . FK PACKAGE
(TOP VIEW)



description

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'HC373 are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

An output-enable ($\overline{OE}$) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

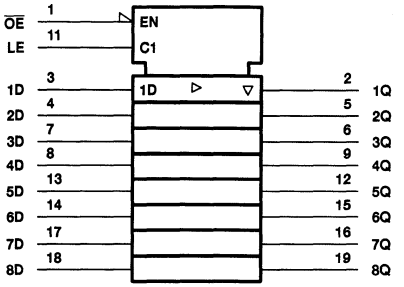
$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54HC373 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC373 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each latch)

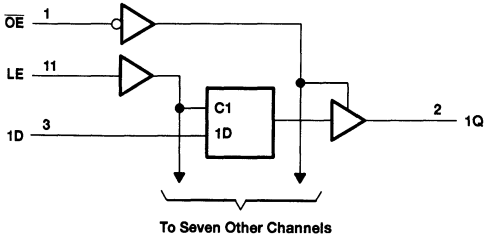
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC373			SN74HC373			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC373		SN74HC373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V			±0.1		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0		6 V			±0.01		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC373		SN74HC373		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su}	Setup time, data before LE↓	2 V	50		75		63		ns
		4.5 V	10		15		13		
		6 V	9		13		11		
t_h	Hold time, data after LE↓	2 V	20		26		24		ns
		4.5 V	10		13		12		
		6 V	10		13		12		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC373		SN74HC373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	2 V		58	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
	LE	Any Q	2 V		73	175		265		220	
			4.5 V		18	35		53		44	
			6 V		15	30		45		38	
t_{en}	$\overline{OE}$	Any Q	2 V		65	150		225		190	ns
			4.5 V		17	30		45		38	
			6 V		14	26		38		32	
t_{dis}	$\overline{OE}$	Any Q	2 V		50	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_t		Any Q	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

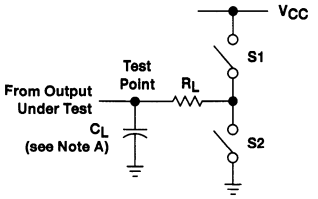
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC373		SN74HC373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	2 V		82	200		300		250	ns
			4.5 V		22	40		60		50	
			6 V		19	34		51		43	
	LE	Any Q	2 V		100	225		335		285	
			4.5 V		24	45		67		57	
			6 V		20	38		57		48	
t_{en}	$\overline{OE}$	Any Q	2 V		90	200		300		250	ns
			4.5 V		23	40		60		50	
			6 V		19	34		51		43	
t_t		Any Q	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

operating characteristics, T_A = 25°C

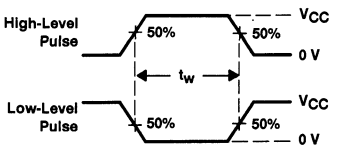
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	No load	100	pF

PARAMETER MEASUREMENT INFORMATION

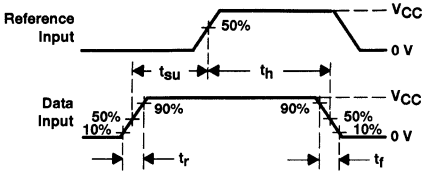


LOAD CIRCUIT

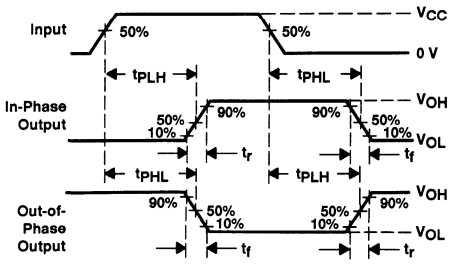
PARAMETER		RL	CL	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



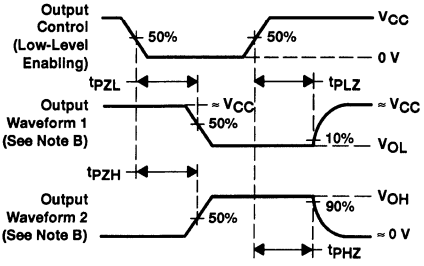
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



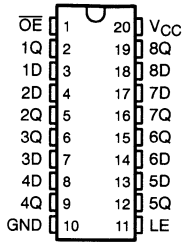
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

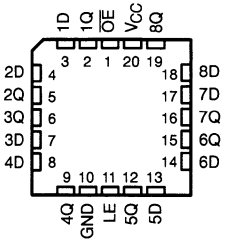
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Eight High-Current Latches in a Single Package**
- **High-Current 3-State True Outputs Can Drive up to 15 LSTTL Loads**
- **Full Parallel Access for Loading**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HCT373 . . . J OR W PACKAGE
SN74HCT373 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT373 . . . FK PACKAGE
(TOP VIEW)



description

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'HCT373 are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

An output-enable ($\overline{OE}$) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

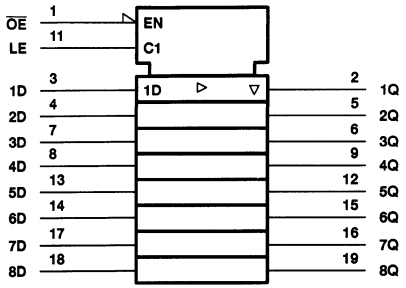
$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54HCT373 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT373 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each latch)

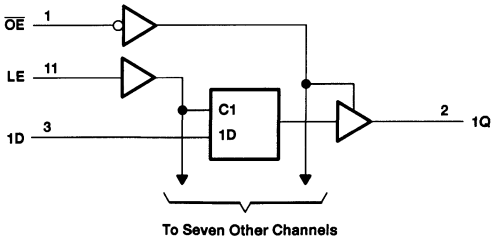
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DW package ..... 1.6 W
N package ..... 1.3 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HCT373			SN74HCT373			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time		0		500	0		500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT373		SN74HCT373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 μA	4.5 V	4.4	4.499		4.4		4.4		V
		I_{OH} = –6 mA		3.98	4.3		3.7		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
		I_{OL} = 6 mA			0.17	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	$V_O = V_{CC}$ or 0		5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}	$V_I = V_{CC}$ or 0,	I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i			4.5 V to 5.5 V		3	10		10		10	pF

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HCT373		SN74HCT373		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	4.5 V	20		30		25		ns
		5.5 V	17		27		23		
t_{su}	Setup time, data before LE↓	4.5 V	10		15		13		ns
		5.5 V	9		14		12		
t_h	Hold time, data after LE↓	4.5 V	10		10		10		ns
		5.5 V	10		10		10		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT373		SN74HCT373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	4.5 V		25	35		53		44	ns
			5.5 V		21	32		48		40	
	LE	Any Q	4.5 V		28	35		53		44	
			5.5 V		25	32		48		40	
t_{en}	$\overline{OE}$	Any Q	4.5 V		26	35		53		44	ns
			5.5 V		23	32		48		40	
t_{dis}	$\overline{OE}$	Any Q	4.5 V		23	35		53		44	ns
			5.5 V		22	32		48		40	
t_t		Any Q	4.5 V		10	12		18		15	ns
			5.5 V		9	11		16		14	

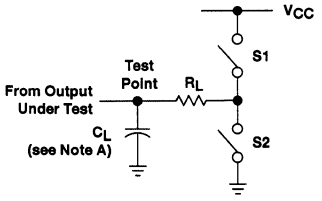
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT373		SN74HCT373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	4.5 V		32	52		79		65	ns
			5.5 V		27	47		71		59	
	LE	Any Q	4.5 V		38	52		79		65	
			5.5 V		36	47		71		59	
t_{en}	$\overline{OE}$	Any Q	4.5 V		33	52		79		65	ns
			5.5 V		28	47		71		59	
t_t		Any Q	4.5 V		18	42		63		53	ns
			5.5 V		16	38		57		48	

operating characteristics, T_A = 25°C

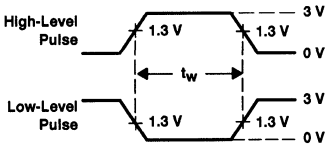
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	No load	50	pF

PARAMETER MEASUREMENT INFORMATION

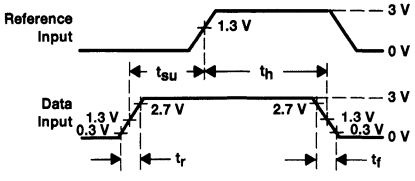


LOAD CIRCUIT

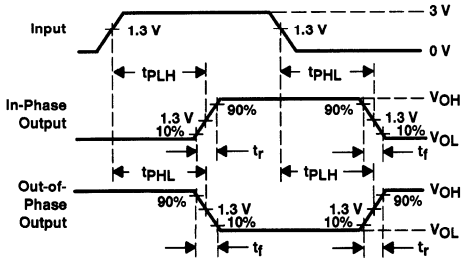
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



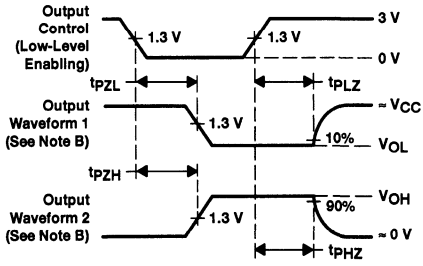
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

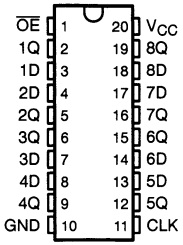
Figure 1. Load Circuit and Voltage Waveforms

SN54HC374, SN74HC374
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

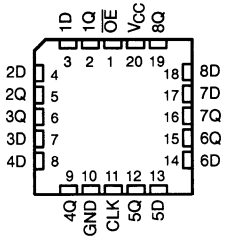
SCLS141A – DECEMBER 1982 – REVISED JANUARY 1996

- **Eight D-Type Flip-Flops in a Single Package**
- **High-Current 3-State True Outputs Can Drive up to 15 LSTTL Loads**
- **Full Parallel Access for Loading**
- **Package Options Include Plastic Small-Outline (DW), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC374 . . . J OR W PACKAGE
SN74HC374 . . . DW, N, OR PW PACKAGE
(TOP VIEW)



SN54HC374 . . . FK PACKAGE
(TOP VIEW)



description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'HC374 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

An output-enable ($\overline{OE}$) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

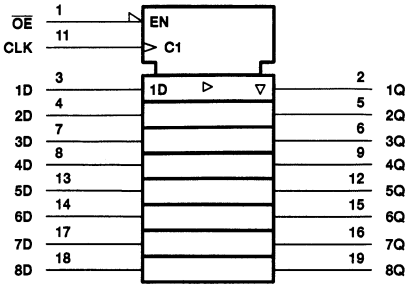
The SN54HC374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC374 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

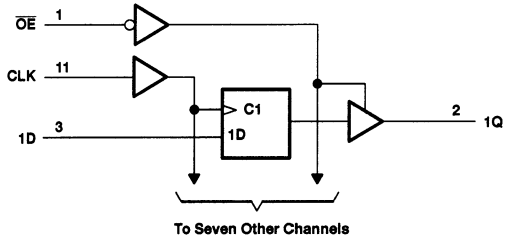
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC374			SN74HC374			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC374		SN74HC374		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0		6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC374		SN74HC374		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	2 V	0	6	0	4	0	5	MHz
		4.5 V	0	30	0	20	0	24	
		6 V	0	35	0	24	0	28	
t_w	Pulse duration, CLK high or low	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su}	Setup time, data before CLK↑	2 V	100		150		125		ns
		4.5 V	20		30		25		
		6 V	17		25		21		
t_h	Hold time, data after CLK↑	2 V	10		13		12		ns
		4.5 V	5		5		5		
		6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC374		SN74HC374		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	12		4		5		MHz
			4.5 V	30	60		20		24		
			6 V	35	70		24		28		
t_{pd}	CLK	Any Q	2 V		63	180		270		225	ns
			4.5 V		17	36		54		45	
			6 V		15	31		46		38	
t_{en}	$\overline{OE}$	Any Q	2 V		60	150		225		190	ns
			4.5 V		16	30		45		38	
			6 V		14	26		38		32	
t_{dis}	$\overline{OE}$	Any Q	2 V		36	150		225		190	ns
			4.5 V		17	30		45		38	
			6 V		16	26		38		32	
t_t		Any Q	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

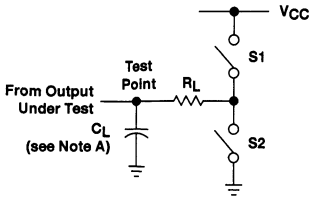
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC374		SN74HC374		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	12				5		MHz
			4.5 V	30	60				24		
			6 V	35	70				28		
t_{pd}	CLK	Any Q	2 V			80		230		290	ns
			4.5 V			22		46		58	
			6 V			19		39		58	
t_{en}	$\overline{OE}$	Any Q	2 V			70		200		250	ns
			4.5 V			25		40		50	
			6 V			22		34		51	
t_t		Any Q	2 V			45		210		265	ns
			4.5 V			17		42		53	
			6 V			13		36		53	

operating characteristics, T_A = 25°C

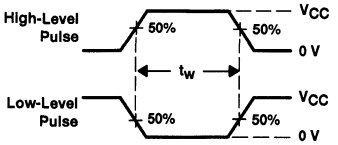
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	No load	100	pF

PARAMETER MEASUREMENT INFORMATION

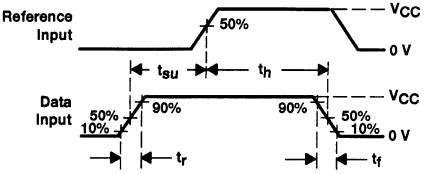


LOAD CIRCUIT

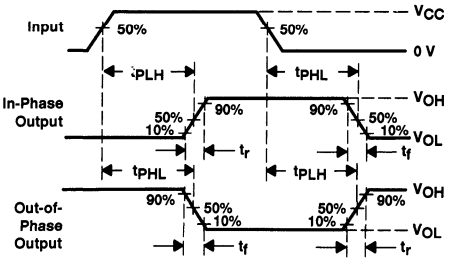
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



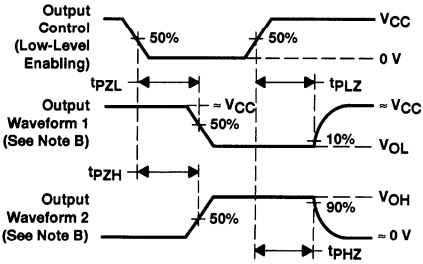
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



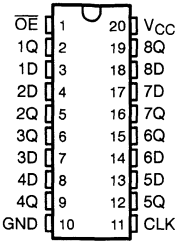
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

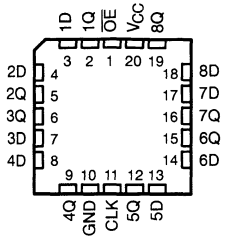
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Eight D-Type Flip-Flops in a Single Package**
- **High-Current 3-State True Outputs Can Drive up to 15 LSTTL Loads**
- **Full Parallel Access for Loading**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HCT374 . . . J OR W PACKAGE
SN74HCT374 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT374 . . . FK PACKAGE
(TOP VIEW)



description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'HCT374 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

An output-enable ($\overline{OE}$) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

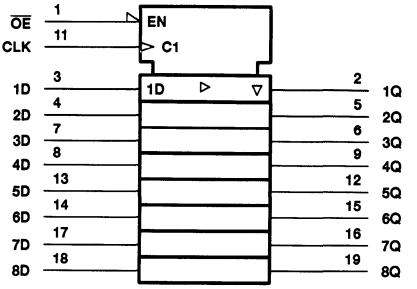
$\overline{OE}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54HCT374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT374 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

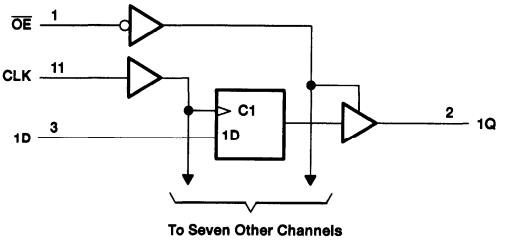
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DW package ..... 1.6 W
N package ..... 1.3 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HCT374			SN74HCT374			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time		0		500	0		500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT374		SN74HCT374		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	4.5 V	4.4	4.499		4.4		4.4		V
		I_{OH} = –6 mA		3.98	4.3		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
		I_{OL} = 6 mA			0.17	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0		5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}†	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i			4.5 V to 5.5 V		3	10		10		10	pF

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HCT374		SN74HCT374		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	4.5 V	0	31	0	21	0	25	MHz
		5.5 V	0	36	0	23	0	28	
t_w	Pulse duration, CLK high or low	4.5 V	16		24		20		ns
		5.5 V	14		22		18		
t_{su}	Setup time, data before CLK↑	4.5 V	20		30		25		ns
		5.5 V	17		27		23		
t_h	Hold time, data after CLK↑	4.5 V	10		10		10		ns
		5.5 V	10		10		10		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT374		SN74HCT374		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			4.5 V	31	36		21		25		MHz
			5.5 V	36	40		23		28		
t_{pd}	CLK	Any Q	4.5 V		30	36		54		45	ns
			5.5 V		25	32		49		41	
t_{en}	$\overline{OE}$	Any Q	4.5 V		26	30		45		38	ns
			5.5 V		23	27		41		34	
t_{dis}	$\overline{OE}$	Any Q	4.5 V		23	30		45		38	ns
			5.5 V		22	27		41		34	
t_t		Any Q	4.5 V		10	12		18		15	ns
			5.5 V		9	11		16		14	

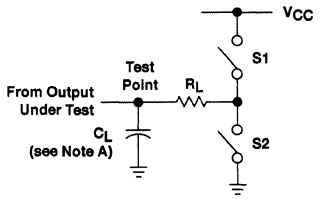
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT374		SN74HCT374		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	CLK	Any Q	4.5 V		40	46		69		58	ns
			5.5 V		35	41		62		52	
t_{en}	$\overline{OE}$	Any Q	4.5 V		34	40		60		50	ns
			5.5 V		29	36		54		45	
t_t		Any Q	4.5 V		18	42		63		53	ns
			5.5 V		16	38		57		48	

operating characteristics, T_A = 25°C

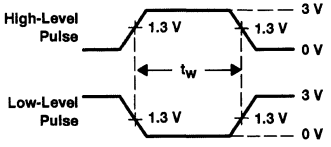
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	No load	85	pF

PARAMETER MEASUREMENT INFORMATION

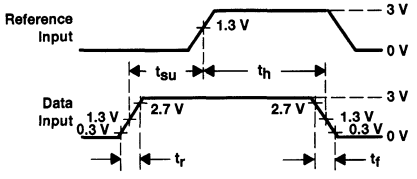


LOAD CIRCUIT

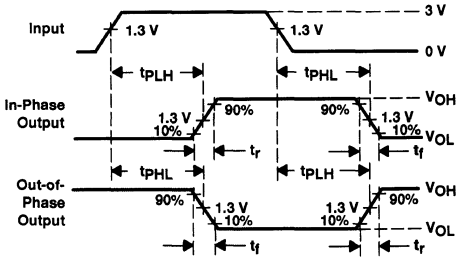
PARAMETER		RL	CL	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



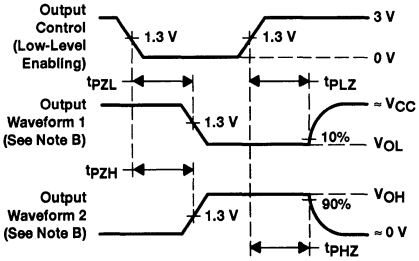
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES



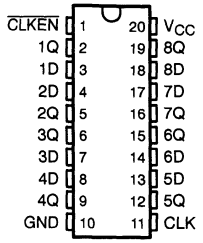
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

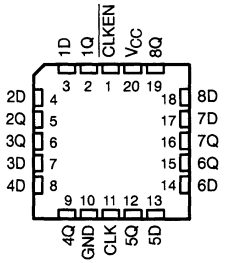
Figure 1. Load Circuit and Voltage Waveforms

- **Eight Flip-Flops With Single-Rail Outputs**
- **Clock Enable Latched to Avoid False Clocking**
- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC377 . . . J OR W PACKAGE
SN74HC377 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC377 . . . FK PACKAGE
(TOP VIEW)



description

These devices are positive-edge-triggered octal D-type flip-flops with an enable input. The 'HC377 are similar to the 'HC273 but feature a latched clock-enable ($\overline{\text{CLKEN}}$) input instead of a common clear.

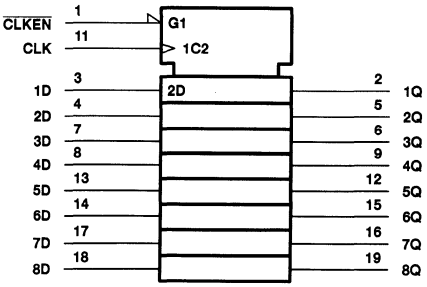
Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse if $\overline{\text{CLKEN}}$ is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output. These devices are designed to prevent false clocking by transitions at $\overline{\text{CLKEN}}$.

The SN54HC377 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC377 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

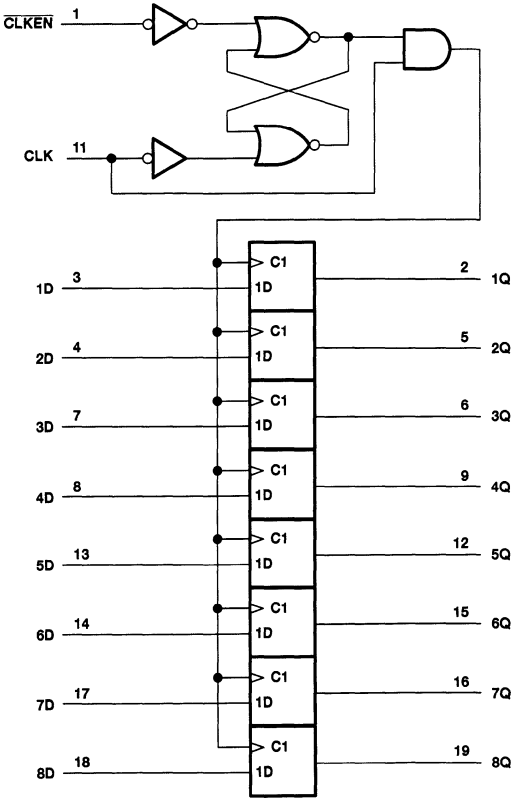
INPUTS			OUTPUT
$\overline{\text{CLKEN}}$	CLK	D	Q
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	L	X	Q_0

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DW package ..... 1.6 W
N package ..... 1.3 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC377			SN74HC377			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC377		SN74HC377		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC377		SN74HC377		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	5	0	3	0	4	MHz
			4.5 V	0	25	0	16	0	20	
			6 V	0	29	0	19	0	23	
t_w	Pulse duration, CLK high or low		2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
t_{su}	Setup time before CLK↑	D	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		$\overline{CLKEN}$ high or low	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		25		21		
t_h	Hold time after CLK↑	$\overline{CLKEN}$ inactive or active, data	2 V	5		5		5		ns
			4.5 V	5		5		5		
			6 V	5		5		5		

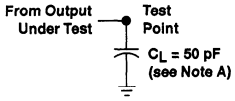
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC377		SN74HC377		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	5	11		3		4		MHz
			4.5 V	25	54		16		20		
			6 V	29	64		19		23		
t_{pd}	CLK	Any	2 V		56	160		240		200	ns
			4.5 V		15	32		48		40	
			6 V		12	27		41		34	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

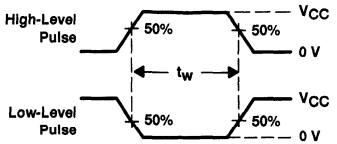
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	No load	30	pF

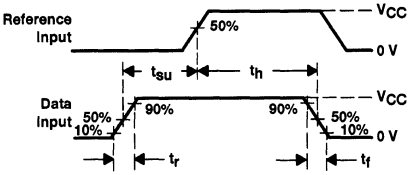
PARAMETER MEASUREMENT INFORMATION



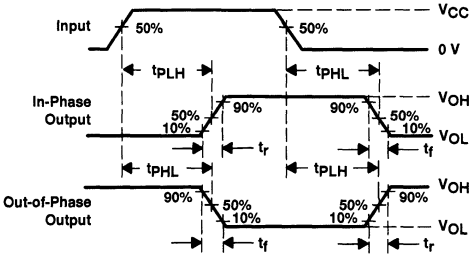
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



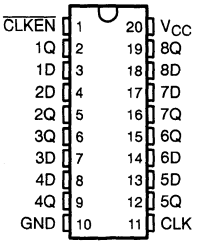
VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

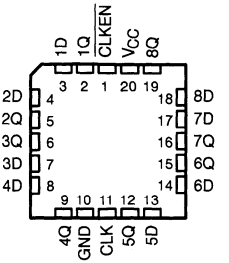
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Contain Eight Flip-Flops With Single-Rail Outputs**
- **Clock Enable Latched to Avoid False Clocking**
- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**
- **Package Options Include Plastic Small-Outline (DW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HCT377 . . . J OR W PACKAGE
SN74HCT377 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT377 . . . FK PACKAGE
(TOP VIEW)



description

These devices are positive-edge-triggered D-type flip-flops. The 'HCT377 are similar to the 'HCT273 but feature a latched clock-enable ($\overline{CLKEN}$) input instead of a common clear.

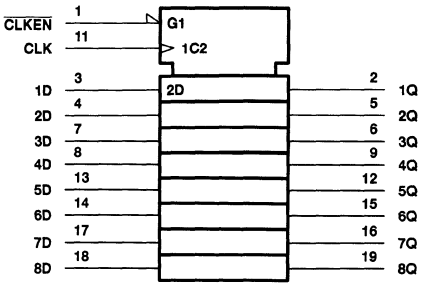
Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse if $\overline{CLKEN}$ is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output. These devices are designed to prevent false clocking by transitions at $\overline{CLKEN}$.

The SN54HCT377 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT377 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

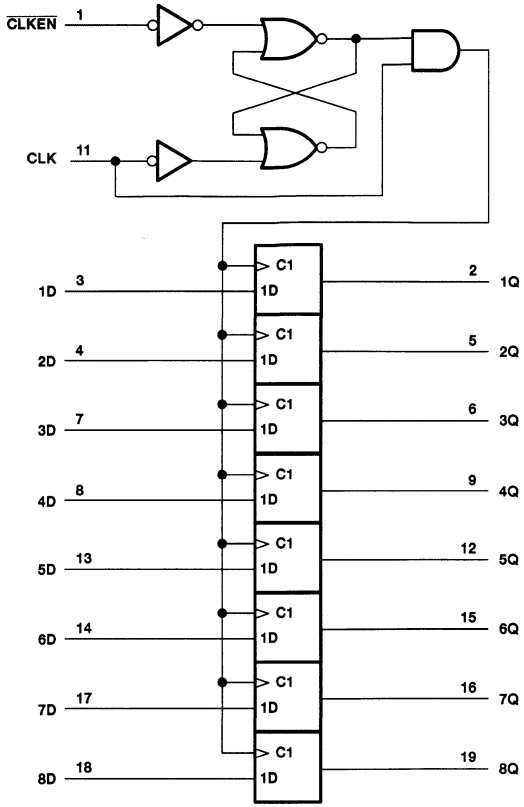
INPUTS			OUTPUT
$\overline{CLKEN}$	CLK	D	Q
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	L	X	Q_0

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DW package ..... 1.6 W
N package ..... 1.3 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HCT377			SN74HCT377			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT377		SN74HCT377		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 μA	4.5 V	4.4	4.499		4.4		4.4		V
		I_{OH} = –4 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0,	I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 0.5 V or 2.4 V, Other inputs at GND or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i			4.5 V to 5.5 V		3	10		10*		10	pF

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HCT377		SN74HCT377		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		4.5 V	0	25	0	17	0	20	MHz
			5.5 V	0	30	0	19	0	22	
t_w	Pulse duration	CLK high or low	4.5 V	20		30		25		ns
			5.5 V	18		28		23		
t_{su}	Setup time before CLK↑	Data	4.5 V	12		18		15		ns
			5.5 V	10		17		14		
		$\overline{CLKEN}$ high or low	4.5 V	12		18		15		
			5.5 V	10		17		14		
t_h	Hold time data after CLK↑	Data	4.5 V	3		3		3		ns
			5.5 V	3		3		3		
		$\overline{CLKEN}$ inactive or active	4.5 V	5		5		5		
			5.5 V	5		5		5		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN54HCT377					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			4.5 V	25	31		17		MHz
			5.5 V	30	37		19		
t_{pd}	CLK	Any	4.5 V		15	30		45	ns
			5.5 V		12	28		40	
t_t		Any	4.5 V		8	15		22	ns
			5.5 V		6	14		21	

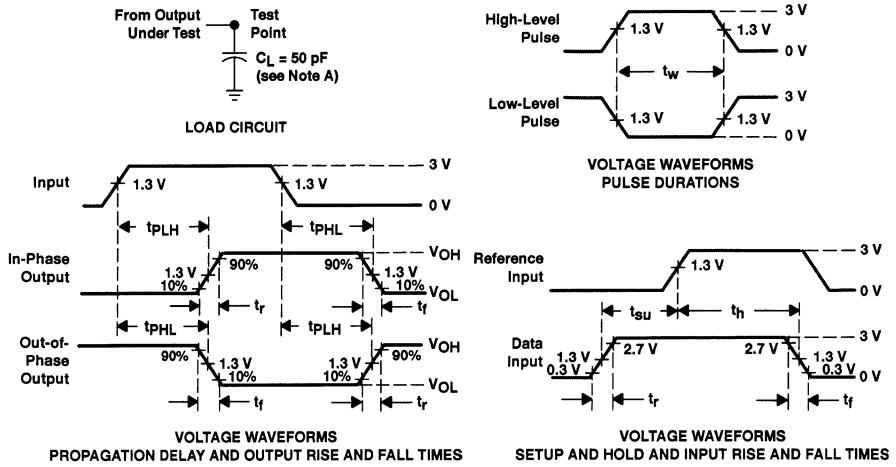
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN74HCT377					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			4.5 V	25	31		20		MHz
			5.5 V	30	37		22		
t_{pd}	CLK	Any	4.5 V		15	30		38	ns
			5.5 V		12	28		35	
t_t		Any	4.5 V		8	15		19	ns
			5.5 V		6	14		17	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	30	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

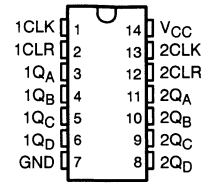
Figure 1. Load Circuit and Voltage Waveforms

SN54HC393, SN74HC393
DUAL 4-BIT BINARY COUNTERS

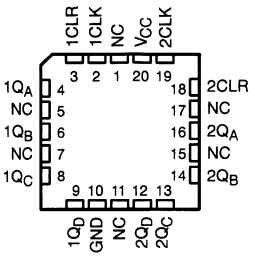
SCLS143A – DECEMBER 1982 – REVISED JANUARY 1996

- **Dual 4-Bit Binary Counters With Individual Clocks**
- **Direct Clear for Each 4-Bit Counter**
- **Can Significantly Improve System Densities by Reducing Counter Package Count by 50 Percent**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC393 . . . J OR W PACKAGE
SN74HC393 . . . D, DB, OR N PACKAGE
(TOP VIEW)



SN54HC393 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

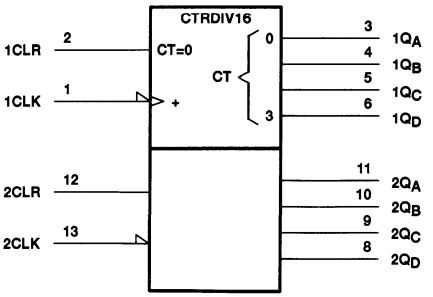
The 'HC393 contain eight flip-flops and additional gating to implement two individual 4-bit counters in a single package. The 'HC393 comprise two independent 4-bit binary counters, each having a clear (CLR) and a clock (CLK) input. N-bit binary counters can be implemented with each package, providing the capability of divide by 256. The 'HC393 have parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system timing signals.

The SN54HC393 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC393 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE COUNT SEQUENCE
(each counter)

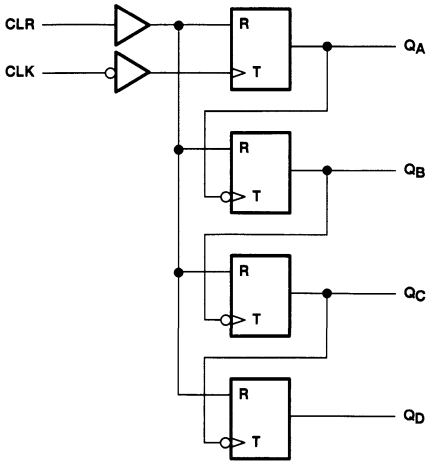
COUNT	OUTPUTS			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, and W packages.

logic diagram, each counter (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
DB package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC393			SN74HC393			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t†	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

† If this device is used in the threshold region (from V_{IL}max = 0.5 V to V_{IH}min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC393		SN74HC393		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC393		SN74HC393		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock} Clock frequency		2 V	0	6	0	4.2	0	5	MHz
		4.5 V	0	31	0	21	0	25	
		6 V	0	36	0	25	0	28	
t_w Pulse duration	CLK high or low	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		18		
	CLR high	2 V	80		120		100		
		4.5 V	16		24		20		
		6 V	14		20		18		
t_{su} Setup time, CLR inactive		2 V	25		25		25		ns
		4.5 V	5		5		5		
		6 V	5		5		5		

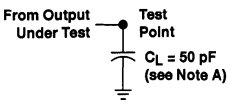
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC393		SN74HC393		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLK	Q_A	2 V	6	10		4.2		5		MHz
			4.5 V	31	50		21		25		
			6 V	36	60		25		28		
t_{pd}	CLK	Q_A	2 V		50	120		180		150	ns
			4.5 V		15	24		36		30	
			6 V		13	20		31		26	
		Q_B	2 V		72	190		285		240	
			4.5 V		22	38		57		47	
			6 V		18	32		48		40	
		Q_C	2 V		91	240		360		300	
			4.5 V		28	48		72		60	
			6 V		22	41		61		51	
		Q_D	2 V		100	290		430		360	
			4.5 V		32	58		87		72	
			6 V		24	50		74		62	
t_{PHL}	CLR	Any	2 V		45	165		250		205	ns
			4.5 V		17	33		49		41	
			6 V		14	28		42		35	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

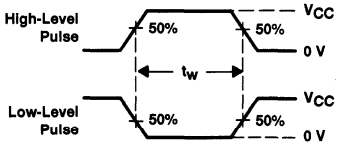
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per counter	No load	40	pF

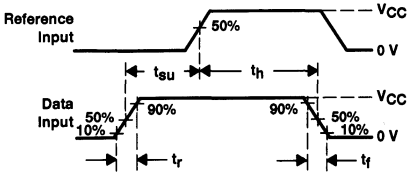
PARAMETER MEASUREMENT INFORMATION



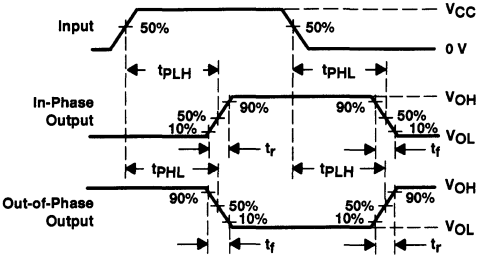
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



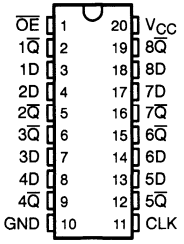
VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

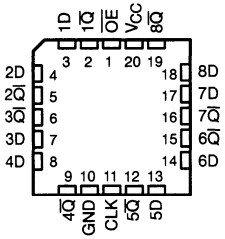
Figure 1. Load Circuit and Voltage Waveforms

- **High-Current 3-State Inverting Outputs Can Drive up to 15 LSTTL Loads**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC534 . . . J OR W PACKAGE
SN74HC534 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC534 . . . FK PACKAGE
(TOP VIEW)



description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'HC534 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the $\overline{Q}$ outputs are set to the complement of the logic states that were set up at the data (D) inputs. The 'HC534 are functionally equivalent to the 'HC374, but the 'HC534 have inverted outputs.

An output-enable ($\overline{OE}$) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

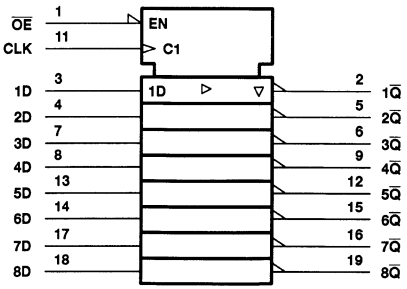
$\overline{OE}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN54HC534 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC534 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

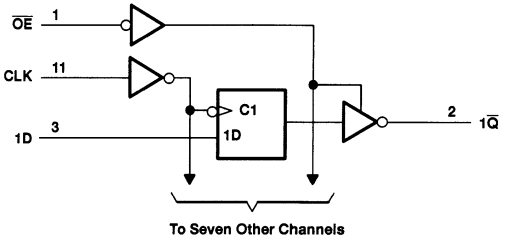
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	H or L	X	$\overline{Q}_0$
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DW package ..... 1.6 W
N package ..... 1.3 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC534			SN74HC534			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC534		SN74HC534		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0,	V_I = V_{IH} or V_{IL}	6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC534		SN74HC534		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	2 V	0	6	0	4.2	0	5	MHz
		4.5 V	0	31	0	21	0	25	
		6 V	0	36	0	25	0	29	
t_w	Pulse duration, CLK high or low	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su}	Setup time, data before CLK↑	2 V	100		150		125		ns
		4.5 V	20		30		25		
		6 V	17		26		21		
t_h	Hold time, data after CLK↑	2 V	5		5		5		ns
		4.5 V	5		5		5		
		6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC534		SN74HC534		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	11		4.2		5		MHz
			4.5 V	31	36		21		25		
			6 V	36	40		25		29		
t_{pd}	CLK	Any $\overline{Q}$	2 V		88	180		270		225	ns
			4.5 V		28	36		54		45	
			6 V		24	31		46		38	
t_{en}	$\overline{OE}$	Any $\overline{Q}$	2 V		77	150		225		190	ns
			4.5 V		26	30		45		38	
			6 V		23	26		38		32	
t_{dis}	$\overline{OE}$	Any $\overline{Q}$	2 V		51	150		225		190	ns
			4.5 V		25	30		45		38	
			6 V		23	26		38		32	
t_t		Any $\overline{Q}$	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

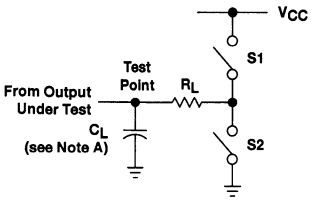
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC534		SN74HC534		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	CLK	Any $\overline{Q}$	2 V		105	230		345		290	ns
			4.5 V		35	46		69		58	
			6 V		31	39		58		49	
t_{en}	$\overline{OE}$	Any $\overline{Q}$	2 V		95	200		300		250	ns
			4.5 V		32	40		60		50	
			6 V		29	34		51		43	
t_t		Any $\overline{Q}$	2 V		60	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		14	36		53		45	

operating characteristics, T_A = 25°C

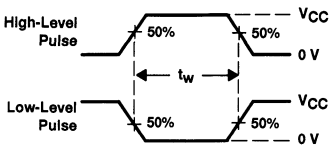
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	No load	100	pF

PARAMETER MEASUREMENT INFORMATION

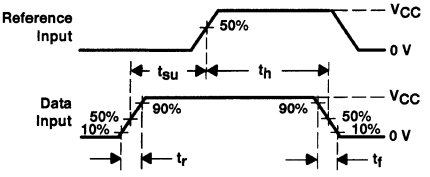


LOAD CIRCUIT

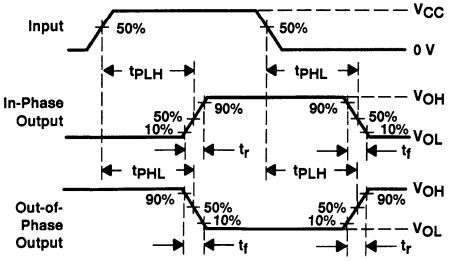
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



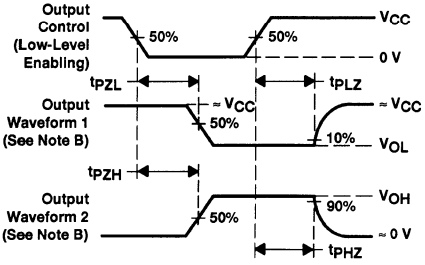
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **High-Current 3-State Outputs Drive Bus Lines Directly or up to 15 LSTTL Loads**
- **Data Flow-Through Pinout (All Inputs on Opposite Side From Outputs)**
- **Package Options Include Plastic (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

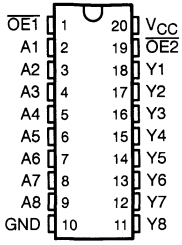
description

These octal buffers and line drivers feature the performance of the popular 'HC240 series and offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed-circuit-board layout.

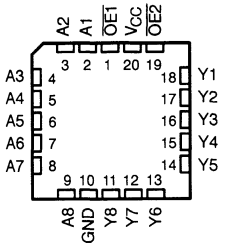
The 3-state control gate is a 2-input NOR. If either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all eight outputs are in the high-impedance state. The 'HC540 provide inverted data at the outputs.

The SN54HC540 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC540 is characterized for operation from –40°C to 85°C.

SN54HC540 . . . J OR W PACKAGE
SN74HC540 . . . DW OR N PACKAGE
(TOP VIEW)



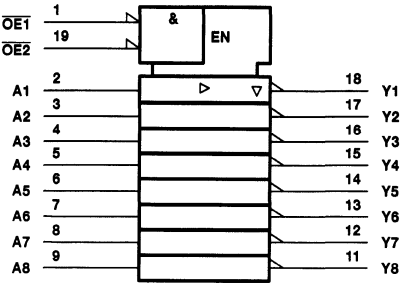
SN54HC540 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each buffer/driver)

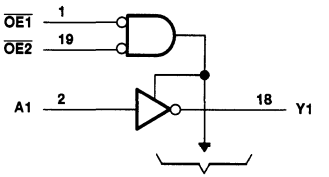
INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DW package ..... 1.6 W
N package ..... 1.3 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC540			SN74HC540			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC540		SN74HC540		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0		6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC540		SN74HC540		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		35	100		149		125	ns
			4.5 V		10	20		30		25	
			6 V		8	17		25		21	
t_{en}	$\overline{OE}$	Y	2 V		75	150		224		188	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_{dis}	$\overline{OE}$	Y	2 V		40	150		224		188	ns
			4.5 V		18	30		45		38	
			6 V		17	26		38		32	
t_t		Y	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

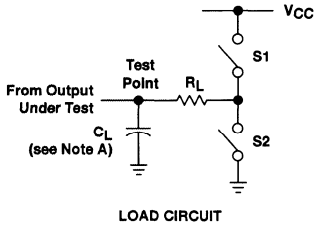
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC540		SN74HC540		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		60	150		224		188	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_{en}	$\overline{OE}$	Y	2 V		100	200		298		250	ns
			4.5 V		20	40		60		50	
			6 V		17	34		51		43	
t_t		Y	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

operating characteristics, T_A = 25°C

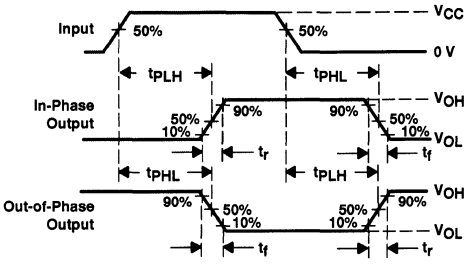
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	No load	35	pF

PARAMETER MEASUREMENT INFORMATION

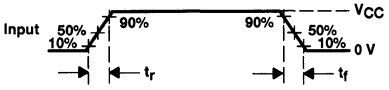


LOAD CIRCUIT

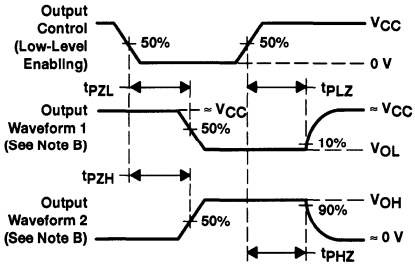
PARAMETER		RL	CL	S1	S2
ten	tPZH	1 kΩ	50 pF or 150 pF	Open	Closed
	tPZL			Closed	Open
tdis	tPHZ	1 kΩ	50 pF	Open	Closed
	tPLZ			Closed	Open
tpd or tt		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



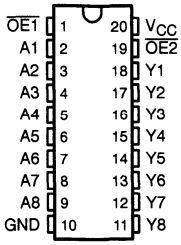
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

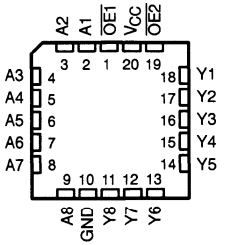
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **High-Current 3-State Outputs Interface Directly With System Bus or Can Drive up to 15 LSTTL Loads**
- **Data Flow-Through Pinout (All Inputs on Opposite Side From Outputs)**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HCT540 . . . J OR W PACKAGE
SN74HCT540 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT540 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed to have the performance of the popular 'HCT240 series and to offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly facilitates printed-circuit-board layout.

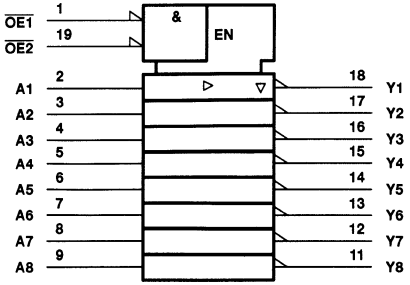
The 3-state control gate is a 2-input NOR. If either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all eight outputs are in the high-impedance state. The 'HCT540 provide inverted data at the outputs.

The SN54HCT540 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT540 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer/driver)

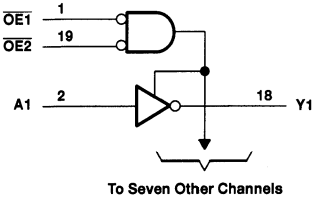
INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DW package ..... 1.6 W
N package ..... 1.3 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HCT540			SN74HCT540			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time		0		500	0		500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT540		SN74HCT540		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	4.5 V	4.4	4.499		4.4		4.4		V
		I_{OH} = –6 mA		3.98	4.3		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
		I_{OL} = 6 mA			0.17	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0,	V_I = V_{IH} or V_{IL}	5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}†	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i			4.5 V to 5.5 V		3	10		10		10	pF

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT540		SN74HCT540		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5 V		13	20		30		25	ns
			5.5 V		12	18		27		23	
t_{en}	$\overline{OE}$	Y	4.5 V		20	30		45		38	ns
			5.5 V		18	27		41		34	
t_{dis}	$\overline{OE}$	Y	4.5 V		19	30		45		38	ns
			5.5 V		18	27		41		34	
t_t		Y	4.5 V		8	12		18		15	ns
			5.5 V		7	11		16		14	

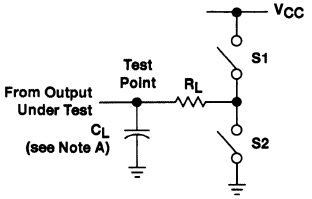
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT540		SN74HCT540		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5 V		20	30		45		38	ns
			5.5 V		19	27		41		34	
t_{en}	$\overline{OE}$	Y	4.5 V		26	40		60		50	ns
			5.5 V		25	36		54		45	
t_t		Y	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

operating characteristics, T_A = 25°C

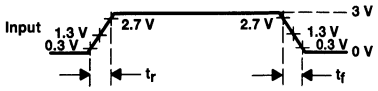
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	No load	35	pF

PARAMETER MEASUREMENT INFORMATION

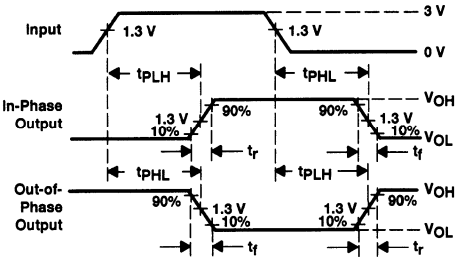


LOAD CIRCUIT

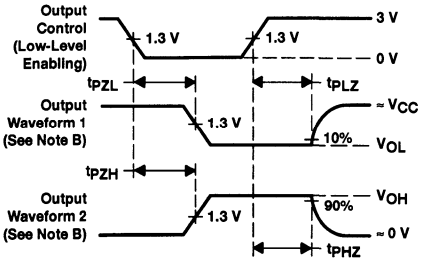
PARAMETER		RL	CL	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **High-Current 3-State Outputs Drive Bus Lines Directly or up to 15 LSTTL Loads**
- **Data Flow-Through Pinout (All Inputs on Opposite Side From Outputs)**
- **Package Options Include Plastic Small-Outline (DW), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

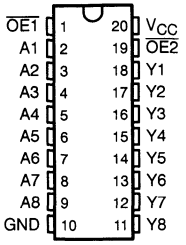
description

These octal buffers and line drivers feature the performance of the popular 'HC240 series and offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed-circuit-board layout.

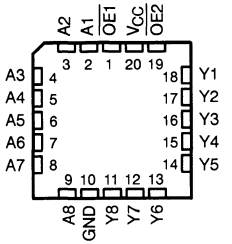
The 3-state control gate is a 2-input NOR. If either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all eight outputs are in the high-impedance state. The 'HC541 provide true data at the outputs.

The SN54HC541 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC541 is characterized for operation from –40°C to 85°C.

SN54HC541 . . . J OR W PACKAGE
SN74HC541 . . . DW, N, OR PW PACKAGE
(TOP VIEW)



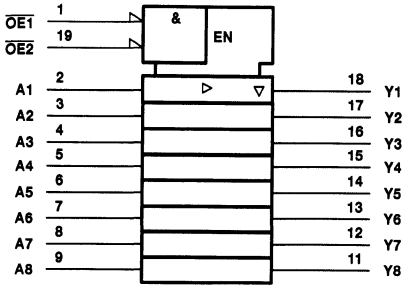
SN54HC541 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each buffer/driver)

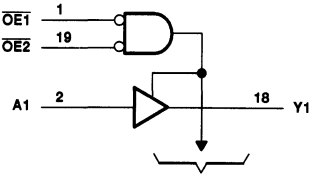
INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC541			SN74HC541			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC541		SN74HC541		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0		6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC541		SN74HC541		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		40	115		171		144	ns
			4.5 V		12	23		34		29	
			6 V		10	20		29		25	
t_{en}	$\overline{OE}$	Y	2 V		80	150		224		188	ns
			4.5 V		17	30		45		38	
			6 V		15	26		38		32	
t_{dis}	$\overline{OE}$	Y	2 V		40	150		224		188	ns
			4.5 V		18	30		45		38	
			6 V		17	26		38		32	
t_t		Y	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

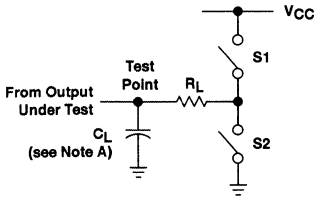
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC541		SN74HC541		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		65	165		246		206	ns
			4.5 V		16	33		49		41	
			6 V		14	28		42		35	
t_{en}	$\overline{OE}$	Y	2 V		100	200		298		250	ns
			4.5 V		20	40		60		50	
			6 V		17	34		51		43	
t_t		Y	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

operating characteristics, T_A = 25°C

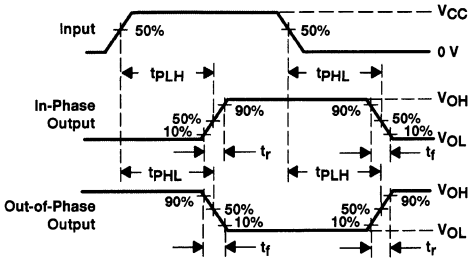
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	No load	35	pF

PARAMETER MEASUREMENT INFORMATION

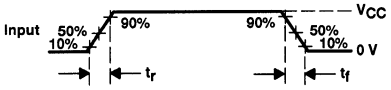


LOAD CIRCUIT

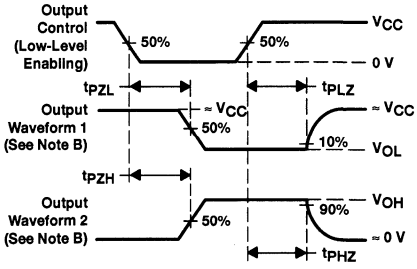
PARAMETER		RL	CL	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



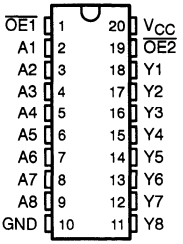
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

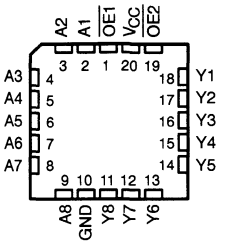
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **High-Current 3-State Outputs Interface Directly With System Bus or Can Drive up to 15 LSTTL Loads**
- **Data Flow-Through Pinout (All Inputs on Opposite Side From Outputs)**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HCT541 . . . J OR W PACKAGE
SN74HCT541 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT541 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed to have the performance of the popular 'HC240 series and to offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly facilitates printed-circuit-board layout.

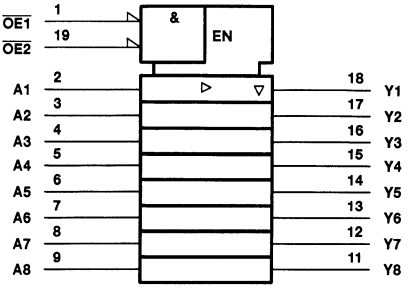
The 3-state control gate is a 2-input NOR. If either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all eight outputs are in the high-impedance state. The 'HCT541 provide true data at the outputs.

The SN54HCT541 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT541 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer/driver)

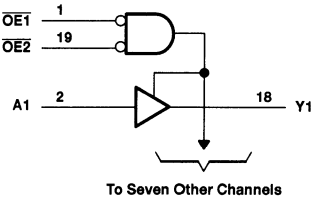
INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DW package ..... 1.6 W
N package ..... 1.3 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HCT541			SN74HCT541			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time		0		500	0		500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT541		SN74HCT541		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	4.5 V	4.4	4.499		4.4		4.4		V
		I_{OH} = –6 mA		3.98	4.3		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
		I_{OL} = 6 mA			0.17	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0,	V_I = V_{IH} or V_{IL}	5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}†	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i			4.5 V to 5.5 V		3	10		10		10	pF

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT541		SN74HCT541		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5 V		13	23		34		29	ns
			5.5 V		12	21		31		26	
t_{en}	$\overline{OE}$	Y	4.5 V		21	30		45		38	ns
			5.5 V		19	27		41		34	
t_{dis}	$\overline{OE}$	Y	4.5 V		19	30		45		38	ns
			5.5 V		18	27		41		34	
t_t		Y	4.5 V		8	12		18		15	ns
			5.5 V		7	11		16		14	

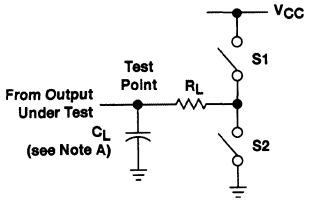
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT541		SN74HCT541		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5 V		20	33		49		42	ns
			5.5 V		19	30		45		38	
t_{en}	$\overline{OE}$	Y	4.5 V		26	40		60		50	ns
			5.5 V		25	36		54		45	
t_t		Y	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

operating characteristics, T_A = 25°C

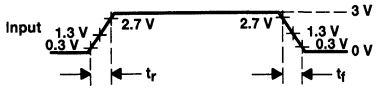
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	No load	35	pF

PARAMETER MEASUREMENT INFORMATION

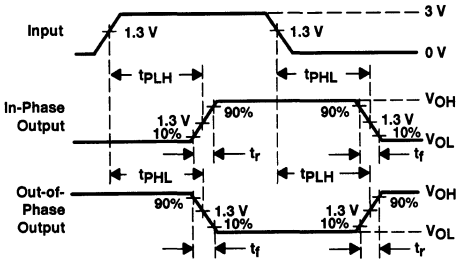


LOAD CIRCUIT

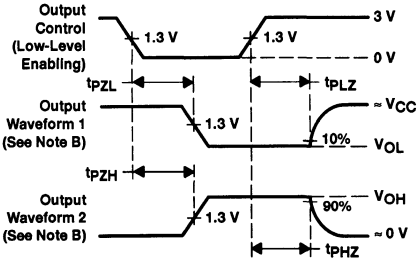
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES



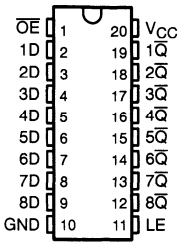
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

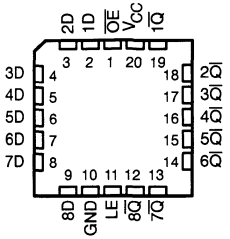
Figure 1. Load Circuit and Voltage Waveforms

- **High-Current 3-State Outputs Drive Bus Lines Directly or up to 15 LSTTL Loads**
- **Bus-Structured Pinout**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC563 . . . J OR W PACKAGE
SN74HC563 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC563 . . . FK PACKAGE
(TOP VIEW)



description

These 8-bit transparent D-type latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the $\overline{Q}$ outputs follow the complements of the data (D) inputs. When LE is taken low, the outputs are latched at the inverses of the levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased high logic level provide the capability to drive bus lines without interface or pullup components.

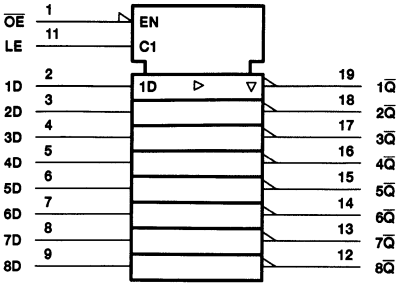
$\overline{OE}$ does not affect internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54HC563 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC563 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each latch)

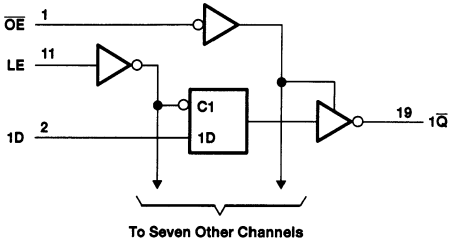
INPUTS			OUTPUT
$\overline{OE}$	LE	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DW package ..... 1.6 W
N package ..... 1.3 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC563			SN74HC563			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC563		SN74HC563		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0		6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC563		SN74HC563		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su}	Setup time, data before LE↓	2 V	50		75		63		ns
		4.5 V	10		15		13		
		6 V	9		13		11		
t_h	Hold time, data after LE↓	2 V	5		5		5		ns
		4.5 V	5		5		5		
		6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC563		SN74HC563		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	$\overline{Q}$	2 V		77	175		265		220	ns
			4.5 V		26	35		53		44	
			6 V		23	30		45		37	
	LE	Any $\overline{Q}$	2 V		90	175		265		220	
			4.5 V		27	35		53		44	
			6 V		23	30		45		37	
t_{en}	$\overline{OE}$	Any $\overline{Q}$	2 V		70	150		225		190	ns
			4.5 V		24	30		45		38	
			6 V		21	26		38		32	
t_{dis}	$\overline{OE}$	Any $\overline{Q}$	2 V		47	150		225		190	ns
			4.5 V		23	30		45		38	
			6 V		21	26		38		32	
t_t		Any $\overline{Q}$	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

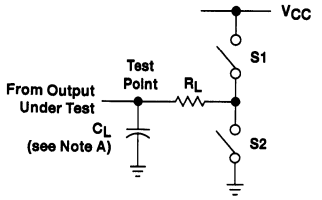
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC563		SN74HC563		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	$\overline{Q}$	2 V		95	200		300		250	ns
			4.5 V		33	40		60		50	
			6 V		29	34		51		43	
	LE	Any $\overline{Q}$	2 V		103	225		335		285	
			4.5 V		33	45		67		57	
			6 V		29	38		57		48	
t_{en}	$\overline{OE}$	Any $\overline{Q}$	2 V		85	200		300		250	ns
			4.5 V		29	40		60		50	
			6 V		26	34		51		43	
t_t		Any $\overline{Q}$	2 V		60	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		14	36		53		45	

operating characteristics, T_A = 25°C

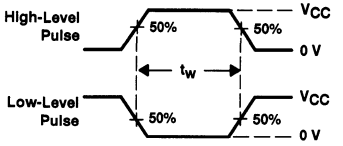
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	No load	50	pF

PARAMETER MEASUREMENT INFORMATION

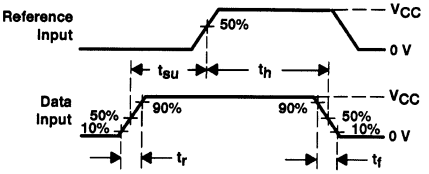


LOAD CIRCUIT

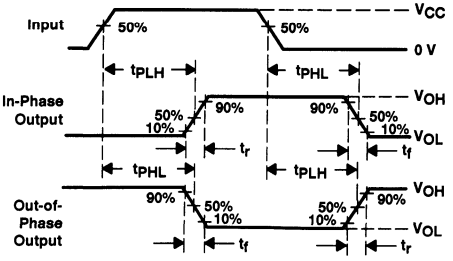
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



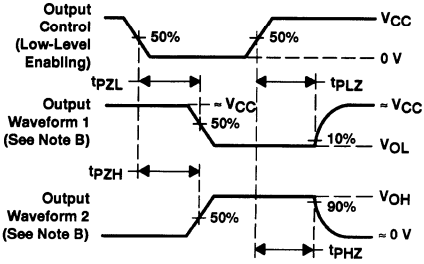
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



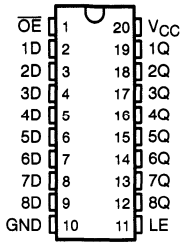
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

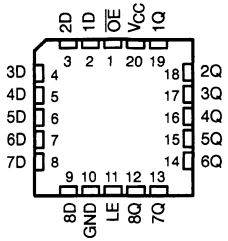
Figure 1. Load Circuit and Voltage Waveforms

- **High-Current 3-State Outputs Drive Bus Lines Directly or up to 15 LSTTL Loads**
- **Bus-Structured Pinout**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC573A . . . J OR W PACKAGE
SN74HC573A . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC573A . . . FK PACKAGE
(TOP VIEW)



description

These octal transparent D-type latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs respond to the data (D) inputs. When LE is low, the outputs are latched to retain the data that was set up.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

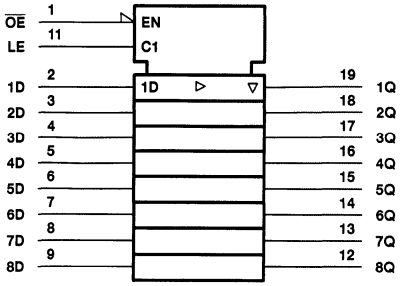
$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54HC573A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC573A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each latch)

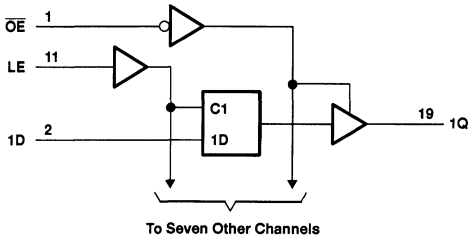
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DW package ..... 1.6 W
N package ..... 1.3 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC573A			SN74HC573A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC573A		SN74HC573A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0		6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC573A		SN74HC573A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su}	Setup time, data before LE↓	2 V	50		75		63		ns
		4.5 V	10		15		13		
		6 V	9		13		11		
t_h	Hold time, data after LE↓	2 V	20		24		24		ns
		4.5 V	5		5		5		
		6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC573A		SN74HC573A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	2 V		77	175		265		220	ns
			4.5 V		26	35		53		44	
			6 V		23	30		45		38	
	LE	Any Q	2 V		87	175		265		220	
			4.5 V		27	35		53		44	
			6 V		23	30		45		38	
t_{en}	$\overline{OE}$	Any Q	2 V		68	150		225		190	ns
			4.5 V		24	30		45		38	
			6 V		21	26		38		32	
t_{dis}	$\overline{OE}$	Any Q	2 V		47	150		225		190	ns
			4.5 V		23	30		45		38	
			6 V		21	26		38		32	
t_t		Any Q	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

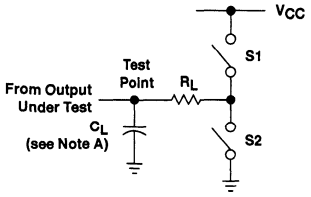
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC573A		SN74HC573A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	2 V		95	200		300		250	ns
			4.5 V		33	40		60		50	
			6 V		21	34		51		43	
	LE	Any Q	2 V		103	225		335		285	
			4.5 V		33	45		67		57	
			6 V		29	38		57		48	
t_{en}	$\overline{OE}$	Any Q	2 V		85	200		300		250	ns
			4.5 V		29	40		60		50	
			6 V		26	34		51		43	
t_t		Any Q	2 V		60	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		14	36		53		45	

operating characteristics, T_A = 25°C

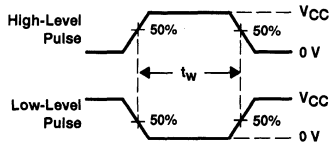
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	No load	50	pF

PARAMETER MEASUREMENT INFORMATION

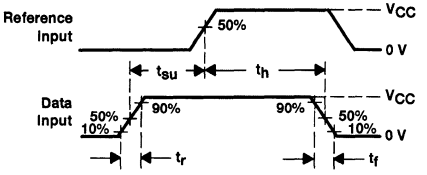


LOAD CIRCUIT

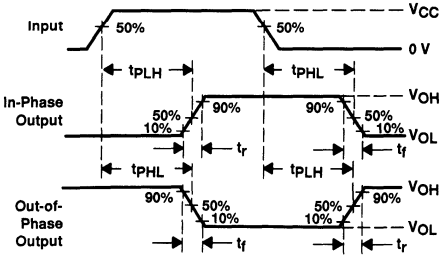
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



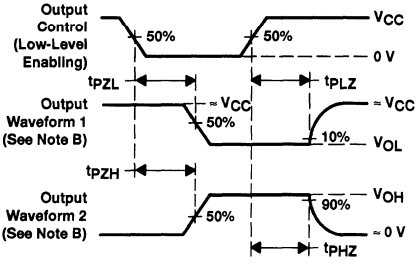
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



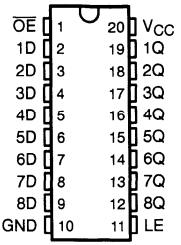
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

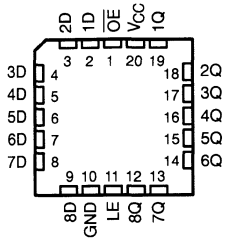
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **High-Current 3-State Outputs Drive Bus Lines Directly or up to 15 LSTTL Loads**
- **Bus-Structured Pinout**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HCT573A . . . J OR W PACKAGE
SN74HCT573A . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT573A . . . FK PACKAGE
(TOP VIEW)



description

These octal transparent D-type latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs respond to the data (D) inputs. When LE is low, the outputs are latched to retain the data that was set up.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

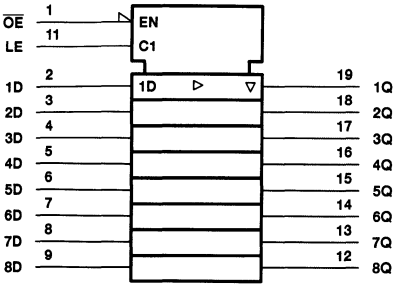
$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54HCT573A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT573A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each latch)

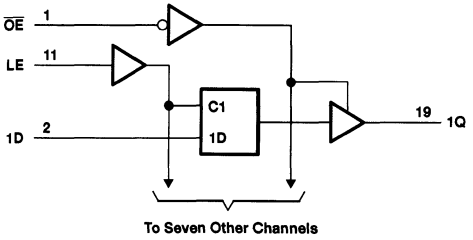
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DW package ..... 1.6 W
N package ..... 1.3 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HCT573A			SN74HCT573A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time		0		500	0		500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT573A		SN74HCT573A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	4.5 V	4.4	4.499		4.4		4.4		V
		I_{OH} = –6 mA		3.98	4.3		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
		I_{OL} = 6 mA			0.17	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0		5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0		5.5 V			8		160		80	μA
ΔI_{CC}†	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i			4.5 V to 5.5 V		3	10		10		10	pF

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HCT573A		SN74HCT573A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	4.5 V	20		30		25		ns
		5.5 V	17		27		23		
t_{su}	Setup time, data before LE↓	4.5 V	10		15		13		ns
		5.5 V	9		14		12		
t_h	Hold time, data after LE↓	4.5 V	5		5		5		ns
		5.5 V	5		5		5		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT573A		SN74HCT573A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	4.5 V		25	35		53		44	ns
			5.5 V		21	32		48		40	
	LE	Any Q	4.5 V		28	35		53		44	
			5.5 V		25	32		48		40	
t_{en}	$\overline{OE}$	Any Q	4.5 V		26	35		53		44	ns
			5.5 V		23	32		48		40	
t_{dis}	$\overline{OE}$	Any Q	4.5 V		23	35		53		44	ns
			5.5 V		22	32		48		40	
t_t		Any Q	4.5 V		9	12		18		15	ns
			5.5 V		9	11		16		14	

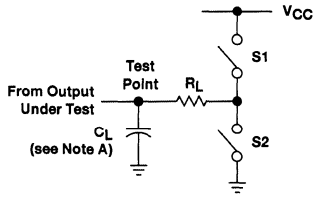
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT573A		SN74HCT573A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	4.5 V		32	52		79		65	ns
			5.5 V		27	47		71		59	
	LE	Any Q	4.5 V		38	52		79		65	
			5.5 V		36	47		71		59	
t_{en}	$\overline{OE}$	Any Q	4.5 V		33	52		79		65	ns
			5.5 V		28	47		71		59	
t_t		Any Q	4.5 V		18	42		63		53	ns
			5.5 V		16	38		57		48	

operating characteristics, T_A = 25°C

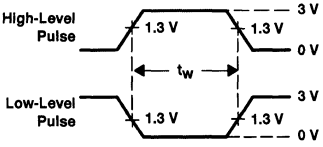
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	No load	50	pF

PARAMETER MEASUREMENT INFORMATION

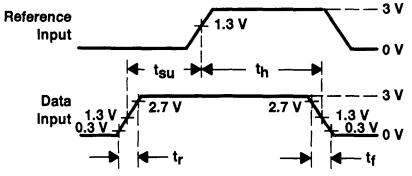


LOAD CIRCUIT

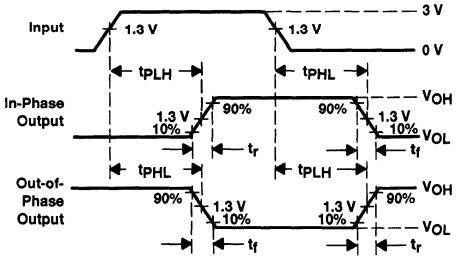
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



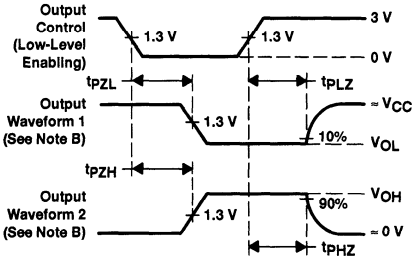
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES



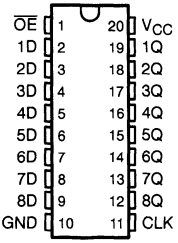
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

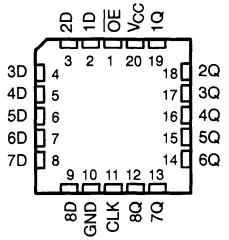
Figure 1. Load Circuit and Voltage Waveforms

- **High-Current 3-State Noninverting Outputs Drive Bus Lines Directly or up to 15 LSTTL Loads**
- **Bus-Structured Pinout**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC574 . . . J OR W PACKAGE
SN74HC574 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC574 . . . FK PACKAGE
(TOP VIEW)



description

These octal edge-triggered D-type flip-flops feature 3-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops enter data on the low-to-high transition of the clock (CLK) input.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

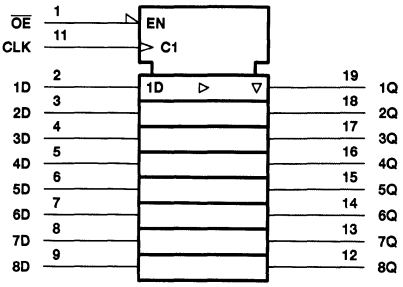
$\overline{OE}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54HC574 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC574 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

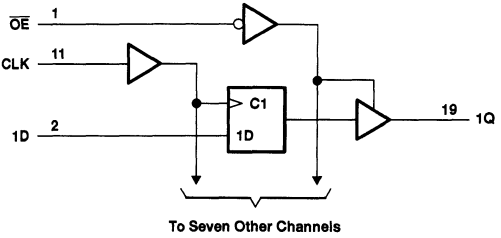
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DW package ..... 1.6 W
N package ..... 1.3 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC574			SN74HC574			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC574		SN74HC574		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0		6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC574		SN74HC574		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	2 V	0	6	0	4	0	5	MHz
		4.5 V	0	30	0	20	0	24	
		6 V	0	38	0	24	0	28	
t_w	Pulse duration, CLK high or low	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su}	Setup time, data before CLK↑	2 V	100		150		125		ns
		4.5 V	20		30		25		
		6 V	17		26		21		
t_h	Hold time, data after CLK↑	2 V	5		5		5		ns
		4.5 V	5		5		5		
		6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC574		SN74HC574		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	11		4		5		MHz
			4.5 V	30	36		20		24		
			6 V	36	40		24		28		
t_{pd}	CLK	Any Q	2 V		90	180		270		225	ns
			4.5 V		28	36		54		45	
			6 V		24	31		46		38	
t_{en}	$\overline{OE}$	Any Q	2 V		77	150		225		190	ns
			4.5 V		26	30		45		38	
			6 V		23	26		38		32	
t_{dis}	$\overline{OE}$	Any Q	2 V		52	150		225		190	ns
			4.5 V		24	30		45		38	
			6 V		22	26		38		32	
t_t		Any Q	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

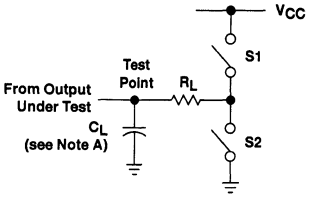
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC574		SN74HC574		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6					5		MHz
			4.5 V	30					24		
			6 V	36					28		
t_{pd}	CLK	Any Q	2 V		105	265		400		330	ns
			4.5 V		36	53		80		66	
			6 V		31	46		68		57	
t_{en}	$\overline{OE}$	Any Q	2 V		95	235		355		295	ns
			4.5 V		32	47		71		59	
			6 V		28	41		60		51	
t_t		Any Q	2 V		60	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		14	36		53		45	

operating characteristics, T_A = 25°C

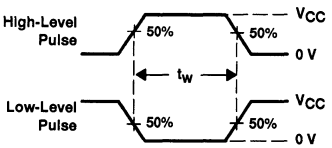
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	No load	100	pF

PARAMETER MEASUREMENT INFORMATION

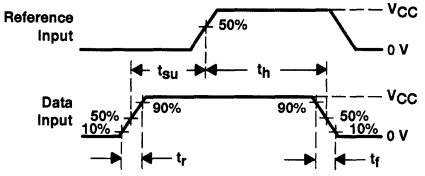


LOAD CIRCUIT

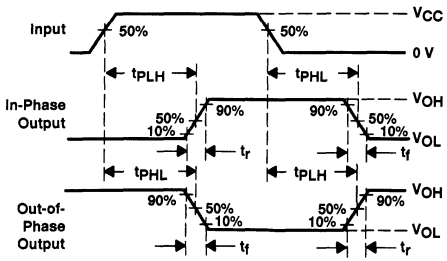
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



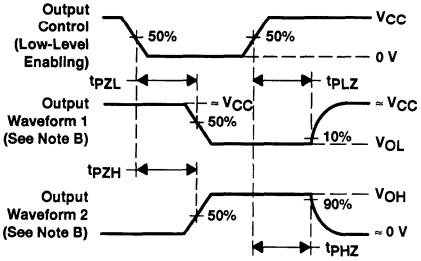
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



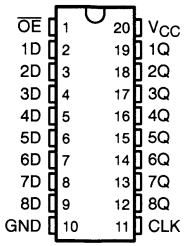
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

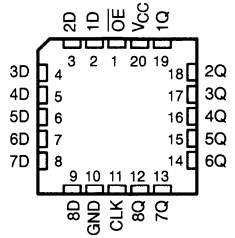
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **High-Current 3-State Noninverting Outputs Drive Bus Lines Directly or up to 15 LSTTL Loads**
- **Bus-Structured Pinout**
- **Package Options Include Plastic Small-Outline (DW), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HCT574 . . . J OR W PACKAGE
SN74HCT574 . . . DW, N, OR PW PACKAGE
(TOP VIEW)



SN54HCT574 . . . FK PACKAGE
(TOP VIEW)



description

These octal edge-triggered D-type flip-flops feature 3-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops enter data on the low-to-high transition of the clock (CLK) input.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

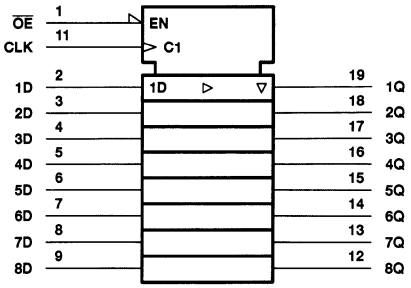
$\overline{OE}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54HCT574 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT574 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

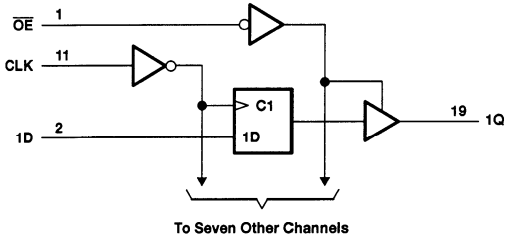
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DW package ..... 1.6 W
N package ..... 1.3 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HCT574			SN74HCT574			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time		0		500	0		500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT574		SN74HCT574		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	4.5 V	4.4	4.499		4.4		4.4		V
		I_{OH} = –6 mA		3.98	4.3		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
		I_{OL} = 6 mA			0.17	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0		5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}†	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i			4.5 V to 5.5 V		3	10		10		10	pF

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HCT574		SN74HCT574		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	4.5 V	0	30	0	20	0	24	MHz
		5.5 V	0	33	0	22	0	27	
t_w	Pulse duration, CLK high or low	4.5 V	16		24		20		ns
		5.5 V	14		22		18		
t_{su}	Setup time, data before CLK↑	4.5 V	20		30		25		ns
		5.5 V	17		27		23		
t_h	Hold time, data after CLK↑	4.5 V	5		5		5		ns
		5.5 V	5		5		5		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT574		SN74HCT574		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			4.5 V	30	36		20		24		MHz
			5.5 V	33	40		22		27		
t_{pd}	CLK	Any Q	4.5 V		30	36		54		45	ns
			5.5 V		25	32		48		41	
t_{en}	$\overline{OE}$	Any Q	4.5 V		26	30		45		38	ns
			5.5 V		23	27		41		34	
t_{dis}	$\overline{OE}$	Any Q	4.5 V		23	30		45		38	ns
			5.5 V		22	27		41		34	
t_t		Any Q	4.5 V		10	12		18		15	ns
			5.5 V		9	11		16		14	

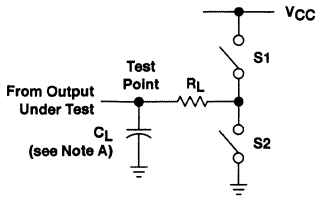
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT574		SN74HCT574		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			4.5 V	30	36		20		24		MHz
			5.5 V	33	40		22		27		
t_{pd}	CLK	Any Q	4.5 V		40	53		80		66	ns
			5.5 V		35	47		71		60	
t_{en}	$\overline{OE}$	Any Q	4.5 V		34	47		71		59	ns
			5.5 V		29	39		94		78	
t_t		Any Q	4.5 V		18	42		63		53	ns
			5.5 V		16	38		57		48	

operating characteristics, T_A = 25°C

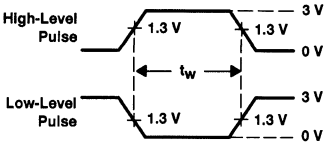
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	No load	93	pF

PARAMETER MEASUREMENT INFORMATION

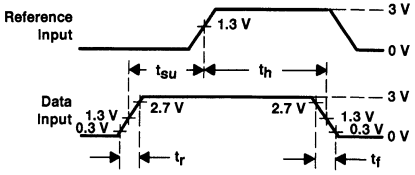


LOAD CIRCUIT

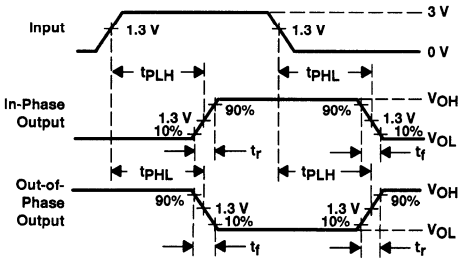
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



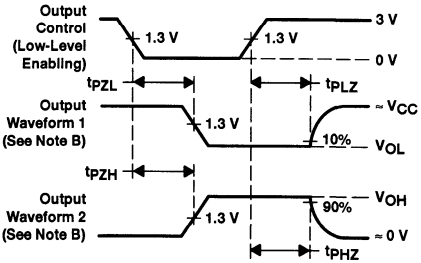
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES



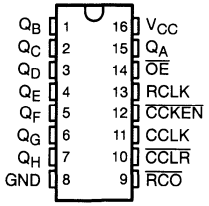
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

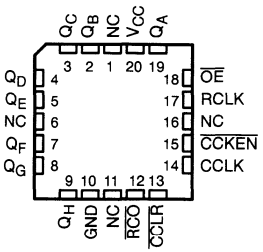
Figure 1. Load Circuit and Voltage Waveforms

- **8-Bit Counter With Register**
- **High-Current 3-State Parallel Register Outputs Can Drive up to 15 LSTTL Loads**
- **Counter Has Direct Clear**
- **Package Options Include Plastic Small-Outline (D, DW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC590A . . . J OR W PACKAGE
SN74HC590A . . . D, DW, OR N PACKAGE
(TOP VIEW)



SN54HC590A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

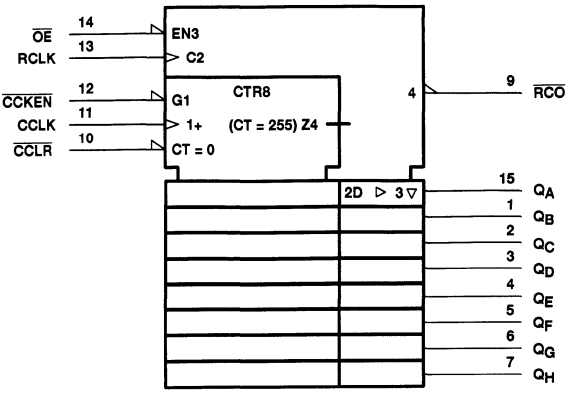
description

The 'HC590A contain an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register. The binary counter features direct clear ($\overline{CCLR}$) and count-enable ($\overline{CCKEN}$) inputs. A ripple-carry ($\overline{RCO}$) output is provided for cascading. Expansion is easily accomplished for two stages by connecting $\overline{RCO}$ of the first stage to $\overline{CCKEN}$ of the second stage. Cascading for larger count chains can be accomplished by connecting $\overline{RCO}$ of each stage to the counter clock (CCLK) input of the following stage.

Both CCLK and the register clock (RCLK) input are positive-edge triggered. If both clocks are connected together, the counter state is always one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

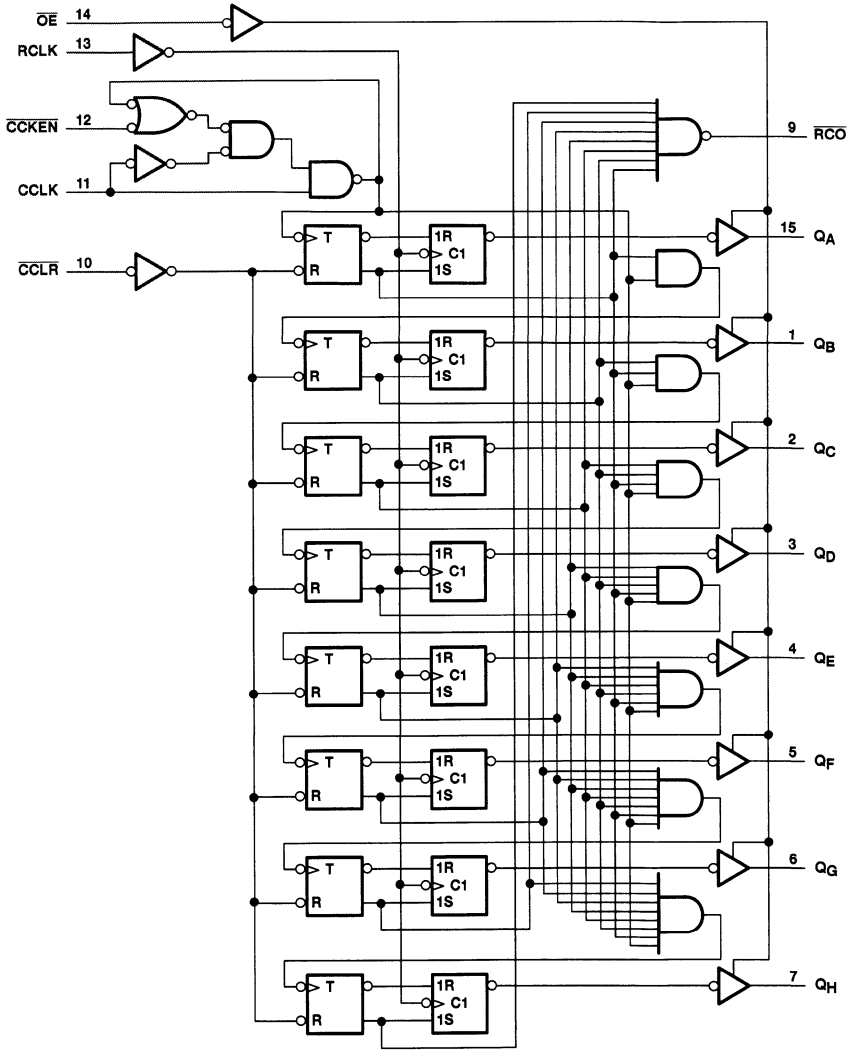
The SN54HC590A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC590A is characterized for operation from –40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DW, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DW, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
DW package ..... 1 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC590A			SN74HC590A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t‡	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

‡ If this device is used in the threshold region (from V_{IL}max = 0.5 V to V_{IH}min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC590A		SN74HC590A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		$\overline{RCO}$, I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		Q_A–Q_H, I_{OH} = –6 mA		3.98	4.3		3.7		3.84		
		$\overline{RCO}$, I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
		Q_A–Q_H, I_{OH} = –7.8 mA		5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		$\overline{RCO}$, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		Q_A–Q_H, I_{OL} = 6 mA			0.17	0.26		0.4		0.33	
		$\overline{RCO}$, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
		Q_A–Q_H, I_{OL} = 7.8 mA			0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V			±0.1		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0		6 V			±0.01		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC590A		SN74HC590A		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	4	0	2.5	0	3.2	MHz
			4.5 V	0	20	0	13		16	
			6 V	0	24	0	16	0	19	
t_w	Pulse duration	CCLK or RCLK high or low	2 V	125		200		155		ns
			4.5 V	25		38		31		
			6 V	21		32		26		
		$\overline{CCLR}$ low	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		26		21		
t_{su}	Setup time	$\overline{CCKEN}$ low before CCLK↑	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		26		21		
		$\overline{CCLR}$ high (inactive) before CCLK↑	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		26		21		
		CCLK↑ before RCLK↑†	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		26		21		
t_h	Hold time	$\overline{CCKEN}$ low after CCLK↑	2 V	50		75		60		ns
			4.5 V	10		15		12		
			6 V	9		13		11		

† This setup time ensures that the register gets stable data from the counter outputs. The clocks may be tied together, in which case the register is one clock pulse behind the counter.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN54HC590A					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			2 V	4	8		2.5		MHz
			4.5 V	20	35		13		
			6 V	24	40		16		
t_{pd}	CCLK↑	$\overline{RCO}$	2 V		80	150		225	ns
			4.5 V		20	31		45	
			6 V		15	26		38	
t_{PLH}	$\overline{CCLR}$↓	$\overline{RCO}$	2 V		70	130		195	ns
			4.5 V		18	28		39	
			6 V		14	23		33	
t_{pd}	RCLK↑	Q	2 V		70	140		210	ns
			4.5 V		18	31		42	
			6 V		14	25		36	
t_{en}	$\overline{OE}$↓	Q	2 V		80	125		185	ns
			4.5 V		20	30		37	
			6 V		15	28		31	
t_{dis}	$\overline{OE}$↑	Q	2 V		80	125		185	ns
			4.5 V		20	30		37	
			6 V		15	28		31	
t_t*		$\overline{RCO}$	2 V		38	75		110	ns
			4.5 V		8	15		22	
			6 V		6	13		19	
		Q	2 V		38	60		90	
			4.5 V		8	12		18	
			6 V		6	10		15	

* This parameter is not production tested for the SN54HC590A.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN74HC590A					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			2 V	4	8		3.2		MHz
			4.5 V	20	35		16		
			6 V	24	40		19		
t_{pd}	CCLK↑	$\overline{RCO}$	2 V		80	150		190	ns
			4.5 V		20	30		38	
			6 V		15	26		33	
t_{PLH}	$\overline{CCLR}$↓	$\overline{RCO}$	2 V		70	130		165	ns
			4.5 V		18	26		33	
			6 V		14	22		28	
t_{pd}	RCLK↑	Q	2 V		70	140		175	ns
			4.5 V		18	28		35	
			6 V		14	24		30	
t_{en}	$\overline{OE}$↓	Q	2 V		80	125		155	ns
			4.5 V		20	25		31	
			6 V		15	21		26	
t_{dis}	$\overline{OE}$↑	Q	2 V		80	125		155	ns
			4.5 V		20	25		31	
			6 V		15	21		26	
t_t		$\overline{RCO}$	2 V		38	75		95	ns
			4.5 V		8	15		19	
			6 V		6	13		16	
		Q	2 V		38	60		75	
			4.5 V		8	12		15	
			6 V		6	10		13	

switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN54HC590A					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{pd}	RCLK↑	Q	2 V		100	300		447	ns
			4.5 V		24	60		90	
			6 V		20	51		77	
t_{en}	$\overline{OE}$	Q	2 V		90	200		300	ns
			4.5 V		23	40		60	
			6 V		19	34		51	
t_t*		Q	2 V		45	210		315	ns
			4.5 V		17	42		63	
			6 V		13	36		53	

* This parameter is not production tested for the SN54HC590A.

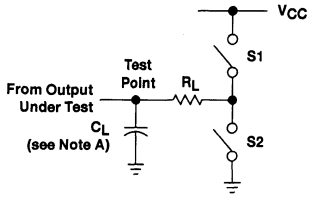
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN74HC590A					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{pd}	RCLK↑	Q	2 V		100	300		380	ns
			4.5 V		24	60		76	
			6 V		20	51		65	
t_{en}	$\overline{OE}$	Q	2 V		90	200		250	ns
			4.5 V		23	40		50	
			6 V		19	34		43	
t_t		Q	2 V		45	210		265	ns
			4.5 V		17	42		53	
			6 V		13	36		45	

operating characteristics, T_A = 25°C

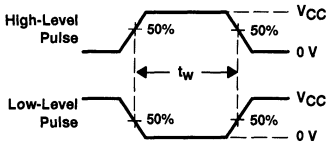
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	250	pF

PARAMETER MEASUREMENT INFORMATION

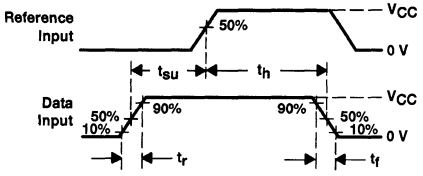


LOAD CIRCUIT

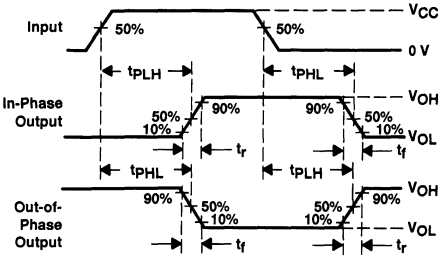
PARAMETER		RL	CL	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



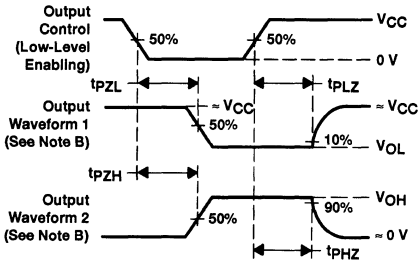
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



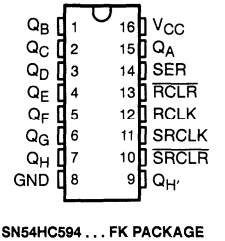
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

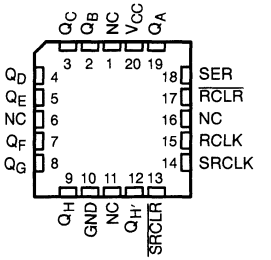
Figure 1. Load Circuit and Voltage Waveforms

- **8-Bit Serial-In, Parallel-Out Shift Registers With Storage**
- **Independent Direct Overriding Clears on Shift and Storage Registers**
- **Independent Clocks for Both Shift and Storage Registers**
- **High-Current Outputs Can Drive up to 15 LSTTL Loads**
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC594 . . . J OR W PACKAGE
SN74HC594 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC594 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

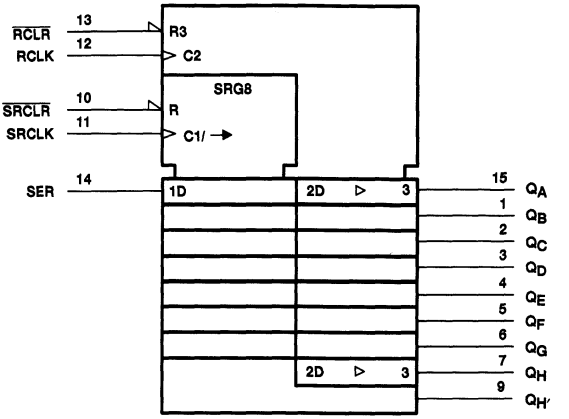
The 'HC594 contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clear ($\overline{RCLR}$, $\overline{SRCLR}$) inputs are provided on both the shift and storage registers. A serial ($Q_{H'}$) output is provided for cascading purposes.

Both the shift register (RCLK) and storage register (SRCLK) clocks are positive edge triggered. If both clocks are connected together, the shift register is always one count pulse ahead of the storage register.

The parallel (Q_A–Q_H) outputs have high-current capability. $Q_{H'}$ is a standard output.

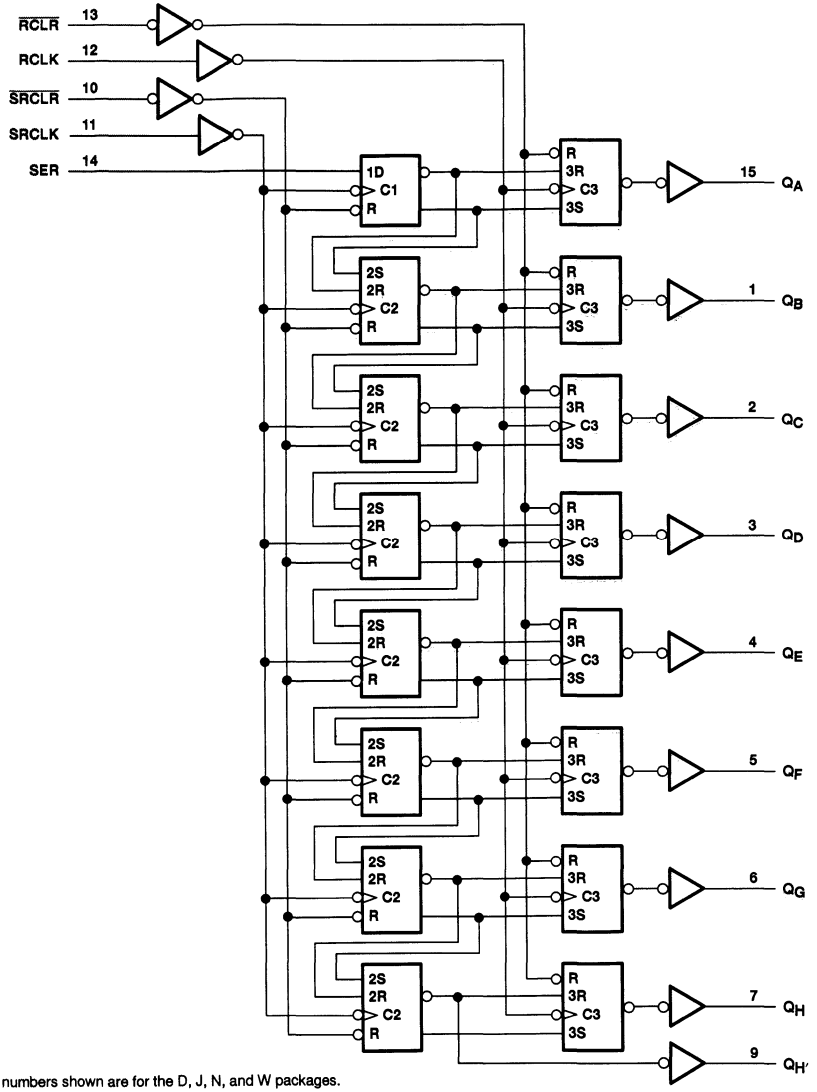
The SN54HC594 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC594 is characterized for operation from –40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC594			SN74HC594			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC594		SN74HC594		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		$Q_{H'}$, I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		Q_A–Q_H, I_{OH} = –6 mA		3.98	4.3		3.7		3.84		
		$Q_{H'}$, I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
		Q_A–Q_H, I_{OH} = –7.8 mA		5.48	5.8		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		$Q_{H'}$, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		Q_A–Q_H, I_{OL} = 6 mA			0.17	0.26		0.4		0.33	
		$Q_{H'}$, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
		Q_A–Q_H, I_{OL} = 7.8 mA			0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	$V_O = V_{CC}$ or 0		6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0		6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC594		SN74HC594		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	5	0	3.3	0	4	MHz
			4.5 V	0	25	0	17	0	20	
			6 V	0	29	0	20	0	24	
t_w	Pulse duration	SRCLK or RCLK high or low	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		$\overline{SRCLR}$ or $\overline{RCLR}$ low	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		25		21		
t_{su}	Setup time	SER before SRCLK↑	2 V	90		135		110		ns
			4.5 V	18		27		22		
			6 V	15		23		19		
		SRCLK↑ before RCLK↑†	2 V	90		135		110		
			4.5 V	18		27		22		
			6 V	15		23		19		
		$\overline{SRCLR}$ low before RCLK↑	2 V	50		75		63		
			4.5 V	10		15		13		
			6 V	9		13		11		
		$\overline{SRCLR}$ high (inactive) before SRCLK↑	2 V	20		20		20		
			4.5 V	10		10		10		
			6 V	10		10		10		
		$\overline{RCLR}$ high (inactive) before SRCLK↑	2 V	5		5		5		
			4.5 V	5		5		5		
			6 V	5		5		5		
t_h	Hold time, SER after SRCLK↑		2 V	5		5		5		ns
			4.5 V	5		5		5		
			6 V	5		5		5		

† This setup time ensures the output register sees stable data from the shift-register outputs. The clocks may be tied together, in which case the output register is one clock pulse behind the shift register.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC594		SN74HC594		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	5	8		3.3		4		MHz
			4.5 V	25	35		17		20		
			6 V	29	40		20		24		
t_{pd}	SRCLK	$Q_{H'}$	2 V		50	150		225		185	ns
			4.5 V		20	30		45		37	
			6 V		15	25		38		31	
	RCLK	Q_A–Q_H	2 V		50	150		225		185	
			4.5 V		20	30		45		37	
			6 V		15	25		38		31	
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	2 V		50	150		225		185	ns
			4.5 V		20	30		45		37	
			6 V		15	25		38		31	
	$\overline{RCLR}$	Q_A–Q_H	2 V		50	125		185		155	
			4.5 V		20	25		37		31	
			6 V		15	21		31		26	
t_t		$Q_{H'}$	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	
		Q_A–Q_H	2 V		38	60		90		75	
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

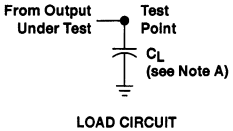
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC594		SN74HC594		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	RCLK	Q_A–Q_H	2 V		90	200		300		250	ns
			4.5 V		23	40		60		50	
			6 V		19	34		51		43	
t_{PHL}	$\overline{RCLR}$	Q_A–Q_H	2 V		90	200		300		250	ns
			4.5 V		23	40		60		50	
			6 V		19	34		51		43	
t_t		Q_A–Q_H	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

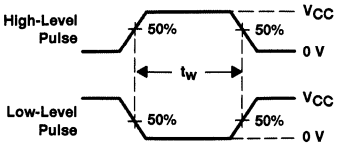
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	395	pF

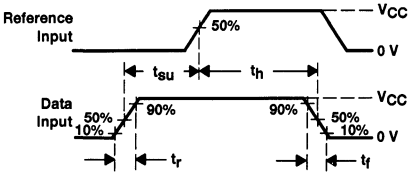
PARAMETER MEASUREMENT INFORMATION



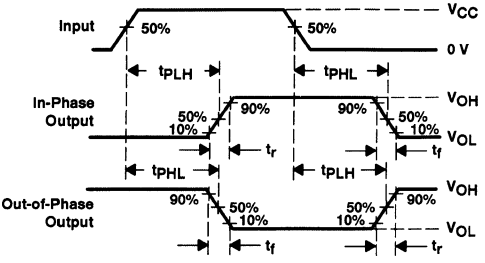
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



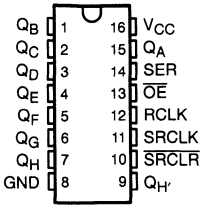
VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

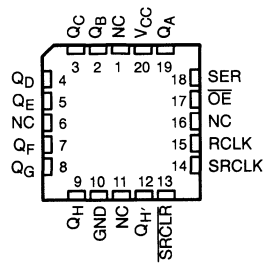
Figure 1. Load Circuit and Voltage Waveforms

- **8-Bit Serial-In, Parallel-Out Shift**
- **High-Current 3-State Outputs Can Drive up to 15 LSTTL Loads**
- **Shift Register Has Direct Clear**
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC595 . . . J OR W PACKAGE
SN74HC595 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC595 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

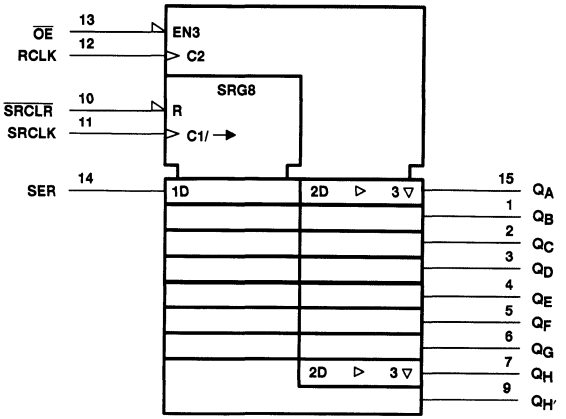
description

The 'HC595 contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear ($\overline{SRCLR}$) input, serial (SER) input, and serial outputs for cascading.

Both the shift register (RCLK) and storage register (SRCLK) clocks are positive-edge triggered. If both clocks are connected together, the shift register is always one clock pulse ahead of the storage register.

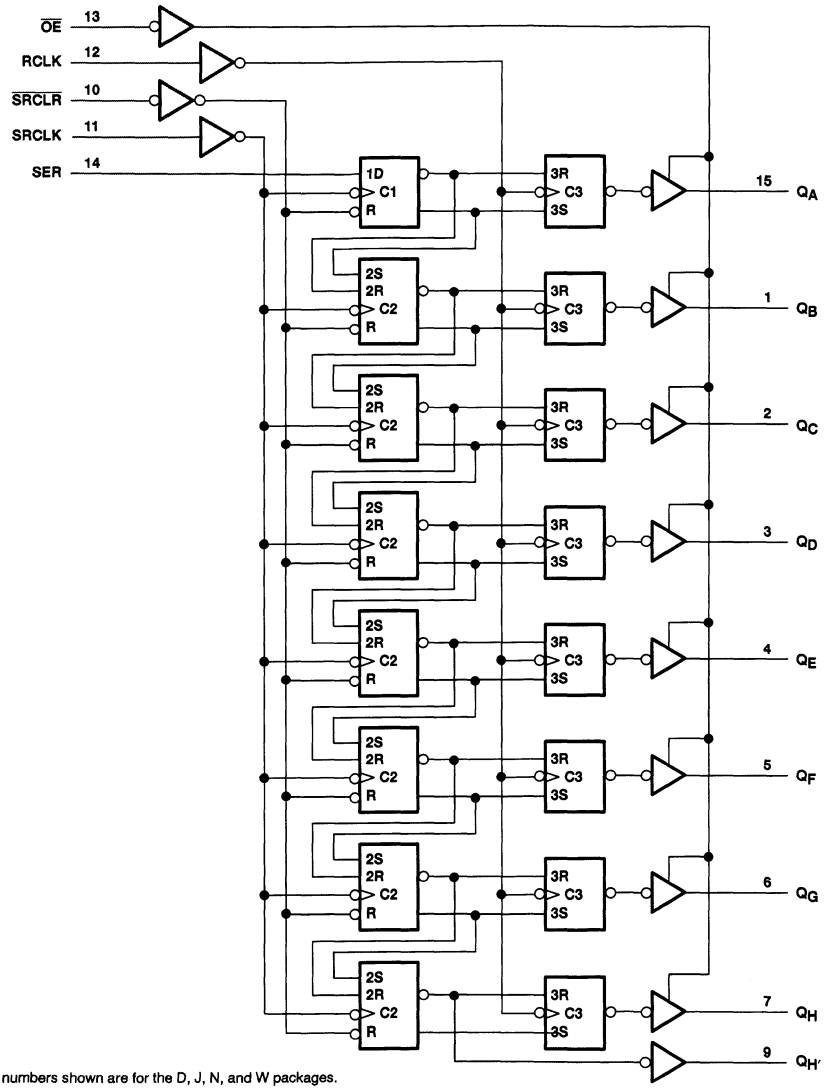
The SN54HC595 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC595 is characterized for operation from –40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC595			SN74HC595			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t‡	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

‡ If this device is used in the threshold region (from V_{IL}max = 0.5 V to V_{IH}min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC595		SN74HC595		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		$Q_{H'}$, I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		Q_A–Q_H, I_{OH} = –6 mA		3.98	4.3		3.7		3.84		
		$Q_{H'}$, I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
		Q_A–Q_H, I_{OH} = –7.8 mA		5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		$Q_{H'}$, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		Q_A–Q_H, I_{OL} = 6 mA			0.17	0.26		0.4		0.33	
		$Q_{H'}$, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
		Q_A–Q_H, I_{OL} = 7.8 mA			0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0		6 V		±0.01	±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC595		SN74HC595		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	29	
t_w	Pulse duration	SRCLK or RCLK high or low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
		$\overline{SRCLR}$ low	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time	SER before SRCLK↑	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		SRCLK↑ before RCLK↑†	2 V	75		113		94		
			4.5 V	15		23		19		
			6 V	13		19		16		
		$\overline{SRCLR}$ low before RCLK↑	2 V	50		75		65		
			4.5 V	10		15		13		
			6 V	9		13		11		
		$\overline{SRCLR}$ high (inactive) before SRCLK↑	2 V	50		75		60		
			4.5 V	10		15		12		
			6 V	9		13		11		
t_h	Hold time, SER after SRCLK↑		2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		

† This setup time ensures the output register sees stable data from the shift-register outputs. The clocks may be tied together, in which case the output register is one clock pulse behind the shift register.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC595		SN74HC595		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	26		4.2		5		MHz
			4.5 V	31	38		21		25		
			6 V	36	42		25		29		
t_{pd}	SRCLK	$Q_{H'}$	2 V		50	160		240		200	ns
			4.5 V		17	32		48		40	
			6 V		14	27		41		34	
	RCLK	Q_A–Q_H	2 V		50	150		225		187	
			4.5 V		17	30		45		37	
			6 V		14	26		38		32	
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	2 V		51	175		261		219	ns
			4.5 V		18	35		52		44	
			6 V		15	30		44		37	
t_{en}	$\overline{OE}$	Q_A–Q_H	2 V		40	150		225		187	ns
			4.5 V		15	30		45		37	
			6 V		13	26		38		32	
t_{dis}	$\overline{OE}$	Q_A–Q_H	2 V		42	200		300		250	ns
			4.5 V		23	40		60		50	
			6 V		20	34		51		43	
t_t		Q_A–Q_H	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	
		$Q_{H'}$	2 V		28	75		110		95	
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

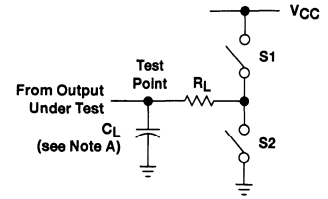
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC595		SN74HC595		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	RCLK	Q_A–Q_H	2 V		60	200		300		250	ns
			4.5 V		22	40		60		50	
			6 V		19	34		51		43	
t_{en}	$\overline{OE}$	Q_A–Q_H	2 V		70	200		298		250	ns
			4.5 V		23	40		60		50	
			6 V		19	34		51		43	
t_t		Q_A–Q_H	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

operating characteristics, T_A = 25°C

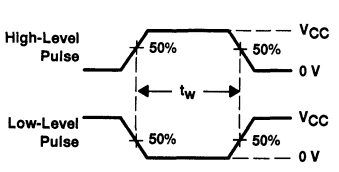
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	400	pF

PARAMETER MEASUREMENT INFORMATION

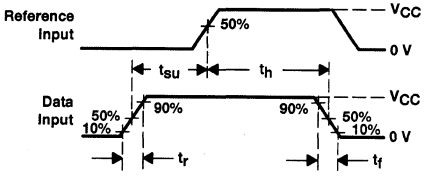


LOAD CIRCUIT

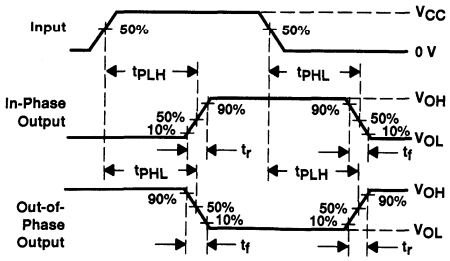
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



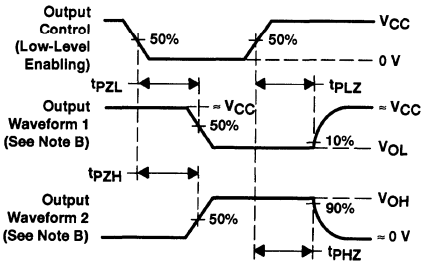
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



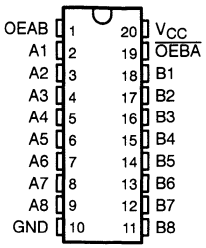
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

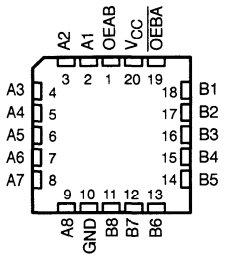
Figure 1. Load Circuit and Voltage Waveforms

- **Lock Bus-Latch Capability**
- **True Logic**
- **High-Current 3-State Outputs Can Drive up to 15 LSTTL Loads**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC623 . . . J OR W PACKAGE
SN74HC623 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC623 . . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation allows for maximum flexibility in timing.

The 'HC623 allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the output-enable (OEAB and $\overline{\text{OEBA}}$) inputs.

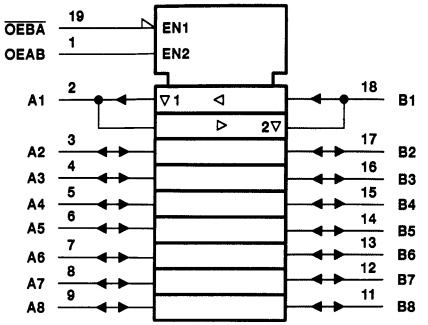
OEAB and $\overline{\text{OEBA}}$ disable the device so that the buses are effectively isolated. The dual-enable configuration gives the transceivers the capability to store data by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. Each output reinforces its input in this transceiver configuration. When both OEAB and $\overline{\text{OEBA}}$ are enabled and all other data sources to the two sets of bus lines are in the high-impedance state, both sets of bus lines (16 total) remain at their last states. The 8-bit codes appearing on the two sets of buses are identical.

The SN54HC623 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC623 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

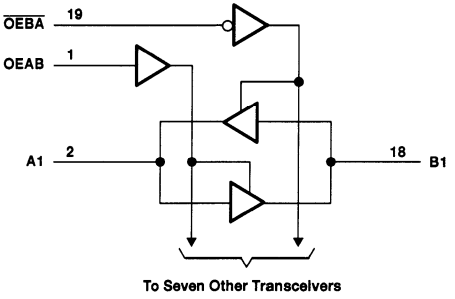
INPUTS		OPERATION
$\overline{\text{OEBA}}$	OEAB	
L	L	B data to A bus
H	H	A data to B bus
H	L	Isolation
L	H	B data to A bus, A data to B bus

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DW package ..... 1.6 W
N package ..... 1.3 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC623			SN74HC623			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC623		SN74HC623		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
				4.5 V	4.4	4.499		4.4		4.4		
				6 V	5.9	5.999		5.9		5.9		
			I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
			I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}		V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
				4.5 V		0.001	0.1		0.1		0.1	
				6 V		0.001	0.1		0.1		0.1	
			I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
			I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	OEAB or $\overline{OEBA}$	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	A or B	V_O = V_{CC} or 0		6 V		±0.01	±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i	OEAB or $\overline{OEBA}$			2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC623		SN74HC623		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		29	105		160		130	ns
			4.5 V		10	21		32		26	
			6 V		8	18		27		22	
t_{en}	$\overline{OEBA}$	A	2 V		112	210		315		265	ns
			4.5 V		27	42		63		53	
			6 V		20	36		54		45	
t_{dis}	$\overline{OEBA}$	A	2 V		40	150		225		190	ns
			4.5 V		18	30		45		38	
			6 V		16	26		38		32	
t_{en}	OEAB	B	2 V		112	210		315		265	ns
			4.5 V		27	42		63		53	
			6 V		20	36		54		45	
t_{dis}	OEAB	B	2 V		40	150		225		190	ns
			4.5 V		18	30		45		38	
			6 V		16	26		38		32	
t_t		A or B	2 V		20	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

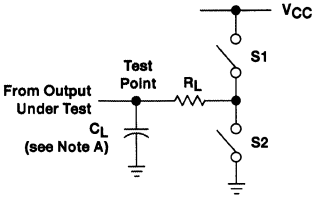
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC623		SN74HC623		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		44	135		200		170	ns
			4.5 V		14	27		40		34	
			6 V		11	23		34		29	
t_{en}	$\overline{OEBA}$	A	2 V		130	270		405		335	ns
			4.5 V		31	54		81		67	
			6 V		23	46		69		56	
	OEAB	B	2 V		130	270		405		335	ns
			4.5 V		31	54		81		67	
			6 V		23	46		69		56	
t_t		A or B	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

operating characteristics, T_A = 25°C

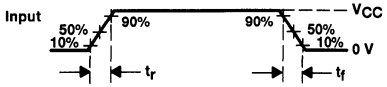
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	No load	40	pF

PARAMETER MEASUREMENT INFORMATION

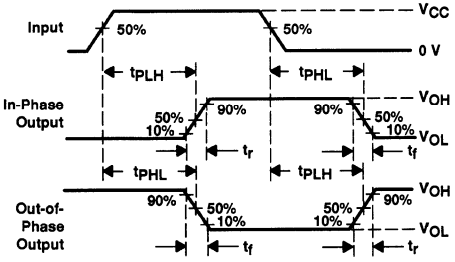


LOAD CIRCUIT

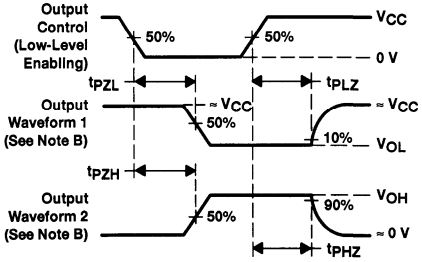
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



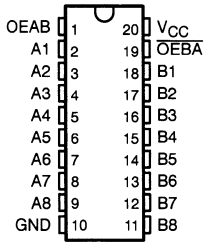
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

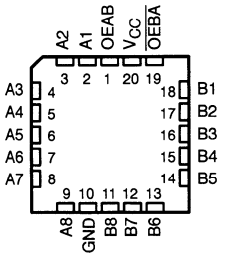
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Lock Bus-Latch Capability**
- **True Logic**
- **High-Current 3-State Outputs Can Drive up to 15 LSTTL Loads**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HCT623 . . . J OR W PACKAGE
SN74HCT623 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT623 . . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation allows for maximum flexibility in timing.

The 'HCT623 allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the output-enable (OEAB and $\overline{\text{OEBA}}$) inputs.

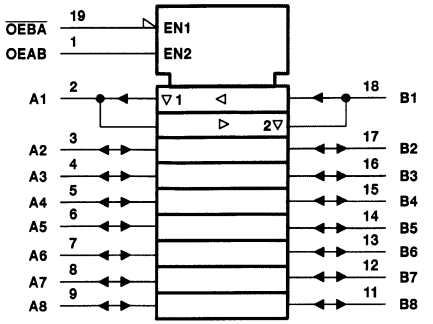
The output-enable inputs disable the device so that the buses are effectively isolated. The dual-enable configuration gives the transceivers the capability to store data by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. Each output reinforces its input in this transceiver configuration. When both OEAB and $\overline{\text{OEBA}}$ are enabled and all other data sources to the two sets of bus lines are in the high-impedance state, both sets of bus lines (16 total) remain at their last states. The 8-bit codes appearing on the two sets of buses are identical.

The SN54HCT623 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT623 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

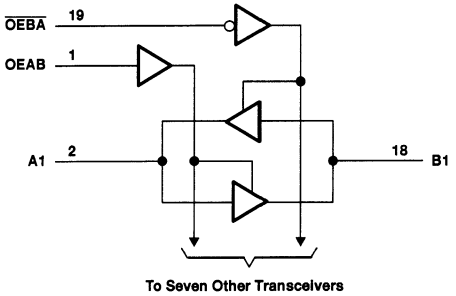
INPUTS		OPERATION
$\overline{\text{OEBA}}$	OEAB	
L	L	B data to A bus
H	H	A data to B bus
H	L	Isolation
L	H	B data to A bus, A data to B bus

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DW package ..... 1.6 W
N package ..... 1.3 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HCT623			SN74HCT623			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time		0		500	0		500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT623		SN74HCT623		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	4.5 V	4.4	4.499		4.4		4.4		V
			I_{OH} = –6 mA		3.98	4.3		3.7		3.84		
V_{OL}		V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
			I_{OL} = 6 mA			0.17	0.26		0.4		0.33	
I_I	OEAB or $\overline{OEBA}$	V_I = V_{CC} or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	A or B	V_O = V_{CC} or GND		5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or 0,	I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}†		One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i	OEAB or $\overline{OEBA}$			4.5 V to 5.5 V		3	10		10		10	pF

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT623		SN74HCT623		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		15	22		33		28	ns
			5.5 V		13	20		30		25	
t_{en}	$\overline{OEBA}$	A	4.5 V		30	42		63		53	ns
			5.5 V		23	38		57		48	
t_{dis}	$\overline{OEBA}$	A	4.5 V		18	30		45		38	ns
			5.5 V		16	28		42		35	
t_{en}	OEAB	B	4.5 V		30	42		63		53	ns
			5.5 V		23	38		57		48	
t_{dis}	OEAB	B	4.5 V		18	30		45		38	ns
			5.5 V		16	28		42		35	
t_t		A or B	4.5 V		9	12		18		15	ns
			5.5 V		8	11		16		14	

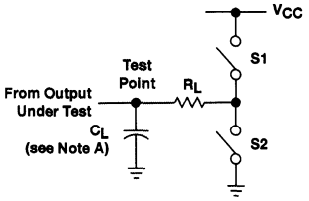
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT623		SN74HCT623		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		18	38		58		47	ns
			5.5 V		11	34		52		42	
t_{en}	$\overline{OEBA}$	A	4.5 V		36	59		89		74	ns
			5.5 V		30	53		80		67	
	OEAB	B	4.5 V		36	59		89		74	
			5.5 V		30	53		80		67	
t_t		A or B	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

operating characteristics, T_A = 25°C

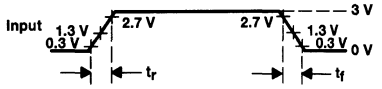
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	No load	40	pF

PARAMETER MEASUREMENT INFORMATION

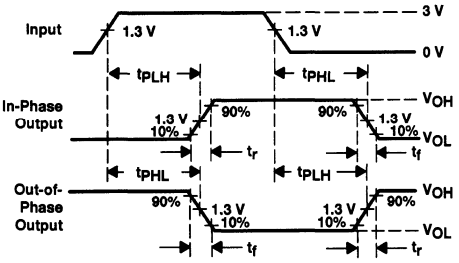


LOAD CIRCUIT

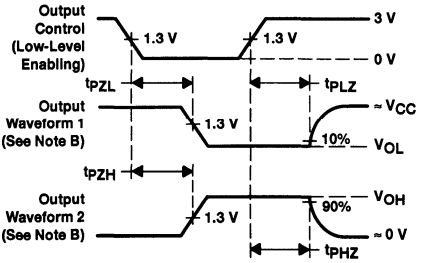
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Inverting Logic**
- **High-Current 3-State Outputs Can Drive up to 15 LSTTL Loads**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

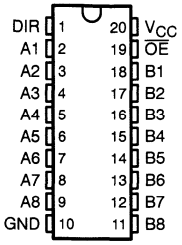
These octal bus transceivers are designed for asynchronous two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

The SN54HC640 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC640 is characterized for operation from –40°C to 85°C.

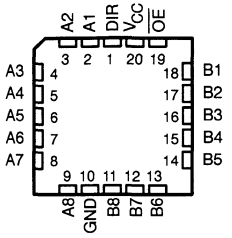
FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus
H	X	Isolation

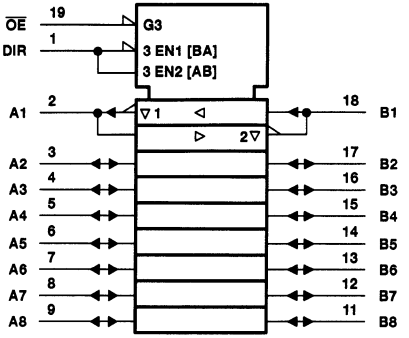
SN54HC640 . . . J OR W PACKAGE
SN74HC640 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC640 . . . FK PACKAGE
(TOP VIEW)

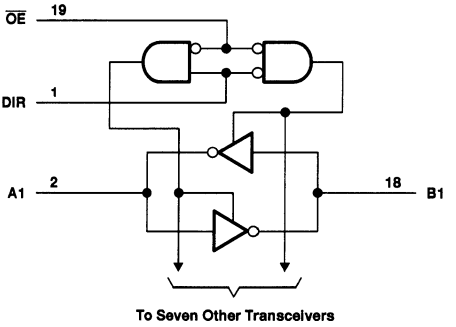


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DW package ..... 1.6 W
N package ..... 1.3 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC640			SN74HC640			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC640		SN74HC640		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
				4.5 V	4.4	4.499		4.4		4.4		
				6 V	5.9	5.999		5.9		5.9		
			I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
			I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}		$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
				4.5 V		0.001	0.1		0.1		0.1	
				6 V		0.001	0.1		0.1		0.1	
			I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
			I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	DIR or $\overline{OE}$	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	A or B	$V_O = V_{CC}$ or 0		6 V		±0.01	±0.5		±10		±5	μA
I_{CC}		$V_I = V_{CC}$ or 0,	I_O = 0	6 V			8		160		80	μA
C_i	DIR or $\overline{OE}$			2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC640		SN74HC640		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		29	105		160		130	ns
			4.5 V		10	21		32		26	
			6 V		8	18		27		22	
t_{en}	$\overline{OE}$	A or B	2 V		109	230		340		290	ns
			4.5 V		27	46		68		58	
			6 V		20	39		58		49	
t_{dis}	$\overline{OE}$	A or B	2 V		40	150		225		190	ns
			4.5 V		18	30		45		38	
			6 V		16	26		38		32	
t_t		A or B	2 V		20	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

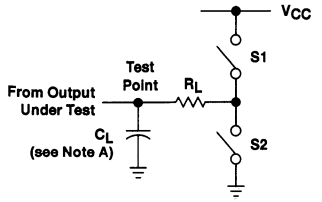
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC640		SN74HC640		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		44	190		290		235	ns
			4.5 V		14	38		58		47	
			6 V		11	33		49		41	
t_{en}	$\overline{OE}$	A or B	2 V		124	315		470		395	ns
			4.5 V		31	63		94		79	
			6 V		23	54		80		68	
t_t		A or B	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

operating characteristics, T_A = 25°C

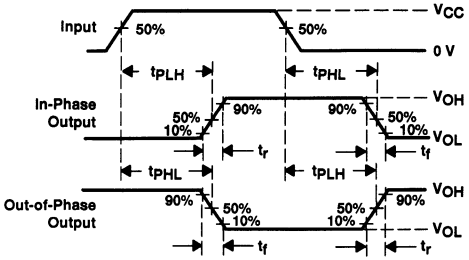
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	No load	40	pF

PARAMETER MEASUREMENT INFORMATION

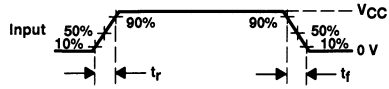


LOAD CIRCUIT

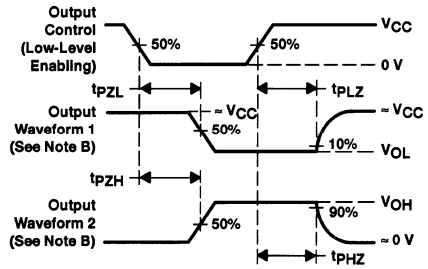
PARAMETER		RL	CL	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **True Logic**
- **High-Current 3-State Outputs Can Drive up to 15 LSTTL Loads**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

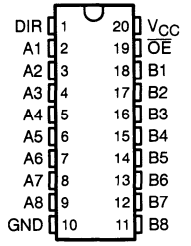
These octal bus transceivers are designed for asynchronous two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

The SN54HC645 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC645 is characterized for operation from –40°C to 85°C.

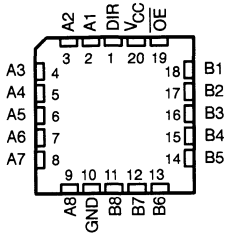
FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

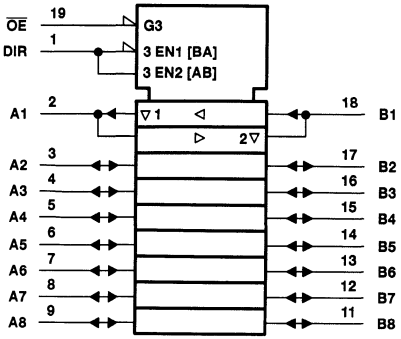
SN54HC645 . . . J OR W PACKAGE
SN74HC645 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC645 . . . FK PACKAGE
(TOP VIEW)

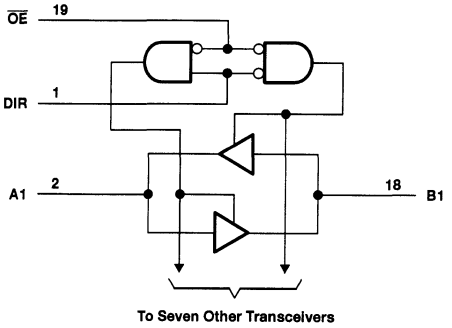


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DW package ..... 1.6 W
N package ..... 1.3 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC645			SN74HC645			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC645		SN74HC645		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
				4.5 V	4.4	4.499		4.4		4.4		
				6 V	5.9	5.999		5.9		5.9		
			I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
			I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}		$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
				4.5 V		0.001	0.1		0.1		0.1	
				6 V		0.001	0.1		0.1		0.1	
			I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
			I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	DIR or $\overline{OE}$	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	A or B	$V_O = V_{CC}$ or 0		6 V		±0.01	±0.5		±10		±5	μA
I_{CC}		$V_I = V_{CC}$ or 0,	I_O = 0	6 V			8		160		80	μA
C_i	DIR or $\overline{OE}$			2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC645		SN74HC645		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		40	105		160		130	ns
			4.5 V		15	21		32		26	
			6 V		12	18		27		22	
t_{en}	$\overline{OE}$	A or B	2 V		125	230		340		290	ns
			4.5 V		23	46		68		58	
			6 V		20	39		58		49	
t_{dis}	$\overline{OE}$	A or B	2 V		74	200		300		250	ns
			4.5 V		25	40		60		50	
			6 V		21	34		51		43	
t_t		A or B	2 V		20	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

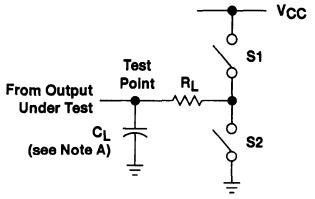
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC645		SN74HC645		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	2 V		54	135		200		170	ns
			4.5 V		18	27		40		34	
			6 V		15	23		34		29	
t_{en}	$\overline{OE}$	A or B	2 V		150	270		405		335	ns
			4.5 V		31	54		81		67	
			6 V		25	46		69		56	
t_t		A or B	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

operating characteristics, T_A = 25°C

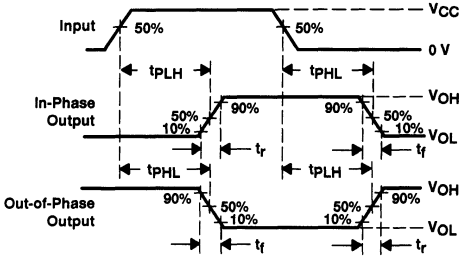
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	No load	40	pF

PARAMETER MEASUREMENT INFORMATION

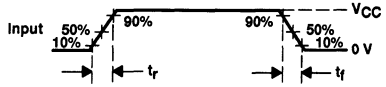


LOAD CIRCUIT

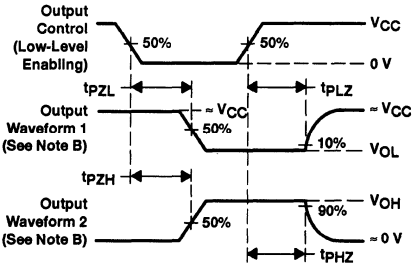
PARAMETER		RL	CL	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



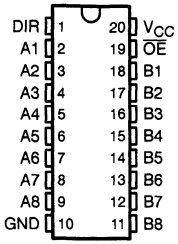
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

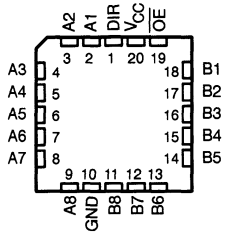
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **True Logic**
- **High-Current 3-State Outputs Can Drive up to 15 LSTTL Loads**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HCT645 . . . J OR W PACKAGE
SN74HCT645 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT645 . . . FK PACKAGE
(TOP VIEW)



description

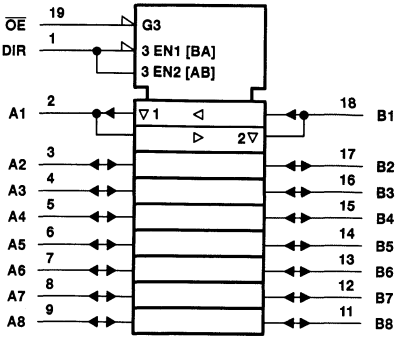
These octal bus transceivers are designed for asynchronous two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

The SN54HCT645 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT645 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

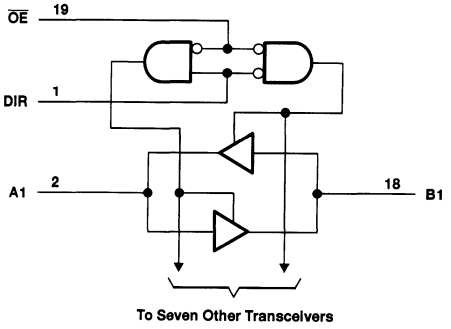
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DW package ..... 1.6 W
N package ..... 1.3 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HCT645			SN74HCT645			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time		0		500	0		500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT645		SN74HCT645		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	4.5 V	4.4	4.499		4.4		4.4		V
			I_{OH} = –6 mA		3.98	4.3		3.7		3.84		
V_{OL}		V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
			I_{OL} = 6 mA			0.17	0.26		0.4		0.33	
I_I	DIR or $\overline{OE}$	V_I = V_{CC} or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	A or B	V_O = V_{CC} or 0		5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or 0,	I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡		One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i	DIR or $\overline{OE}$			4.5 V to 5.5 V		3	10		10		10	pF

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT645		SN74HCT645		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		16	22		33		28	ns
			5.5 V		14	20		30		25	
t_{en}	$\overline{OE}$	A or B	4.5 V		25	46		69		58	ns
			5.5 V		22	41		62		52	
t_{dis}	$\overline{OE}$	A or B	4.5 V		26	40		60		50	ns
			5.5 V		23	36		54		45	
t_t		A or B	4.5 V		9	12		18		15	ns
			5.5 V		8	11		16		14	

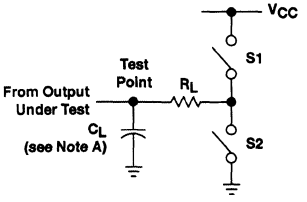
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT645		SN74HCT645		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		20	30		45		38	ns
			5.5 V		18	27		41		34	
t_{en}	$\overline{OE}$	A or B	4.5 V		36	59		89		74	ns
			5.5 V		30	53		80		67	
t_t		A or B	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

operating characteristics, T_A = 25°C

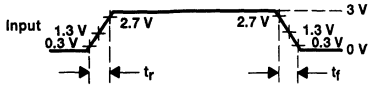
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	No load	40	pF

PARAMETER MEASUREMENT INFORMATION

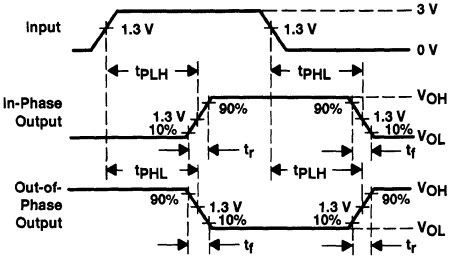


LOAD CIRCUIT

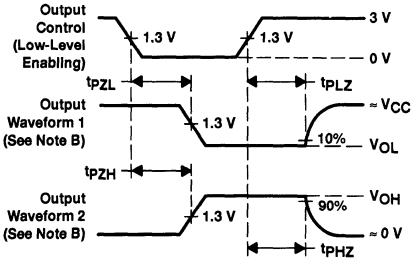
PARAMETER		RL	CL	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES



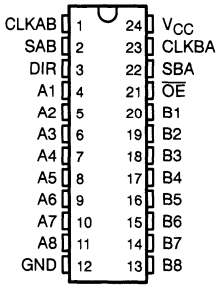
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

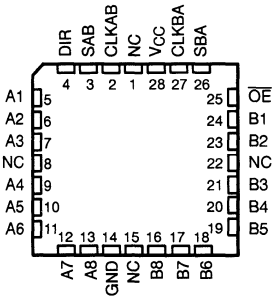
Figure 1. Load Circuit and Voltage Waveforms

- **Independent Registers for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **True Data Paths**
- **High-Current 3-State Outputs Can Drive up to 15 LSTTL Loads**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs**

SN54HC646 . . . JT OR W PACKAGE
SN74HC646 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54HC646 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

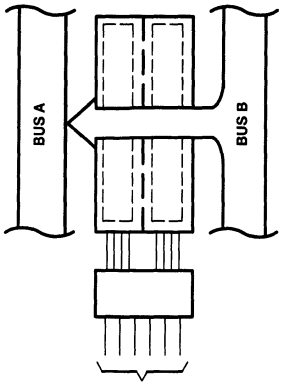
The 'HC646 consist of bus-transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'HC646.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either or both registers.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. DIR determines which bus receives data when $\overline{OE}$ is active (low). In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

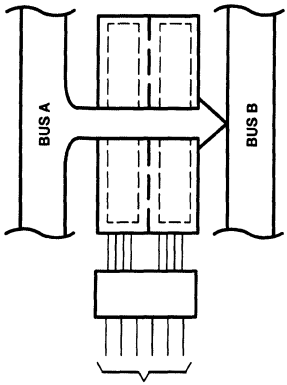
When an output function is disabled, the input function is still enabled and can be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The SN54HC646 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC646 is characterized for operation from –40°C to 85°C.



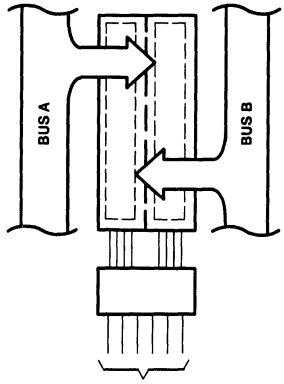
21	3	1	23	2	22
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



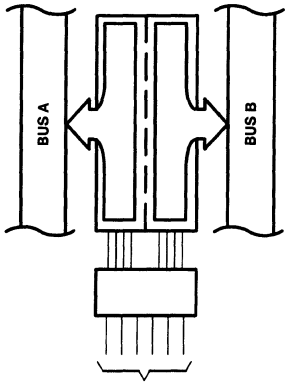
21	3	1	23	2	22
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



21	3	1	23	2	22
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM A, B, OR A AND B



21	3	1	23	2	22
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

TRANSFER STORED DATA TO A AND/OR B

Pin numbers shown are for the DW, JT, NT, and W packages.

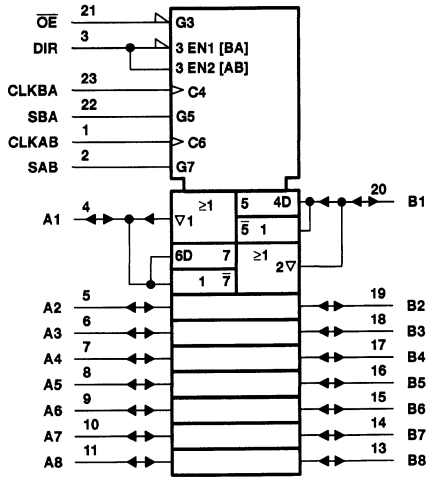
Figure 1. Bus-Management Functions

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

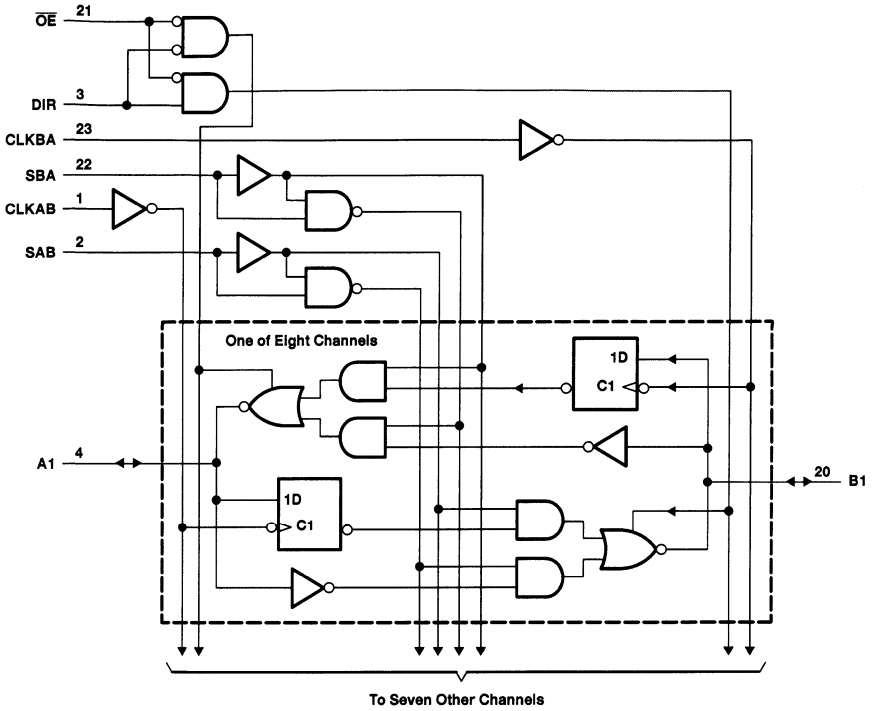
† The data-output functions can be enabled or disabled by various signals at $\overline{OE}$ and DIR. Data-input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, NT, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, NT, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DW package ..... 1.7 W
NT package ..... 1.3 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has a trace length of zero.

recommended operating conditions

			SN54HC646			SN74HC646			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC646		SN74HC646		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
				4.5 V	4.4	4.499		4.4		4.4		
				6 V	5.9	5.999		5.9		5.9		
			I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
			I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}		V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
				4.5 V		0.001	0.1		0.1		0.1	
				6 V		0.001	0.1		0.1		0.1	
			I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
			I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	Control inputs	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	A or B	V_O = V_{CC} or 0		6 V		±0.01	±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i	Control inputs			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC646		SN74HC646		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	2 V	0	6	0	4.3	0	5.5	MHz
		4.5 V	0	31	0	22	0	27	
		6 V	0	36	0	25	0	31	
t_w	Pulse duration, CLKBA or CLKAB high or low	2 V	80		115		95		ns
		4.5 V	16		23		19		
		6 V	14		20		16		
t_{su}	Setup time, A before CLKAB↑ or B before CLKBA↑	2 V	100		150		125		ns
		4.5 V	20		30		25		
		6 V	17		26		21		
t_h	Hold time, A after CLKAB↑ or B after CLKBA↑	2 V	5		5		5		ns
		4.5 V	5		5		5		
		6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC646		SN74HC646		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	11		4.4		5.5		MHz
			4.5 V	31	54		22		27		
			6 V	36	64		25		31		
t_{pd}	CLKBA or CLKAB	A or B	2 V		65	180		270		225	ns
			4.5 V		18	36		54		45	
			6 V		14	31		46		38	
	A or B	B or A	2 V		50	135		205		170	
			4.5 V		14	27		41		34	
			6 V		11	23		35		29	
	SBA or SAB†	A or B	2 V		70	190		285		240	
			4.5 V		20	38		57		48	
			6 V		16	32		48		41	
t_{en}	$\overline{OE}$	A or B	2 V		85	245		370		305	ns
			4.5 V		25	49		74		61	
			6 V		20	42		63		52	
t_{dis}	$\overline{OE}$	A or B	2 V		85	245		370		305	ns
			4.5 V		25	49		74		61	
			6 V		20	42		63		52	
t_{en}	DIR	A or B	2 V		80	245		370		305	ns
			4.5 V		25	49		74		61	
			6 V		20	42		63		52	
t_{dis}	DIR	A or B	2 V		80	245		370		305	ns
			4.5 V		25	49		74		61	
			6 V		20	42		63		52	
t_t		Any	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC646		SN74HC646		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	CLKBA or CLKAB	A or B	2 V		90	265		400		330	ns
			4.5 V		24	53		80		66	
			6 V		20	46		68		57	
	A or B	B or A	2 V		70	220		335		280	
			4.5 V		20	44		67		56	
			6 V		15	38		57		49	
	SBA or SAB†	A or B	2 V		80	275		415		345	
			4.5 V		24	55		83		69	
			6 V		20	47		70		60	
t_{en}	$\overline{OE}$	A or B	2 V		113	330		500		410	ns
			4.5 V		33	66		100		82	
			6 V		27	57		85		71	
	DIR	A or B	2 V		113	330		500		410	
			4.5 V		33	66		100		82	
			6 V		27	57		85		71	
t_t		Any	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		43	

† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	50	pF

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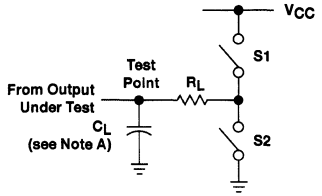
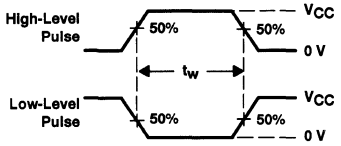
PARAMETER MEASUREMENT INFORMATION

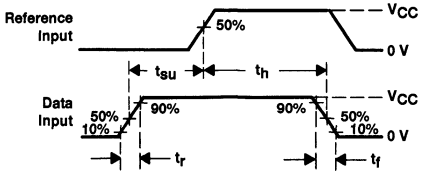


LOAD CIRCUIT

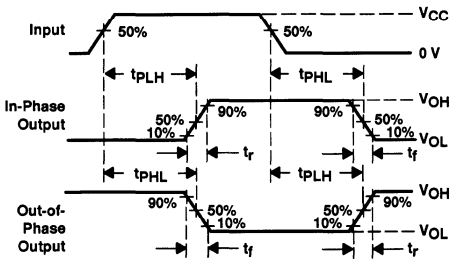
PARAMETER		RL	CL	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



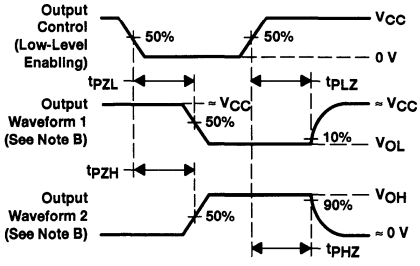
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



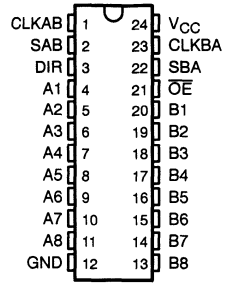
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

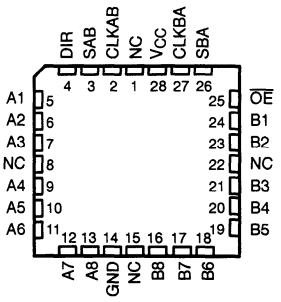
Figure 2. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Independent Registers for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **True Data Paths**
- **High-Current 3-State Outputs Can Drive up to 15 LSTTL Loads**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs**

SN54HCT646 . . . JT OR W PACKAGE
SN74HCT646 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54HCT646 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

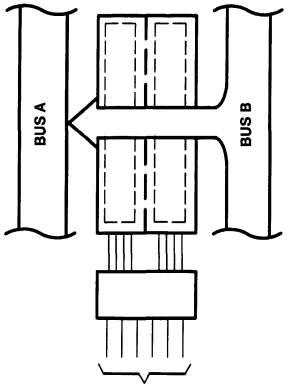
The 'HCT646 consist of bus-transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'HCT646.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs control the transceiver functions. In the transceiver mode, data present at the high-impedance port can be stored in either or both registers.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. DIR determines which bus receives data when $\overline{OE}$ is active (low). In the isolation mode ($\overline{OE}$ high), A data can be stored in one register and/or B data can be stored in the other register.

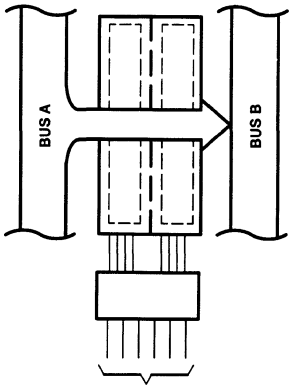
When an output function is disabled, the input function is still enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

The SN54HCT646 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT646 is characterized for operation from –40°C to 85°C.



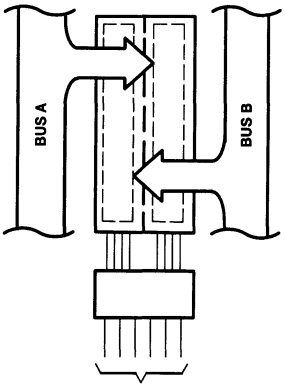
21	3	1	23	2	22
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



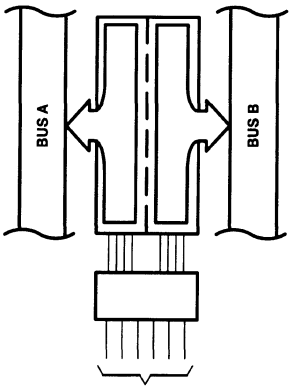
21	3	1	23	2	22
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



21	3	1	23	2	22
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM A, B, OR A AND B



21	3	1	23	2	22
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

TRANSFER STORED DATA TO A AND/OR B

Pin numbers shown are for the DW, JT, NT, and W packages.

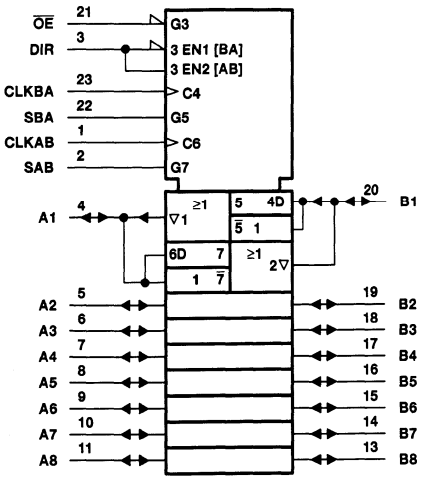
Figure 1. Bus-Management Functions

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

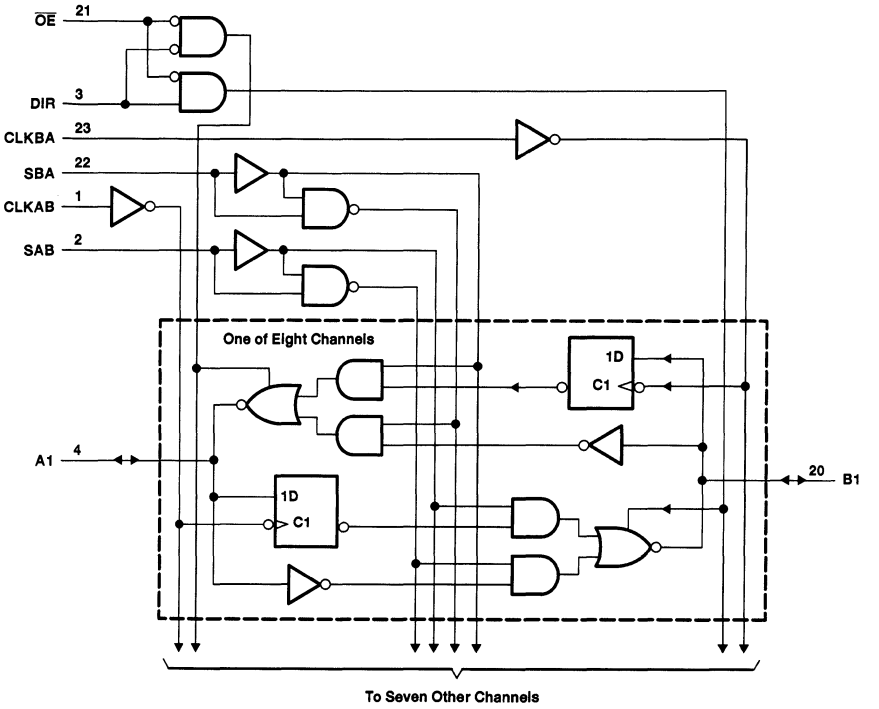
† The data-output functions can be enabled or disabled by various signals at $\overline{OE}$ and DIR. Data-input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, NT, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, NT, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DW package ..... 1.7 W
NT package ..... 1.3 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has a trace length of zero.

recommended operating conditions

			SN54HCT646			SN74HCT646			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time		0		500	0		500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT646		SN74HCT646		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	4.5 V	4.4	4.499		4.4		4.4		V
			I_{OH} = –6 mA		3.98	4.3		3.7		3.84		
V_{OL}		V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
			I_{OL} = 6 mA			0.17	0.26		0.4		0.33	
I_I	Control inputs	V_I = V_{CC} or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	A or B	V_O = V_{CC} or 0		5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or 0, I_O = 0		5.5 V			8		160		80	μA
ΔI_{CC}†		One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i	Control inputs			4.5 V to 5.5 V		3	10		10		10	pF

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HCT646		SN74HCT646		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	4.5 V	0	31	0	22	0	27	MHz
		5.5 V	0	36	0	24	0	29	
t_w	Pulse duration, CLKBA or CLKAB high or low	4.5 V	16		23		19		ns
		5.5 V	14		21		17		
t_{su}	Setup time, A before CLKAB↑ or B before CLKBA↑	4.5 V	20		30		25		ns
		5.5 V	18		27		23		
t_h	Hold time, A after CLKAB↑ or B after CLKBA↑	4.5 V	5		5		5		ns
		5.5 V	5		5		5		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT646		SN74HCT646		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			4.5 V	31	54		22		27		MHz
			5.5 V	36	64		24		29		
t_{pd}	CLKBA or CLKAB	A or B	4.5 V		18	36		54		45	ns
			5.5 V		16	32		49		41	
	A or B	B or A	4.5 V		14	27		41		34	
			5.5 V		12	24		37		31	
	SBA or SAB†	A or B	4.5 V		20	38		57		48	
			5.5 V		17	34		51		43	
t_{en}	$\overline{OE}$	A or B	4.5 V		25	49		74		61	ns
			5.5 V		22	44		67		55	
t_{dis}	$\overline{OE}$	A or B	4.5 V		25	49		74		61	ns
			5.5 V		22	44		67		55	
t_{en}	DIR	A or B	4.5 V		25	49		74		61	ns
			5.5 V		22	44		67		55	
t_{dis}	DIR	A or B	4.5 V		25	49		74		61	ns
			5.5 V		22	44		67		55	
t_t		Any	4.5 V		9	12		18		15	ns
			5.5 V		7	11		16		14	

† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 2)

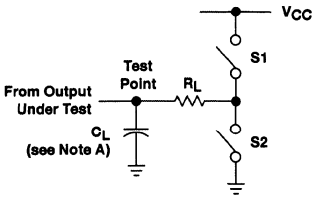
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT646		SN74HCT646		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	CLKBA or CLKAB	A or B	4.5 V		24	53		80		66	ns
			5.5 V		22	47		52		60	
	A or B	B or A	4.5 V		22	44		67		55	
			5.5 V		20	39		60		50	
	SBA or SAB†	A or B	4.5 V		26	55		83		69	
			5.5 V		24	49		74		62	
t_{en}	$\overline{OE}$	A or B	4.5 V		33	66		100		87	ns
			5.5 V		22	59		90		74	
	DIR	A or B	4.5 V		33	66		100		87	
			5.5 V		22	59		90		74	
t_t		Any	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

operating characteristics, T_A = 25°C

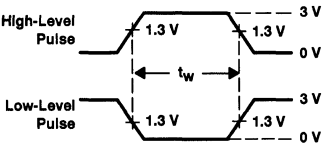
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	50	pF

PARAMETER MEASUREMENT INFORMATION

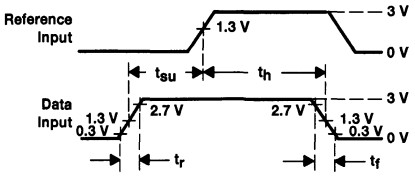


LOAD CIRCUIT

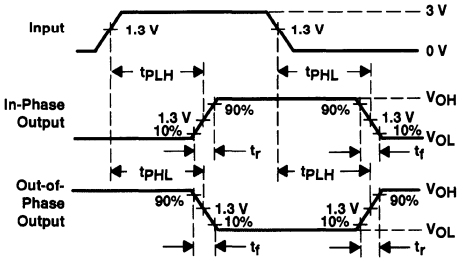
PARAMETER		RL	CL	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



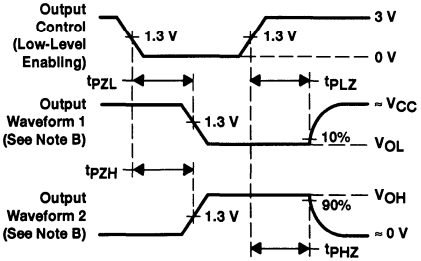
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES



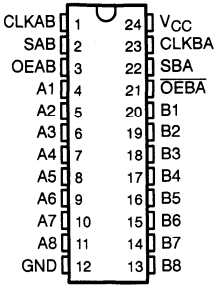
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

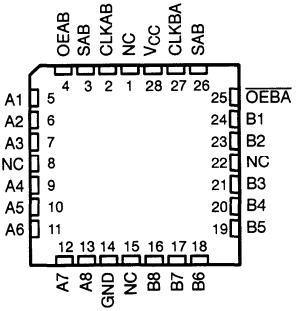
Figure 2. Load Circuit and Voltage Waveforms

- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **True Data Paths**
- **High-Current 3-State Outputs Can Drive up to 15 LSTTL Loads**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs**

SN54HC652 . . . JT OR W PACKAGE
SN74HC652 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54HC652 . . . FK PACKAGE
(TOP VIEW)



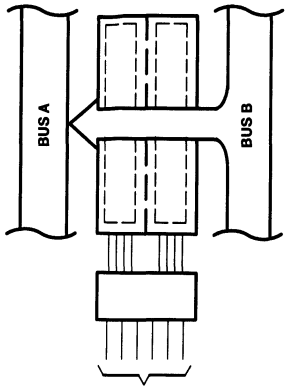
NC – No internal connection

description

These devices consist of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select real-time or stored data transfer. A low input level selects real-time data, and a high input level selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'HC652.

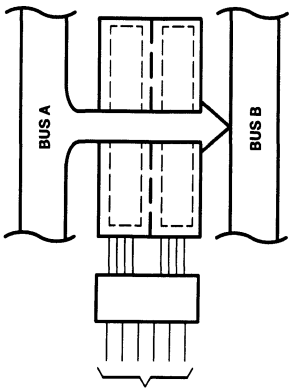
Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) terminals regardless of the select- or output-control terminals. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. When all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

The SN54HC652 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC652 is characterized for operation from –40°C to 85°C.



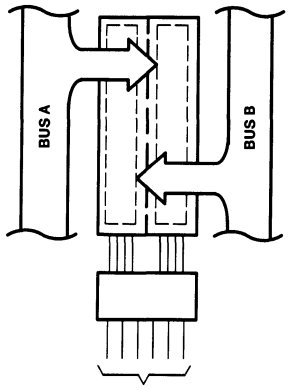
3	21	1	23	2	22
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



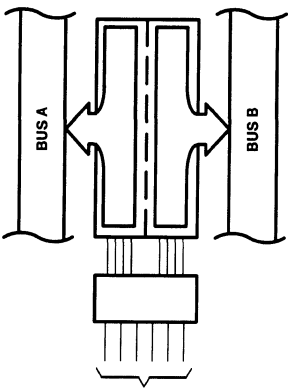
3	21	1	23	2	22
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



3	21	1	23	2	22
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM A, B, OR A AND B



3	21	1	23	2	22
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER STORED DATA TO A AND/OR B

Pin numbers shown are for the DW, JT, NT, and W packages.

Figure 1. Bus-Management Functions

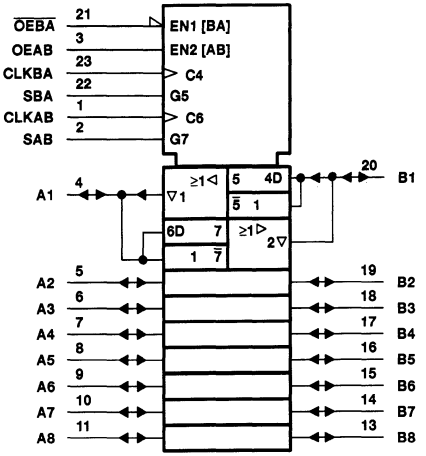
FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

† The data output functions may be enabled or disabled by a variety of level combinations at OEAB or $\overline{OEBA}$. Data input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition on the clock inputs.

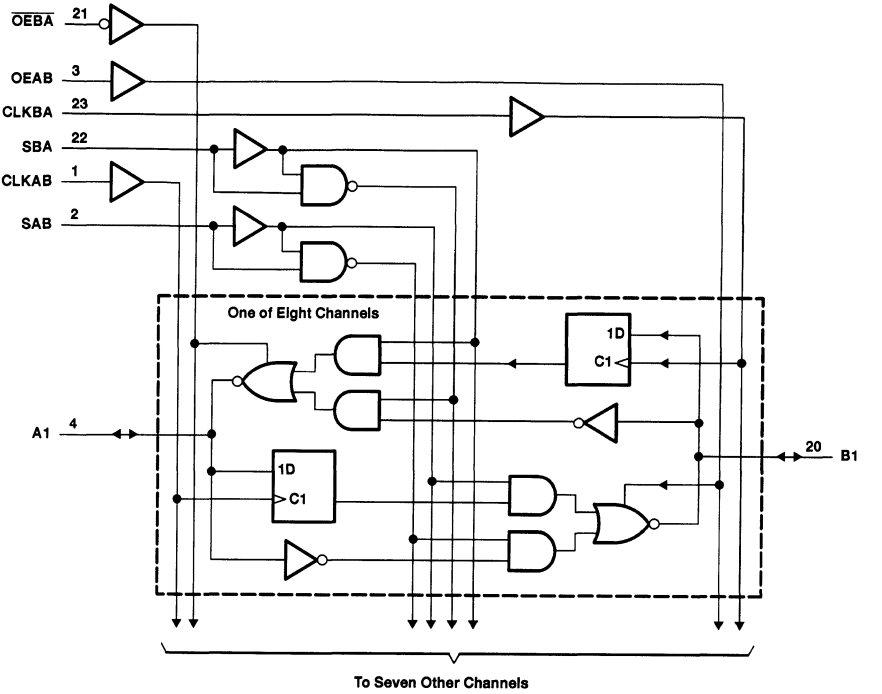
‡ Select control = L; clocks can occur simultaneously.
Select control = H; clocks must be staggered in order to load both registers.

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, NT, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, NT, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DW package ..... 1.7 W
NT package ..... 1.3 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has a trace length of zero.

recommended operating conditions

			SN54HC652			SN74HC652			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC652		SN74HC652		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
				4.5 V	4.4	4.499		4.4		4.4		
				6 V	5.9	5.999		5.9		5.9		
			I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
			I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}		V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
				4.5 V		0.001	0.1		0.1		0.1	
				6 V		0.001	0.1		0.1		0.1	
			I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
			I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	Control inputs	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	A or B	V_O = V_{CC} or GND		6 V		±0.01	±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i	Control inputs			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC652		SN74HC652		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	2 V	0	6	0	4.3	0	5.5	MHz
		4.5 V	0	31	0	22	0	27	
		6 V	0	36	0	25	0	31	
t_w	Pulse duration, CLKBA or CLKAB high or low	2 V	80		115		95		ns
		4.5 V	16		23		19		
		6 V	14		20		16		
t_{su}	Setup time, A before CLKAB↑ or B before CLKBA↑	2 V	100		150		125		ns
		4.5 V	20		30		25		
		6 V	17		26		21		
t_h	Hold time, A after CLKAB↑ or B after CLKBA↑	2 V	5		5		5		ns
		4.5 V	5		5		5		
		6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC652		SN74HC652		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	10		4.3		5.5		MHz
			4.5 V	31	40		22		27		
			6 V	36	45		25		31		
t_{pd}	CLKBA or CLKAB	A or B	2 V		65	180		270		225	ns
			4.5 V		18	36		54		45	
			6 V		14	31		46		38	
	A or B	B or A	2 V		50	135		205		170	
			4.5 V		14	27		41		34	
			6 V		11	23		35		29	
	SBA or SAB†	A or B	2 V		70	190		285		240	
			4.5 V		20	38		57		48	
			6 V		16	32		48		41	
t_{en}	$\overline{OEBA}$ or OEAB	A or B	2 V		85	245		370		305	ns
			4.5 V		25	49		74		61	
			6 V		20	42		63		52	
t_{dis}	$\overline{OEBA}$ or OEAB	A or B	2 V		50	245		370		305	ns
			4.5 V		23	49		74		61	
			6 V		20	42		63		52	
t_t		Any	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 2)

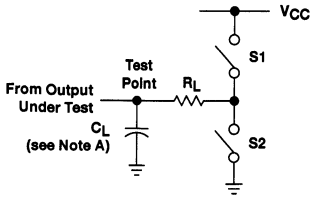
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC652		SN74HC652		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	CLKBA or CLKAB	A or B	2 V		90	265		400		330	ns
			4.5 V		24	53		80		66	
			6 V		18	46		68		57	
	A or B	B or A	2 V		70	220		330		275	
			4.5 V		20	44		70		55	
			6 V		15	38		57		48	
	SBA or SAB†	A or B	2 V		80	275		415		345	
			4.5 V		24	55		83		69	
			6 V		20	47		70		60	
t_{en}	$\overline{OEBA}$ or OEAB	A or B	2 V		100	330		500		410	ns
			4.5 V		33	66		100		82	
			6 V		27	57		85		71	
t_t		Any	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		43	

† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

operating characteristics, T_A = 25°C

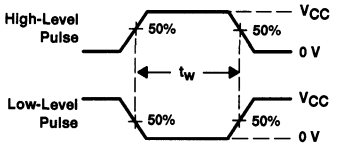
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	50	pF

PARAMETER MEASUREMENT INFORMATION

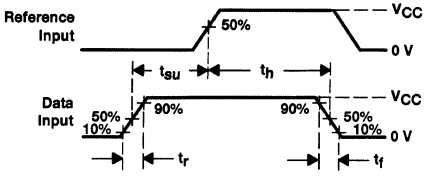


LOAD CIRCUIT

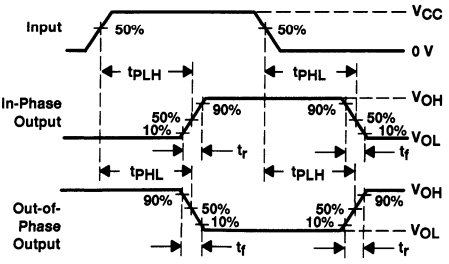
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



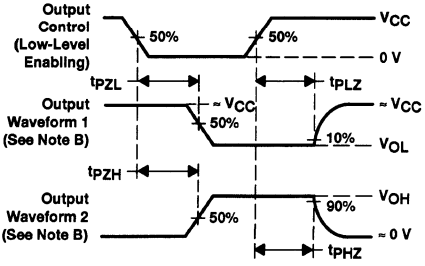
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



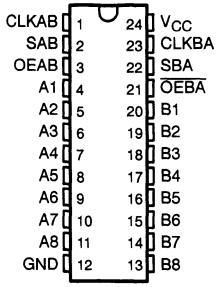
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

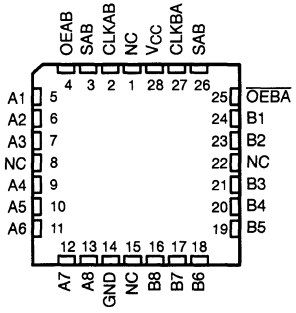
Figure 2. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **True Data Paths**
- **High-Current 3-State Outputs Can Drive up to 15 LSTTL Loads**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs**

SN54HCT652 . . . JT OR W PACKAGE
SN74HCT652 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54HCT652 . . . FK PACKAGE
(TOP VIEW)



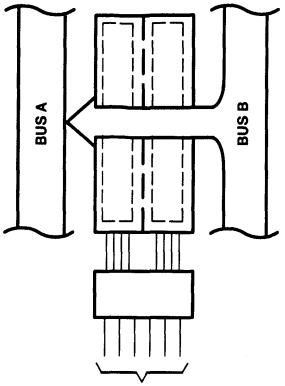
NC – No internal connection

description

The 'HCT652 consist of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select real-time or stored data transfer. A low input level selects real-time data; a high input level selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'HCT652.

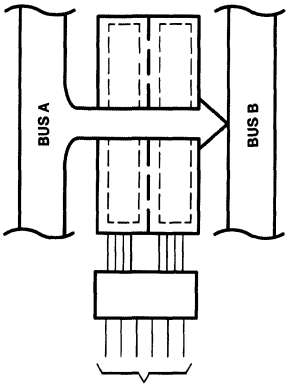
Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) terminals regardless of the select- or output-control terminals. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. When all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

The SN54HCT652 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT652 is characterized for operation from –40°C to 85°C.



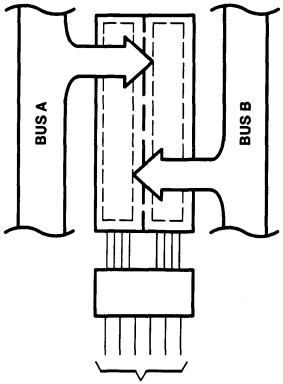
3	21	1	23	2	22
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



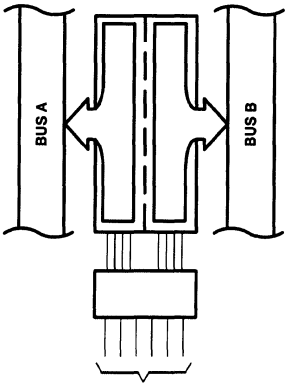
3	21	1	23	2	22
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



3	21	1	23	2	22
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM A, B, OR A AND B



3	21	1	23	2	22
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER STORED DATA TO A AND/OR B

Pin numbers are for the DW, JT, NT, and W packages.

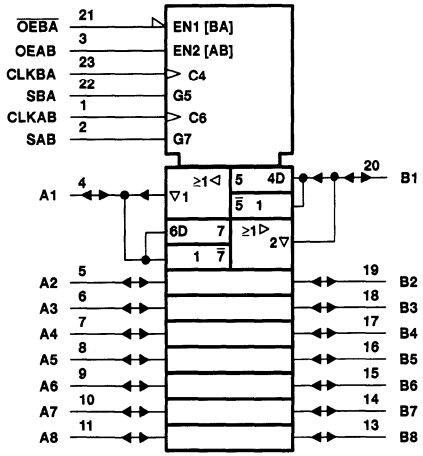
Figure 1. Bus-Management Functions

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

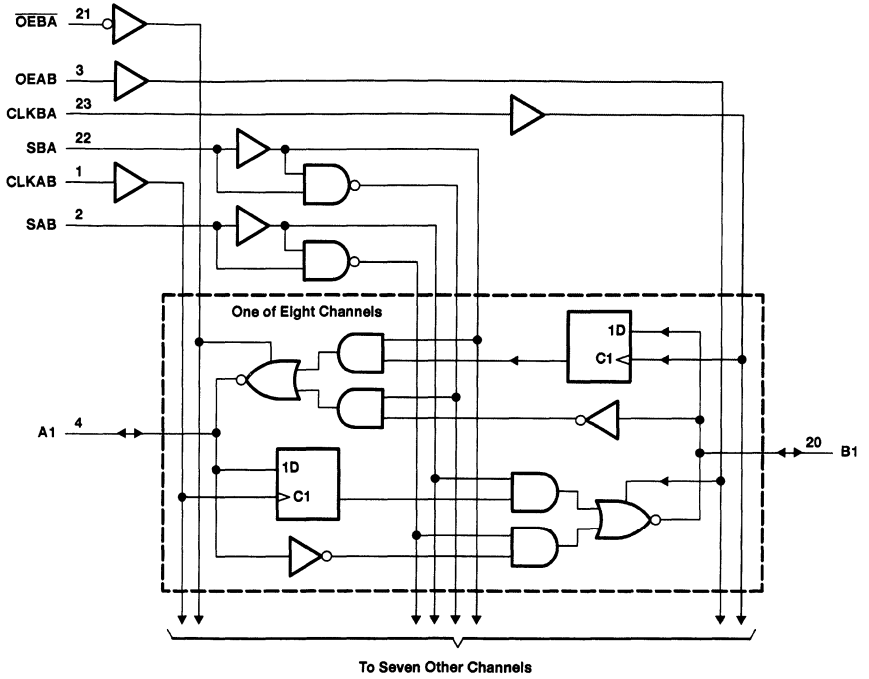
† The data-output functions can be enabled or disabled by a variety of level combinations at OEAB or $\overline{OEBA}$. Data-input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition on the clock inputs.
‡ Select control = L; clocks can occur simultaneously.
Select control = H; clocks must be staggered to load both registers.

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for the DW, JT, NT, and W packages.

logic diagram (positive logic)



Pin numbers are for the DW, JT, NT, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DW package	1.7 W
NT package	1.3 W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has a trace length of zero.

recommended operating conditions

			SN54HCT652			SN74HCT652			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time		0		500	0		500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT652		SN74HCT652		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	4.5 V	4.4	4.499		4.4		4.4		V
			I_{OH} = –6 mA		3.98	4.3		3.7		3.84		
V_{OL}		V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
			I_{OL} = 6 mA			0.17	0.26		0.4		0.33	
I_I	Control inputs	V_I = V_{CC} or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	A or B	V_O = V_{CC} or 0, V_I = V_{IH} or V_{IL}, Data = V_{CC} or 0		5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or 0, I_O = 0		5.5 V			8		160		80	μA
ΔI_{CC}†		One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i	Control inputs			4.5 V to 5.5 V		3	10		10		10	pF

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HCT652		SN74HCT652		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	4.5 V	0	25	0	17	0	20	MHz
		5.5 V	0	28	0	19	0	22	
t_w	Pulse duration, CLKBA or CLKAB high or low	4.5 V	20		30		25		ns
		5.5 V	18		27		23		
t_{su}	Setup time, A before CLKAB↑ or B before CLKBA↑	4.5 V	15		23		19		ns
		5.5 V	14		21		17		
t_h	Hold time, A after CLKAB↑ or B after CLKBA↑	4.5 V	5		5		5		ns
		5.5 V	5		5		5		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT652		SN74HCT652		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			4.5 V	25	35		17		20		MHz
			5.5 V	28	40		19		22		
t_{pd}	CLKBA or CLKAB	A or B	4.5 V		18	36		54		45	ns
			5.5 V		16	32		48		41	
	A or B	B or A	4.5 V		14	27		41		34	
			5.5 V		12	24		37		31	
	SBA or SAB†	A or B	4.5 V		20	38		57		48	
			5.5 V		17	34		51		43	
t_{en}	$\overline{OEBA}$ or OEAB	A or B	4.5 V		25	49		74		61	ns
			5.5 V		22	44		67		55	
t_{dis}	$\overline{OEBA}$ or OEAB	A or B	4.5 V		25	49		74		61	ns
			5.5 V		22	44		67		55	
t_t		Any	4.5 V		9	12		18		15	ns
			5.5 V		7	11		16		14	

† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 2)

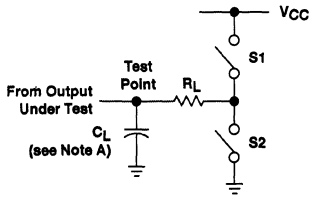
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT652		SN74HCT652		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	CLKBA or CLKAB	A or B	4.5 V		24	53		80		66	ns
			5.5 V		22	47		73		60	
	A or B	B or A	4.5 V		22	44		70		55	
			5.5 V		20	39		60		50	
	SBA or SAB†	A or B	4.5 V		26	55		83		69	
			5.5 V		24	49		74		62	
t_{en}	$\overline{OEBA}$ or OEAB	A or B	4.5 V		33	66		100		82	ns
			5.5 V		30	59		90		74	
t_t		Any	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

operating characteristics, T_A = 25°C

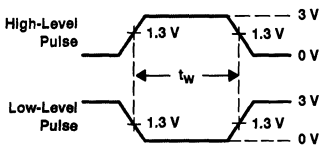
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	50	pF

PARAMETER MEASUREMENT INFORMATION

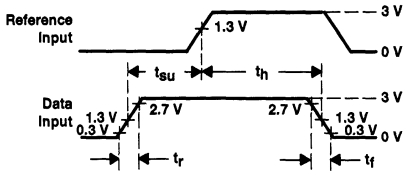


LOAD CIRCUIT

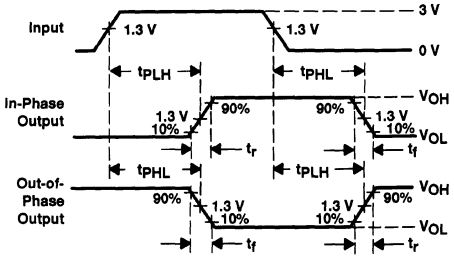
PARAMETER		RL	CL	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



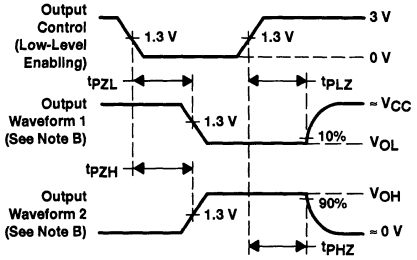
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

SCLS018B – MARCH 1984 – REVISED JANUARY 1996

- **Compare Two 8-Bit Words**
- **100-kΩ Pullup Resistors Are on the Q Inputs**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

These magnitude comparators perform comparisons of two 8-bit binary or BCD words. The 'HC682 feature 100-kΩ pullup termination resistors on the Q inputs for analog or switch data.

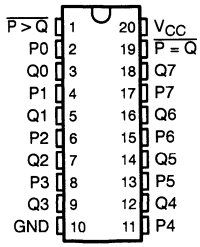
The SN54HC682 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC682 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

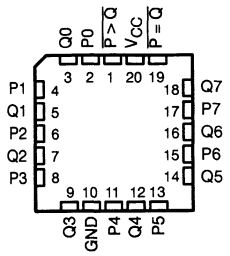
DATA INPUTS P, Q	OUTPUTS	
	$\overline{P = Q}$	$\overline{P > Q}$
P = Q	L	H
P > Q	H	L
P < Q	H	H

The $\overline{P < Q}$ function can be generated by applying $\overline{P = Q}$ and $\overline{P > Q}$ to a 2-input NAND gate.

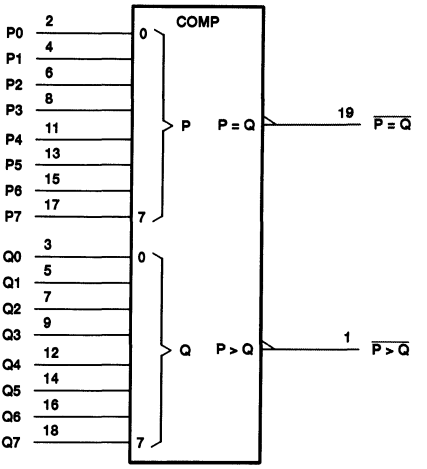
SN54HC682 . . . J OR W PACKAGE
SN74HC682 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC682 . . . FK PACKAGE
(TOP VIEW)

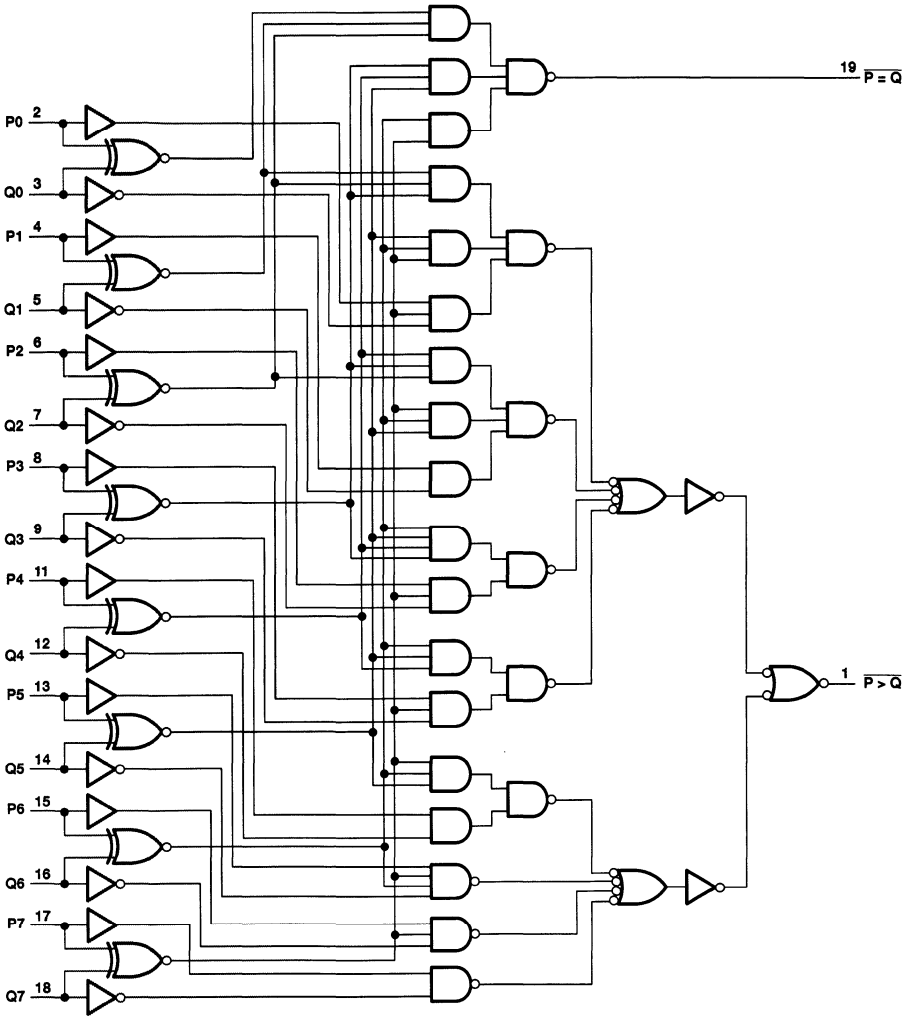


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DW package ..... 1.6 W
N package ..... 1.3 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC682			SN74HC682			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC682		SN74HC682		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_{IH}	V_I = V_{CC}		6 V		0.1	100		1000		1000	nA
I_{IL}	V_I = 0	Q inputs	6 V		–50	–90		–160		–140	μA
		All other inputs	6 V		–0.1	–100		–1000		–1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V		480	700		1300		1100	μA
C_i			2 V to 6 V		3	10		10		10	pF

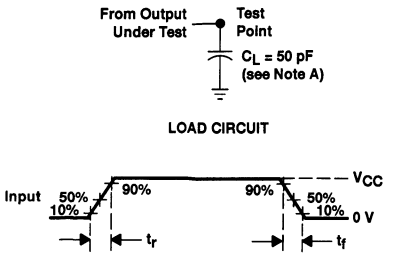
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC682		SN74HC682		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	P or Q	Any	2 V		130	275		413		344	ns
			4.5 V		26	55		88		69	
			6 V		22	47		70		58	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

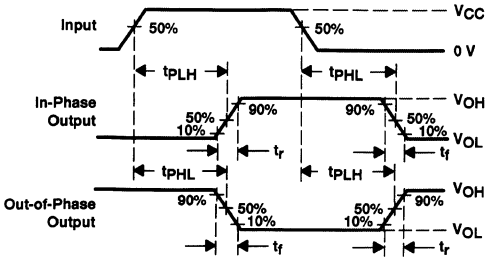
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	40	pF

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

SCLS340 – MARCH 1996

- **Compare Two 8-Bit Words**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

These magnitude comparators perform comparisons of two 8-bit binary or BCD words. These devices provide $\overline{P = Q}$ and $\overline{P > Q}$ outputs.

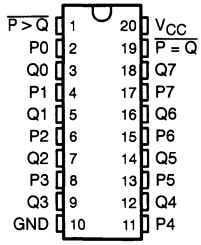
The SN54HC684 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC684 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

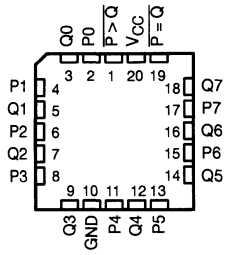
DATA INPUTS P, Q	OUTPUTS	
	$\overline{P = Q}$	$\overline{P > Q}$
P = Q	L	H
P > Q	H	L
P < Q	H	H

The $\overline{P < Q}$ function can be generated by applying $\overline{P = Q}$ and $\overline{P > Q}$ to a 2-input NAND gate.

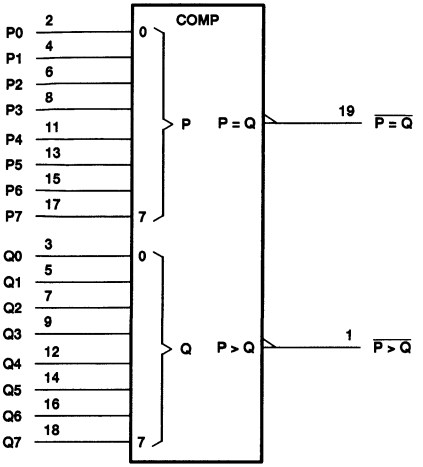
SN54HC684 . . . J OR W PACKAGE
SN74HC684 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC684 . . . FK PACKAGE
(TOP VIEW)

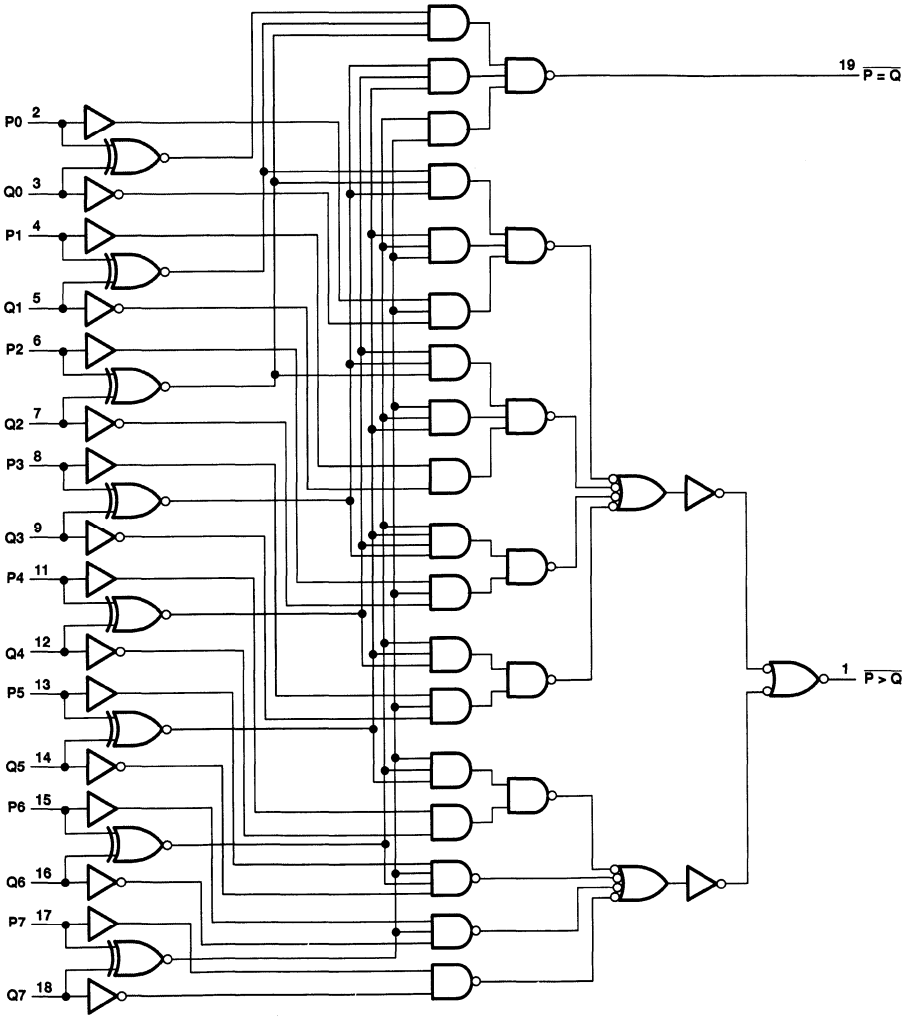


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DW package ..... 1.6 W
N package ..... 1.3 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC684			SN74HC684			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC684		SN74HC684		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.30		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_{IH}	V_I = V_{CC}		6 V		0.1	100		1000		1000	nA
I_{IL}	V_I = 0		6 V		–0.1	–100		–1000		–1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

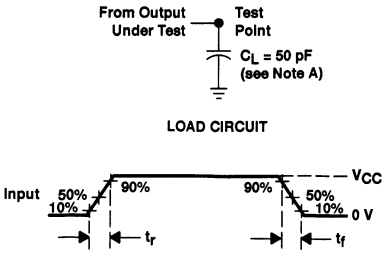
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC684		SN74HC684		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	P or Q	Any	2 V		130	275		413		344	ns
			4.5 V		26	55		88		69	
			6 V		22	47		70		58	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

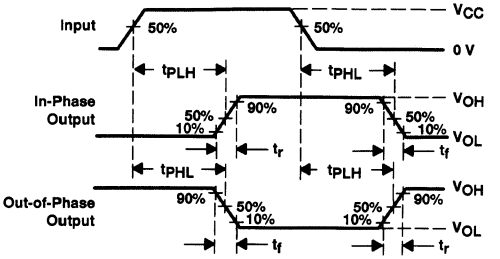
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	40	pF

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Compare Two 8-Bit Words**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

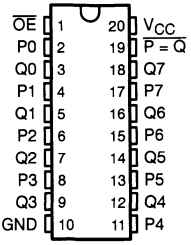
These identity comparators perform comparisons of two 8-bit binary or BCD words. An output-enable ($\overline{OE}$) input may be used to force the output to the high level.

The SN54HC688 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC688 is characterized for operation from –40°C to 85°C.

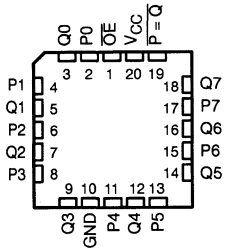
FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	$\overline{OE}$	$\overline{P = Q}$
P = Q	L	L
P > Q	X	H
P < Q	X	H
X	H	H

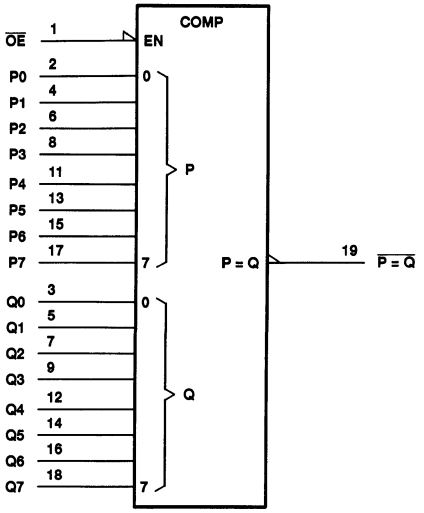
SN54HC688 . . . J OR W PACKAGE
SN74HC688 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC688 . . . FK PACKAGE
(TOP VIEW)

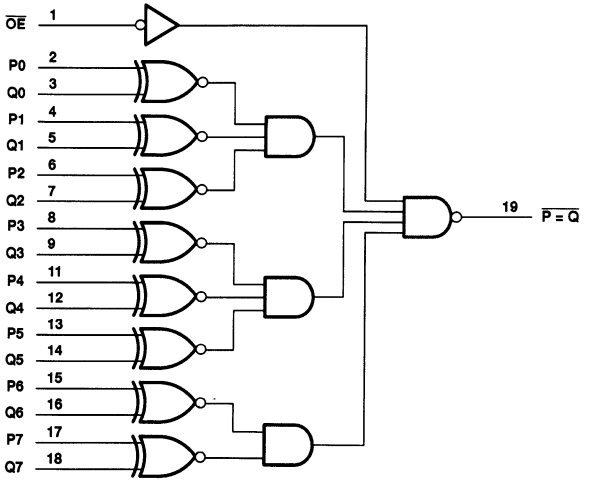


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DW package ..... 1.6 W
N package ..... 1.3 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC688			SN74HC688			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC688		SN74HC688		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

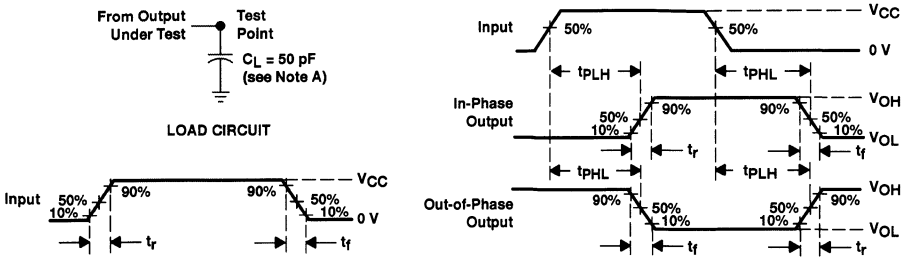
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC688		SN74HC688		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	P or Q	$\overline{P = Q}$	2 V		113	210		313		265	ns
			4.5 V		30	42		63		53	
			6 V		24	36		53		45	
	$\overline{OE}$	$\overline{P = Q}$	2 V		66	120		179		151	
			4.5 V		16	24		36		30	
			6 V		14	20		30		26	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	40	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

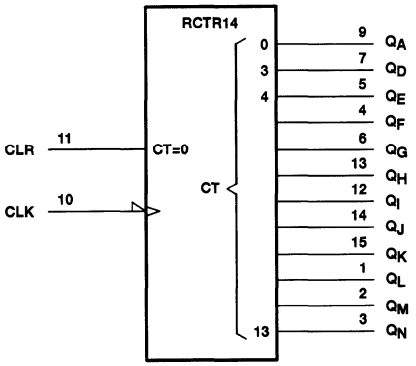
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

These devices are 14-stage binary ripple-carry counters that advance on the negative-going edge of the clock pulse. The counters are reset to zero (all outputs low) independently of the clock (CLK) input when the clear (CLR) input goes high.

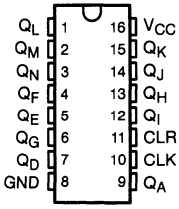
The SN54HC4020 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC4020 is characterized for operation from –40°C to 85°C.

logic symbol†

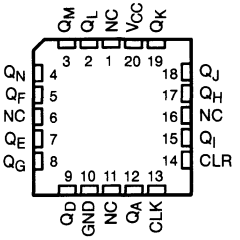


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

SN54HC4020 . . . J OR W PACKAGE
SN74HC4020 . . . D OR N PACKAGE
(TOP VIEW)

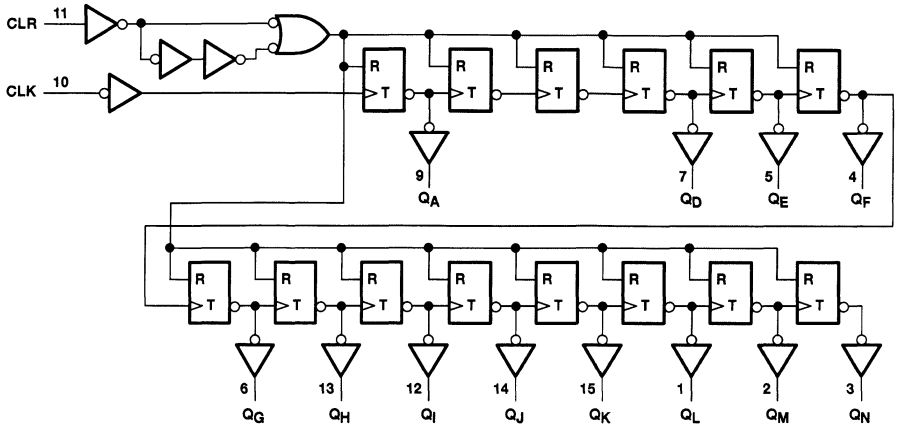


SN54HC4020 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC4020			SN74HC4020			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC4020		SN74HC4020		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V			±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC4020		SN74HC4020		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	5.5	0	3.7	0	4.3	MHz
			4.5 V	0	28	0	19	0	22	
			6 V	0	33	0	22	0	25	
t_w	Pulse duration	CLK high or low	2 V	90		135		115		ns
			4.5 V	18		27		23		
			6 V	15		23		20		
		CLR high	2 V	70		105		90		
			4.5 V	14		21		18		
			6 V	12		18		25		
t_{su}	Setup time, CLR inactive before CLK↓		2 V	60		90		75		ns
			4.5 V	12		18		15		
			6 V	10		15		13		

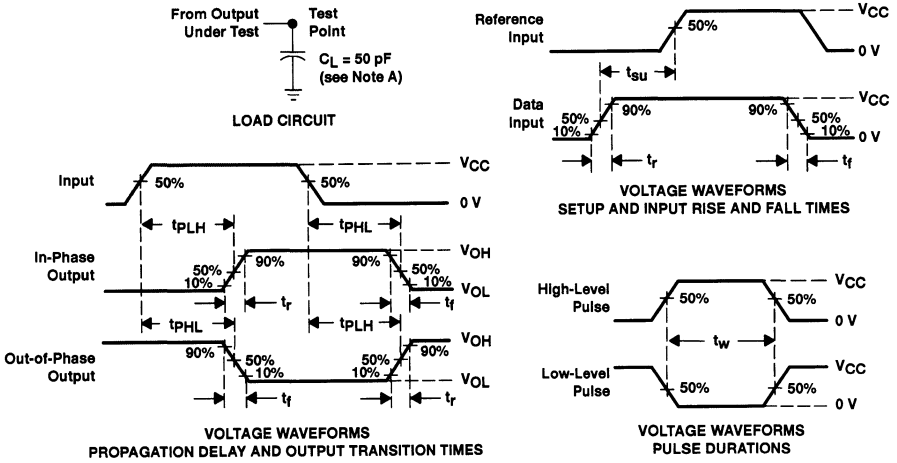
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC4020		SN74HC4020		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	5.5	10		3.7		4.3		MHz
			4.5 V	28	45		19		22		
			6 V	33	53		22		25		
t_{pd}	CLK	Q_A	2 V		62	150		225		190	ns
			4.5 V		16	30		45		38	
			6 V		12	26		38		32	
t_{PHL}	CLR	Any	2 V		63	140		210		175	ns
			4.5 V		17	28		42		35	
			6 V		13	24		36		30	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	88	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

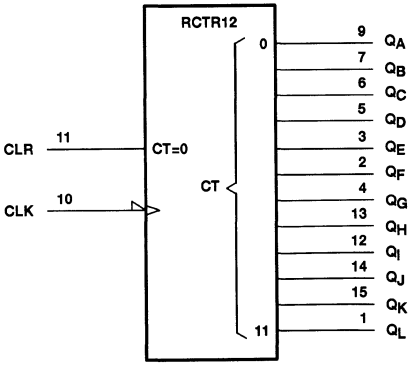
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

The 'HC4040 are 12-stage asynchronous binary counters with the outputs of all stages available externally. A high level at the clear (CLR) input asynchronously clears the counter and resets all outputs low. The count is advanced on a high-to-low transition at the clock (CLK) input. Applications include time-delay circuits, counter controls, and frequency-dividing circuits.

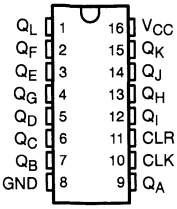
The SN54HC4040 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC4040 is characterized for operation from –40°C to 85°C.

logic symbol†

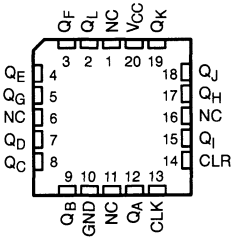


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

SN54HC4040 . . . J OR W PACKAGE
SN74HC4040 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)

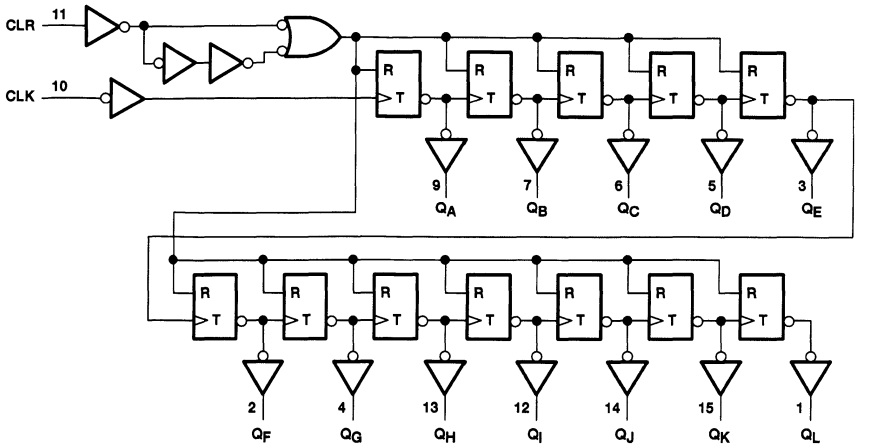


SN54HC4040 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
DB package ..... 0.55 W
N package ..... 1.1 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC4040			SN74HC4040			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t†	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

† If this device is used in the threshold region (from V_{IL}max = 0.5 V to V_{IH}min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC4040		SN74HC4040		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC4040		SN74HC4040		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock} Clock frequency		2 V	0	5.5	0	3.7	0	4.3	MHz
		4.5 V	0	28	0	19	0	22	
		6 V	0	33	0	22	0	25	
t_w Pulse duration	CLK high or low	2 V	90		135		115		ns
		4.5 V	18		27		23		
		6 V	15		23		20		
	CLR high	2 V	70		105		90		
		4.5 V	14		21		18		
		6 V	12		18		15		
t_{su} Setup time, CLR inactive before CLK↓		2 V	60		90		75		ns
		4.5 V	12		18		15		
		6 V	10		15		13		

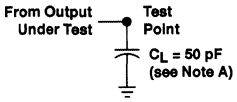
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC4040		SN74HC4040		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	5.5	10		3.7		4.3		MHz
			4.5 V	28	45		19		22		
			6 V	33	53		22		25		
t_{pd}	CLK	Q_A	2 V		62	150		225		190	ns
			4.5 V		16	30		45		38	
			6 V		12	26		38		32	
t_{PHL}	CLR	Any	2 V		63	140		210		175	ns
			4.5 V		17	28		42		35	
			6 V		13	24		36		30	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

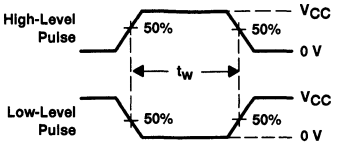
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	88	pF

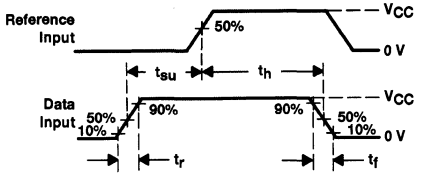
PARAMETER MEASUREMENT INFORMATION



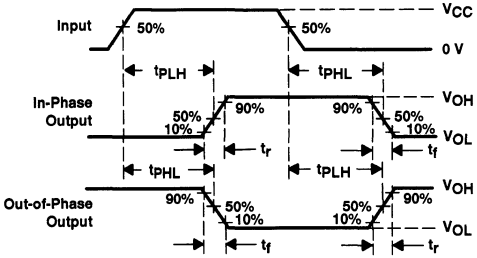
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

SCLS161A – DECEMBER 1982 – REVISED JANUARY 1996

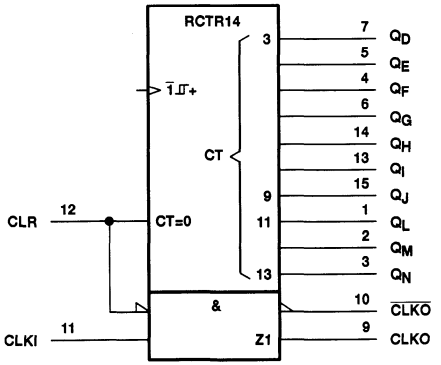
- **Allow Design of Either RC or Crystal Oscillator Circuits**
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

The 'HC4060 consist of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal-oscillator circuits. A high-to-low transition on the clock (CLKI) input increments the counter. A high level at the clear (CLR) input disables the oscillator ($\overline{CLKO}$ goes high and CLKO goes low) and resets the counter to zero (all Q outputs low).

The SN54HC4060 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC4060 is characterized for operation from –40°C to 85°C.

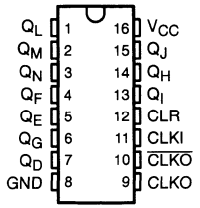
logic symbol†



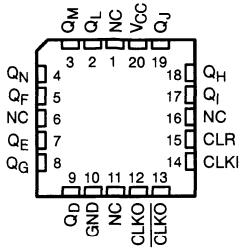
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, J, N, and W packages.

SN54HC4060 . . . J OR W PACKAGE
SN74HC4060 . . . D OR N PACKAGE
(TOP VIEW)

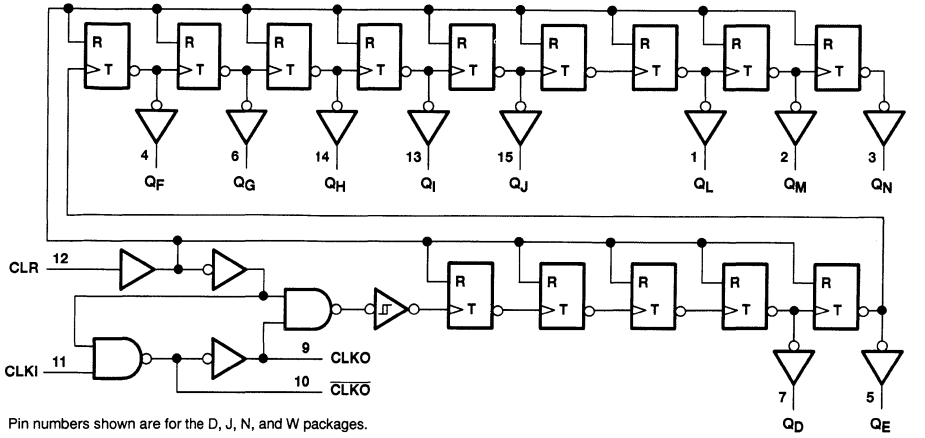


SN54HC4060 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.3 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC4060			SN74HC4060			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC4060		SN74HC4060		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	All outputs	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
				4.5 V	4.4	4.499		4.4		4.4		
				6 V	5.9	5.999		5.9		5.9		
	Q outputs	V_I = V_{IH} or V_{IL}	I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
			I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	All outputs	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
				4.5 V		0.001	0.1		0.1		0.1	
				6 V		0.001	0.1		0.1		0.1	
	Q outputs	V_I = V_{IH} or V_{IL}	I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
			I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I		V_I = V_{CC} or 0		6 V			±0.1	±100		±1000		±1000	nA
I_{CC}		V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i				2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC4060		SN74HC4060		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock} Clock frequency		2 V	0	5.5	0	3.7	0	4.3	MHz
		4.5 V	0	28	0	19	0	22	
		6 V	0	33	0	22	0	25	
t_w Pulse duration	CLKI high or low	2 V	90		135		115		ns
		4.5 V	18		27		23		
		6 V	15		23		20		
	CLR high	2 V	90		135		115		
		4.5 V	18		27		23		
		6 V	15		23		20		
t_{su} Setup time, CLR inactive before CLKI↓		2 V	160		240		200		ns
		4.5 V	32		48		40		
		6 V	27		41		34		

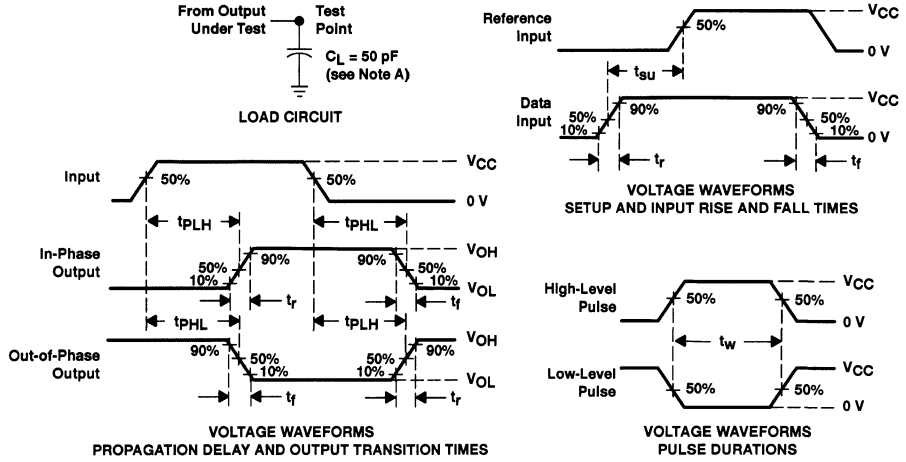
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC4060		SN74HC4060		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	5.5	10		3.7		4.3		MHz
			4.5 V	28	45		19		22		
			6 V	33	53		22		25		
t_{pd}	CLKI	Q_D	2 V		240	490		735		615	ns
			4.5 V		58	98		147		123	
			6 V		42	83		125		105	
t_{PHL}	CLR	Any Q	2 V		66	140		210		175	ns
			4.5 V		18	28		42		35	
			6 V		14	24		36		30	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	30		19		16	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	88	pF

PARAMETER MEASUREMENT INFORMATION



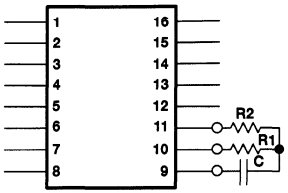
NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

CONNECTING AN RC OSCILLATOR CIRCUIT TO THE 'HC4060

The 'HC4060 consist of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal-oscillator circuits.

When an RC oscillator circuit is implemented, two resistors and a capacitor are required. The components are attached to the terminals as shown below:



To determine the values of capacitance and resistance necessary to obtain a specific oscillator frequency (f), use this formula:

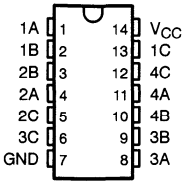
$$f = \frac{1}{2(R1)(C)\left(\frac{0.405\ R2}{R1 + R2} + 0.693\right)}$$

If R2 >> R1 (i.e., R2 = 10R1), the above formula simplifies to:

$$f = \frac{0.455}{RC}$$

- **High Degree of Linearity**
- **High On-Off Output Voltage Ratio**
- **Low Crosstalk Between Switches**
- **Low On-State Impedance — Typically, 50 Ω at V_{CC} = 6 V**
- **Individual Switch Controls**
- **Extremely Low Input Current**
- **Package Options Include Plastic Small-Outline (D), Plastic Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) 300-mil DIPs**

D, DB, PW, OR N PACKAGE
(TOP VIEW)



description

The SN74HC4066 is a silicon-gate CMOS quadruple analog switch designed to handle both analog and digital signals. Each switch permits signals with amplitudes of up to 6 V (peak) to be transmitted in either direction.

Each switch section has its own enable input control (C). A high-level voltage applied to C turns on the associated switch section.

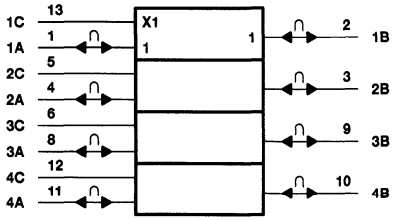
Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

The SN74HC4066 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each switch)

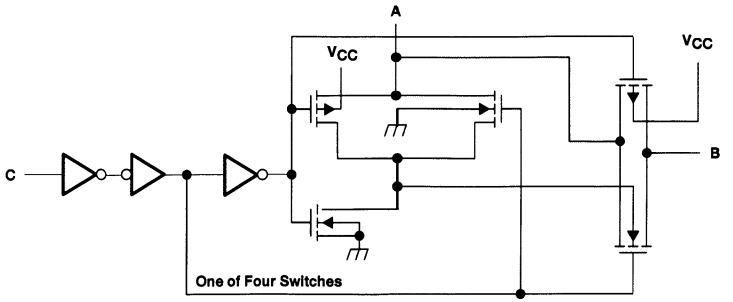
INPUT CONTROL (C)	SWITCH
L	OFF
H	ON

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each switch (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... –0.5 V to 7 V
Control-input diode current, I_I ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
I/O port diode current, I_I ($V_I < 0$ or $V_{I/O} < V_{CC}$) ..... ±20 mA
On-state switch current ($V_{I/O}$ = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB or PW package ..... 0.5 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The maximum power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2‡	5	6	V
$V_{I/O}$	I/O port voltage		0		V_{CC}	V
V_{IH}	High-level input voltage, control inputs	V_{CC} = 2 V	1.5		V_{CC}	V
		V_{CC} = 4.5 V	3.15		V_{CC}	
		V_{CC} = 6 V	4.2		V_{CC}	
V_{IL}	Low-level input voltage, control inputs	V_{CC} = 2 V	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	
		V_{CC} = 6 V	0		1.2	
t_t	Input rise/fall time	V_{CC} = 2 V			1000	ns
		V_{CC} = 4.5 V			500	
		V_{CC} = 6 V			400	
T_A	Operating free-air temperature		–40		85	°C

‡ With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
					MIN	TYP	MAX			
R_{on}	On-state switch resistance		I_T = –1 mA, V_I = 0 to V_{CC}, V_C = V_{IH}, (see Figure 1)	2 V		150				Ω
				4.5 V		50	85		106	
				6 V		30				
$R_{on(p)}$	Peak on resistance		V_I = V_{CC} or GND, V_C = V_{IH}, I_T = –1 mA	2 V		320				Ω
				4.5 V		70	170		215	
				6 V		50				
I_I	Control input current		V_C = 0 or V_{CC}	6 V		±0.1	±100		±1000	nA
I_{Soff}	Off-state switch leakage current		V_I = V_{CC} or 0, V_O = V_{CC} or 0, V_C = V_{IL}, (see Figure 2)	6 V			±0.1		±5	µA
I_{Son}	On-state switch leakage current		V_I = V_{CC} or 0, V_C = V_{IH}, (see Figure 3)	6 V			±0.1		±5	µA
I_{CC}	Supply current		V_I = 0 or V_{CC}, I_O = 0	6 V			2		20	µA
C_i	Input capacitance	A or B		5 V		9				pF
		C				3	10		10	
C_f	Feedthrough capacitance	A to B	V_I = 0			0.5				pF
C_o	Output capacitance	A or B		5 V		9				pF

switching characteristics over recommended operating free-air temperature range

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
						MIN	TYP	MAX			
t_{PLH}, t_{PHL}	Propagation delay time	A or B	B or A	C_L = 50 pF, (see Figure 4)	2 V		10	60		75	ns
					4.5 V		4	12		15	
					6 V		3	10		13	
t_{PZH}, t_{PZL}	Switch turn-on time	C	A or B	R_L = 1 kΩ, C_L = 50 pF, (see Figure 5)	2 V		70	180		225	ns
					4.5 V		21	36		45	
					6 V		18	31		38	
t_{PLZ}, t_{PHZ}	Switch turn-off time	C	A or B	R_L = 1 kΩ, C_L = 50 pF, (see Figure 5)	2 V		50	200		250	ns
					4.5 V		25	40		50	
					6 V		22	34		43	
f_I	Control input frequency	C	A or B	C_L = 15 pF, R_L = 1 kΩ, V_C = V_{CC} or GND, V_O = V_{CC}/2, (see Figure 6)	2 V		15				MHz
					4.5 V		30				
					6 V		30				
	Control feedthrough noise	C	A or B	C_L = 50 pF, R_{in} = R_L = 600 Ω, V_C = V_{CC} or GND, f_{in} = 1 MHz, (see Figure 7)	4.5 V		15				mV (rms)
					6 V		20				

operating characteristics, V_{CC} = 4.5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF,	f = 1 MHz	45	pF
	Minimum through bandwidth, A to B or B to A† [20 log (V_O/V_I)] = –3 dB	C_L = 50 pF, V_C = V_{CC},	R_L = 600 Ω, (see Figure 8)	30	MHz
	Crosstalk between any switches‡	C_L = 10 pF, f_{in} = 1 MHz,	R_L = 50 Ω, (see Figure 9)	45	dB
	Feedthrough, switch off, A to B or B to A‡	C_L = 50 pF, f_{in} = 1 MHz,	R_L = 600 Ω, (see Figure 10)	42	dB
	Amplitude distortion rate, A to B or B to A	C_L = 50 pF, f_{in} = 1 kHz,	R_L = 10 kΩ, (see Figure 11)	0.05%	

† Adjust the input amplitude for output = 0 dBm at f = 10 kHz. Input signal must be a sine wave.
‡ Adjust the input amplitude for output = 0 dBm at f = 1 MHz. Input signal must be a sine wave.

PARAMETER MEASUREMENT INFORMATION

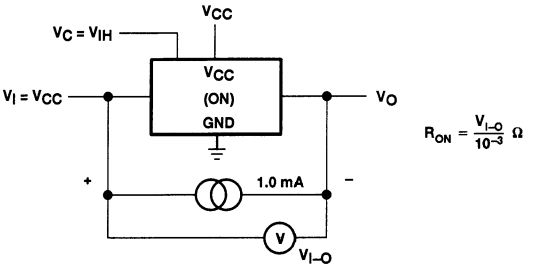
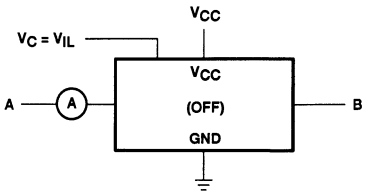


Figure 1. On-State Resistance Test Circuit



$V_S = V_A - V_B$
CONDITION 1: V_A = 0, V_B = V_{CC}
CONDITION 2: V_A = V_{CC}, V_B = 0

Figure 2. Off-State Switch Leakage Current Test Circuit

PARAMETER MEASUREMENT INFORMATION

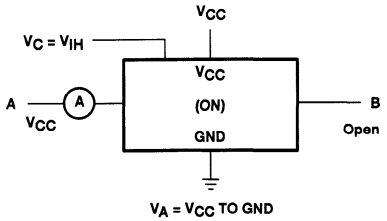


Figure 3. On-State Leakage Current Test Circuit

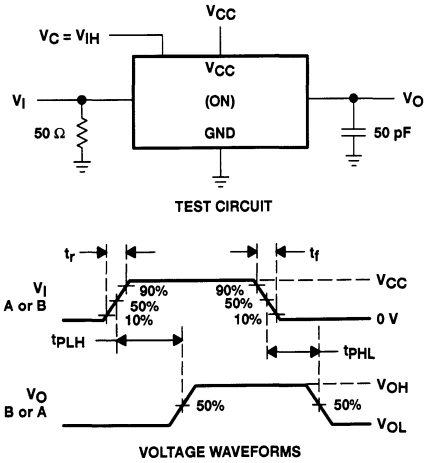
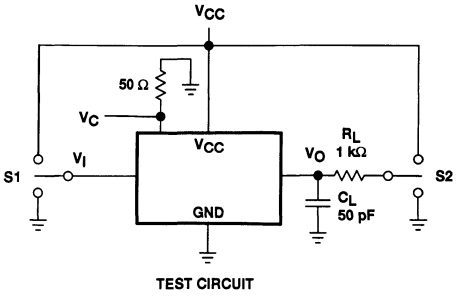


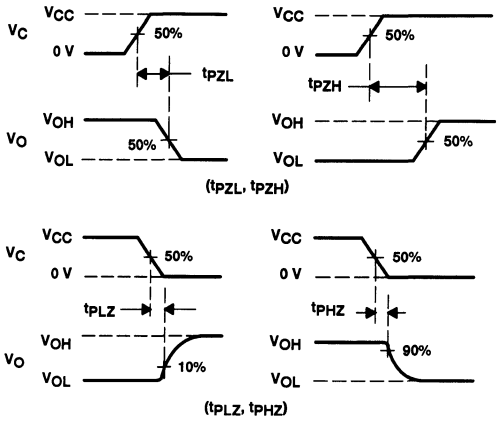
Figure 4. Propagation Delay Time, Signal Input to Signal Output

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

TEST	S1	S2
t_{PZL}	GND	V_{CC}
t_{PZH}	V_{CC}	GND
t_{PLZ}	GND	V_{CC}
t_{PHZ}	V_{CC}	GND



VOLTAGE WAVEFORMS

Figure 5. Switching Time (t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}), Control to Signal Output

PARAMETER MEASUREMENT INFORMATION

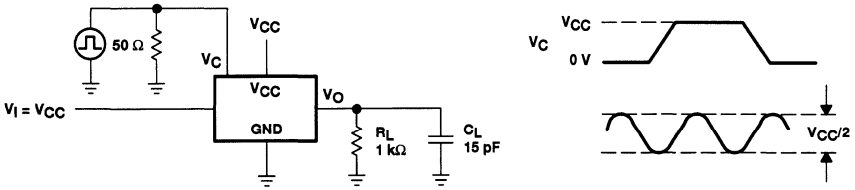


Figure 6. Control Input Frequency

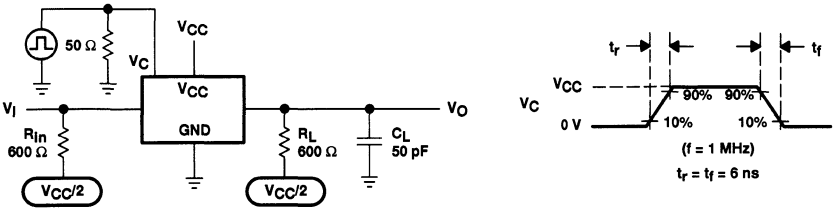


Figure 7. Control Feedthrough Noise

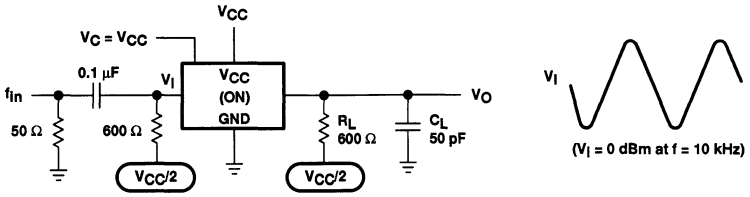


Figure 8. Minimum Through Bandwidth

PARAMETER MEASUREMENT INFORMATION

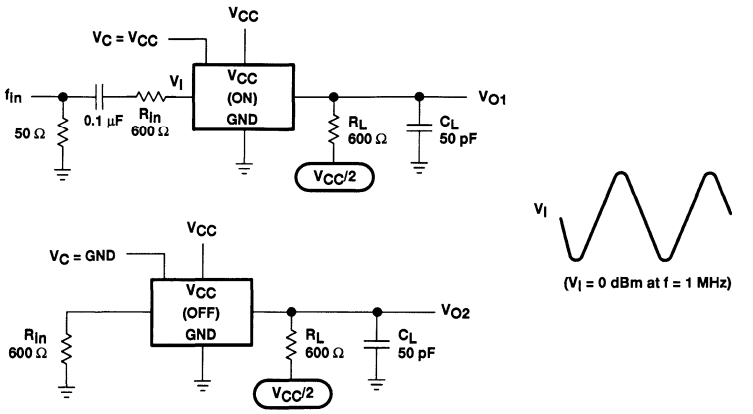


Figure 9. Crosstalk Between Any Two Switches

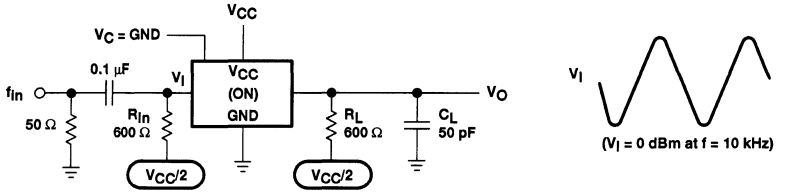


Figure 10. Feedthrough, Switch Off

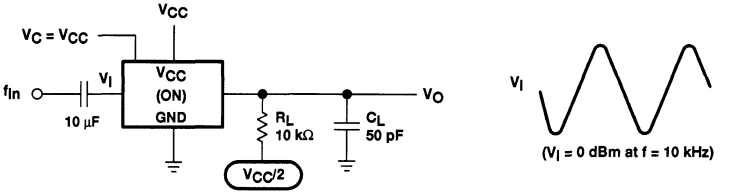
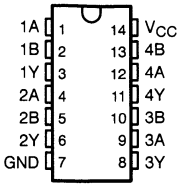


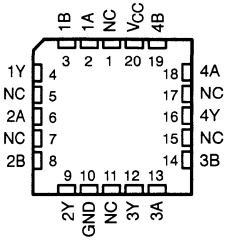
Figure 11. Amplitude Distortion Rate

- **Operation From Very Slow Input Transitions**
- **Temperature-Compensated Threshold Levels**
- **High Noise Immunity**
- **Same Pinouts as 'HC08**
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC7001 . . . J OR W PACKAGE
SN74HC7001 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC7001 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

Each circuit functions as a quadruple AND gate. They perform the Boolean function $Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic. Because of the Schmitt action, the inputs have different input threshold levels for positive- and negative-going signals.

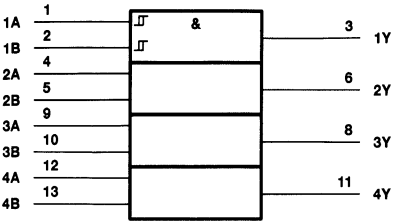
These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

The SN54HC7001 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC7001 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

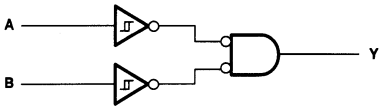
INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC7001			SN74HC7001			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC7001		SN74HC7001		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
V_{T+}			2 V	0.7	1.2	1.5	0.7	1.5	0.7	1.5	V
			4.5 V	1.55	2.5	3.15	1.55	3.15	1.55	3.15	
			6 V	2.1	3.3	4.2	2.1	4.2	2.1	4.2	
V_{T-}			2 V	0.3	0.6	1	0.3	1	0.3	1	V
			4.5 V	0.9	1.6	2.45	0.9	2.45	0.9	2.45	
			6 V	1.2	2	3.2	1.2	3.2	1.2	3.2	
$V_{T+} - V_{T-}$			2 V	0.2	0.6	1.2	0.2	1.2	0.2	1.2	V
			4.5 V	0.4	0.9	2.1	0.4	2.1	0.4	2.1	
			6 V	0.5	1.3	2.5	0.5	2.5	0.5	2.5	
I_I	V_I = V_{CC} or 0		6 V			±0.1		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			2		40		20	μA
C_i			2 V to 6 V		3	10		10		10	pF

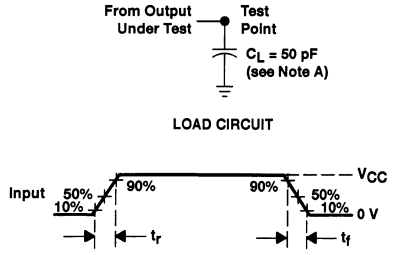
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC7001		SN74HC7001		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		60	130		195		163	ns
			4.5 V		18	26		39		33	
			6 V		14	22		33		28	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

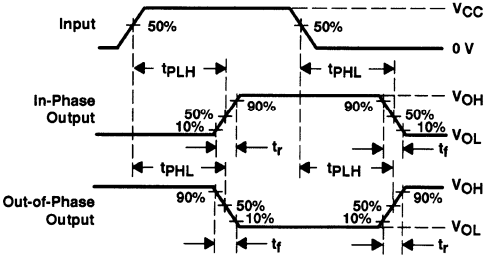
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	20	pF

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



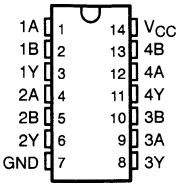
VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

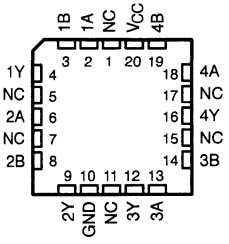
Figure 1. Load Circuit and Voltage Waveforms

- **Operation From Very Slow Input Transitions**
- **Temperature-Compensated Threshold Levels**
- **High Noise Immunity**
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC7002 . . . J OR W PACKAGE
SN74HC7002 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC7002 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

In these devices, each circuit functions as a quadruple NOR gate. They perform the Boolean function $Y = \overline{A} \bullet \overline{B}$ or $Y = \overline{A + B}$ in positive logic. However, because of the Schmitt action, the inputs have different input threshold levels for positive- and negative-going signals.

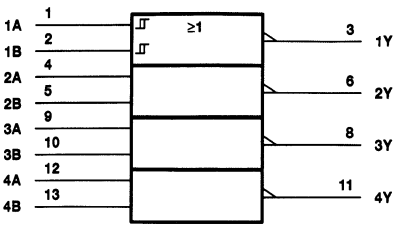
These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

The SN54HC7002 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC7002 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

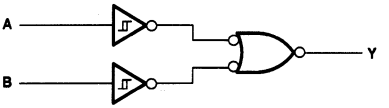
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC7002			SN74HC7002			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC7002		SN74HC7002		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
V_{T+}			2 V	0.7	1.2	1.5	0.7	1.5	0.7	1.5	V
			4.5 V	1.55	2.5	3.15	1.55	3.15	1.55	3.15	
			6 V	2.1	3.3	4.2	2.1	4.2	2.1	4.2	
V_{T-}			2 V	0.3	0.6	1	0.3	1	0.3	1	V
			4.5 V	0.9	1.6	2.45	0.9	2.45	0.9	2.45	
			6 V	1.2	2	3.2	1.2	3.2	1.2	3.2	
$V_{T+} - V_{T-}$			2 V	0.2	0.6	1.2	0.2	1.2	0.2	1.2	V
			4.5 V	0.4	0.9	2.1	0.4	2.1	0.4	2.1	
			6 V	0.5	1.3	2.5	0.5	2.5	0.5	2.5	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0		6 V			2		40		20	μA
C_i			2 V to 6 V		3	10		10		10	pF

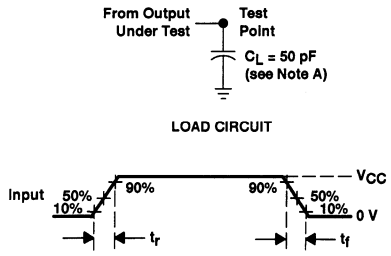
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC7002		SN74HC7002		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		60	130		195		163	ns
			4.5 V		18	26		39		33	
			6 V		14	22		33		28	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

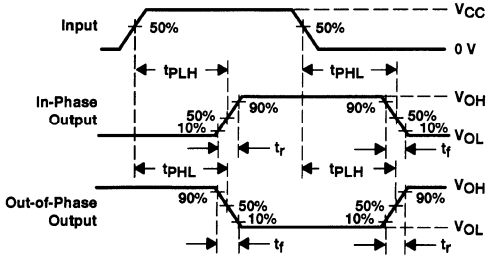
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	20	pF

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



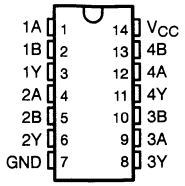
VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

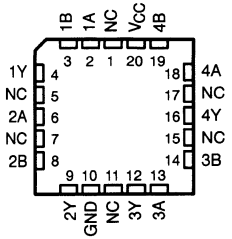
Figure 1. Load Circuit and Voltage Waveforms

- **Operation From Very Slow Input Transitions**
- **Temperature-Compensated Threshold Levels**
- **High Noise Immunity**
- **Same Pinouts as 'HC32**
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC7032 . . . J OR W PACKAGE
SN74HC7032 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC7032 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

In these devices, each circuit functions as a quadruple OR gate. They perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = A + B$ in positive logic. However, because of the Schmitt action, the inputs have different input threshold levels for positive- and negative-going signals.

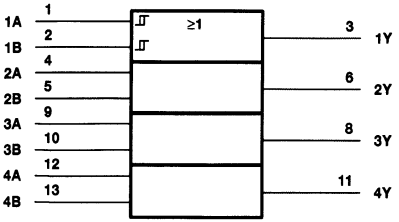
These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

The SN54HC7032 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC7032 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

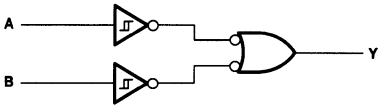
INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ..... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): D package ..... 1.25 W
N package ..... 1.1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

			SN54HC7032			SN74HC7032			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC7032		SN74HC7032		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
V_{T+}			2 V	0.7	1.2	1.5	0.7	1.5	0.7	1.5	V
			4.5 V	1.55	2.5	3.15	1.55	3.15	1.55	3.15	
			6 V	2.1	3.3	4.2	2.1	4.2	2.1	4.2	
V_{T-}			2 V	0.3	0.6	1	0.3	1	0.3	1	V
			4.5 V	0.9	1.6	2.45	0.9	2.45	0.9	2.45	
			6 V	1.2	2	3.2	1.2	3.2	1.2	3.2	
$V_{T+} - V_{T-}$			2 V	0.2	0.6	1.2	0.2	1.2	0.2	1.2	V
			4.5 V	0.4	0.9	2.1	0.4	2.1	0.4	2.1	
			6 V	0.5	1.3	2.5	0.5	2.5	0.5	2.5	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			2		40		20	μA
C_i			2 V to 6 V		3	10		10		10	pF

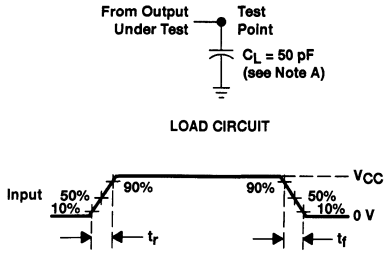
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC7032		SN74HC7032		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		60	130		195		163	ns
			4.5 V		18	26		39		33	
			6 V		14	22		33		28	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

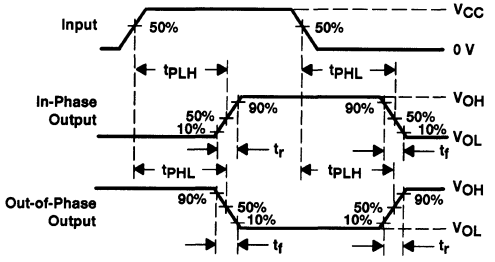
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	20	pF

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

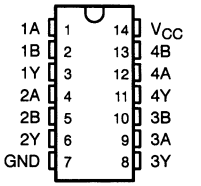
Figure 1. Load Circuit and Voltage Waveforms

Contents

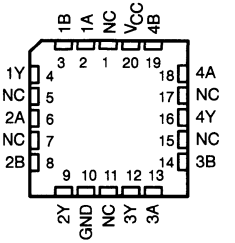
SCLS182C – FEBRUARY 1993 – REVISED APRIL 1996

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process**
- **Typical V_{OLP} (Output Ground Bounce)< 0.8 V at V_{CC}, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC}, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Flat (W) Packages, Chip Carriers (FK), and (J) 300-mil DIPs**

SN54LV00 . . . J OR W PACKAGE
SN74LV00 . . . D, DB, OR PW PACKAGE
(TOP VIEW)



SN54LV00 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These quadruple 2-input positive-NAND gates are designed for 2.7-V to 5.5-V V_{CC} operation.

The 'LV00 perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN74LV00 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

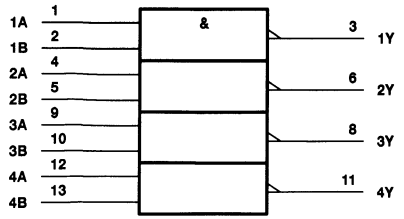
The SN54LV00 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV00 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

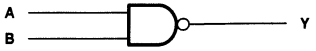
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, DB, J, PW, and W packages.

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 4)

			SN54LV00		SN74LV00		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	5.5	2.7	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		2		V
		V_{CC} = 4.5 V to 5.5 V	3.15		3.15		
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8		0.8	V
		V_{CC} = 4.5 V to 5.5 V		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V to 3.6 V		–6		–6	mA
		V_{CC} = 4.5 V to 5.5 V		–12		–12	
I_{OL}	Low-level output current	V_{CC} = 2.7 V to 3.6 V		6		6	mA
		V_{CC} = 4.5 V to 5.5 V		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	100	0	100	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	SN54LV00			SN74LV00			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = –100 μA		MIN to MAX	V_{CC} – 0.2			V_{CC} – 0.2			V
	I_{OH} = –6 mA		3 V	2.4			2.4			
	I_{OH} = –12 mA		4.5 V	3.6			3.6			
V_{OL}	I_{OL} = 100 μA		MIN to MAX			0.2			0.2	V
	I_{OL} = 6 mA		3 V			0.4			0.4	
	I_{OL} = 12 mA		4.5 V			0.55			0.55	
I_I	V_I = V_{CC} or GND		3.6 V			±1			±1	μA
			5.5 V			±1			±1	
I_{CC}	V_I = V_{CC} or GND	I_O = 0	3.6 V			20			20	μA
			5.5 V			20			20	
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		3 V to 3.6 V			500			500	μA
C_i	V_I = V_{CC} or GND		3.3 V		2.5			2.5		pF
			5 V		1.5			1.5		

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LV00								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y		6	11		9	15		18	ns

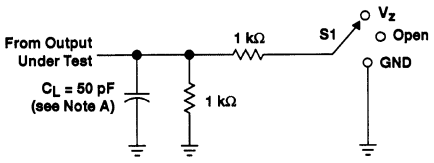
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LV00								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y		6	11		9	15		18	ns

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 10 MHz	3.3 V	23	pF
			5 V	23	

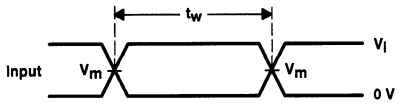
PARAMETER MEASUREMENT INFORMATION



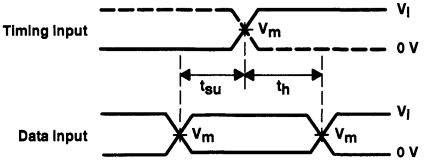
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_z
t_{PHZ}/t_{PZH}	GND

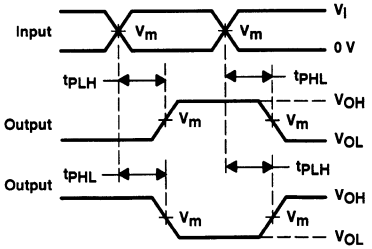
WAVEFORM CONDITION	V_{CC} = 4.5 V to 5.5 V	V_{CC} = 2.7 V to 3.6 V
V_m	0.5 × V_{CC}	1.5 V
V_I	V_{CC}	2.7 V
V_z	2 × V_{CC}	6 V



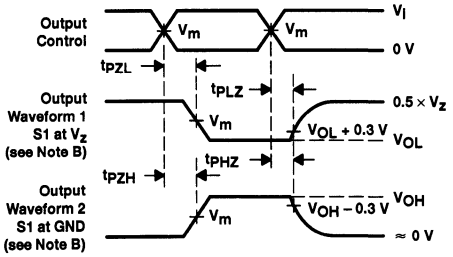
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

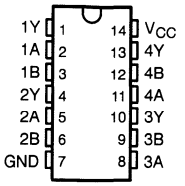
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

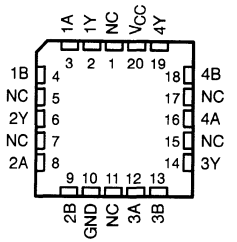
SCLS183B – FEBRUARY 1993 – REVISED APRIL 1996

- *EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC}, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC}, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) 300-mil DIPs

SN54LV02 . . . J OR W PACKAGE
SN74LV02 . . . D, DB, OR PW PACKAGE
(TOP VIEW)



SN54LV02 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These quadruple 2-input positive-NOR gates are designed for 2.7-V to 5.5-V V_{CC} operation.

The 'LV02 perform Boolean function $Y = \overline{A + B}$ or $Y = \overline{A} \bullet \overline{B}$ in positive logic.

The SN74LV02 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

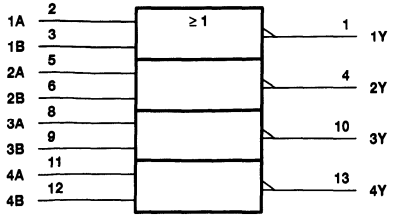
The SN54LV02 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV02 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, PW, and W packages.

logic diagram, each gate (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 4)

			SN54LV02		SN74LV02		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	5.5	2.7	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		2		V
		V_{CC} = 4.5 V to 5.5 V	3.15		3.15		
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8		0.8	V
		V_{CC} = 4.5 V to 5.5 V		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V to 3.6 V		–6		–6	mA
		V_{CC} = 4.5 V to 5.5 V		–12		–12	
I_{OL}	Low-level output current	V_{CC} = 2.7 V to 3.6 V		6		6	mA
		V_{CC} = 4.5 V to 5.5 V		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	100	0	100	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}†	SN54LV02			SN74LV02			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = –100 μA	MIN to MAX	V_{CC} – 0.2			V_{CC} – 0.2			V
	I_{OH} = –6 mA	3 V	2.4			2.4			
	I_{OH} = –12 mA	4.5 V	3.6			3.6			
V_{OL}	I_{OL} = 100 μA	MIN to MAX			0.2			0.2	V
	I_{OL} = 6 mA	3 V			0.4			0.4	
	I_{OL} = 12 mA	4.5 V			0.55			0.55	
I_I	V_I = V_{CC} or GND	3.6 V			±1			±1	μA
		5.5 V			±1			±1	
I_{CC}	V_I = V_{CC} or GND, I_O = 0	3.6 V			20			20	μA
		5.5 V			20			20	
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			500			500	μA
C_i	V_I = V_{CC} or GND	3.3 V		2.5			2.5		pF
		5 V		2.5			2.5		

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LV02									UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	A	Y		5	10		8	13			16	ns

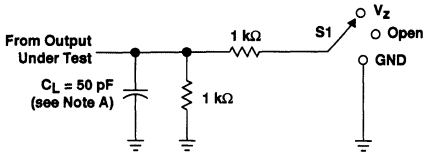
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LV02								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y		5	10		8	13		16	ns

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 10 MHz	3.3 V	16	pF
			5 V	20	

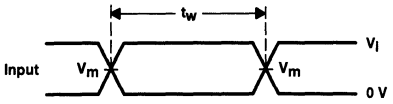
PARAMETER MEASUREMENT INFORMATION



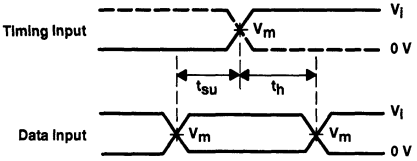
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_Z
t_{PHZ}/t_{PZH}	GND

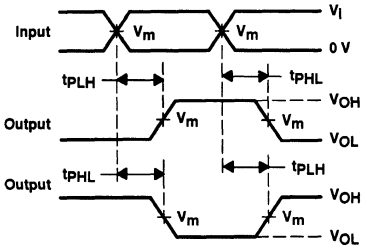
WAVEFORM CONDITION	V_{CC} = 4.5 V to 5.5 V	V_{CC} = 2.7 V to 3.6 V
V_m	0.5 × V_{CC}	1.5 V
V_I	V_{CC}	2.7 V
V_Z	2 × V_{CC}	6 V



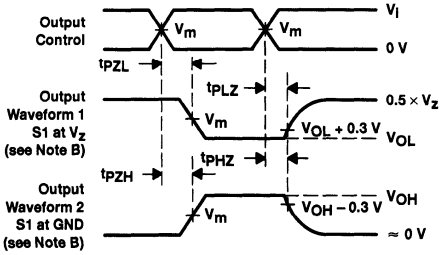
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

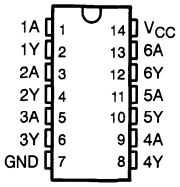
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

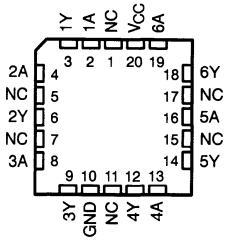
SCLS184C – FEBRUARY 1993 – REVISED APRIL 1996

- *EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC}, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC}, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) 300-mil DIPs

SN54LV04 . . . J OR W PACKAGE
SN74LV04 . . . D, DB, OR PW PACKAGE
(TOP VIEW)



SN54LV04 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These hex inverters are designed for 2.7-V to 5.5-V V_{CC} operation.

The 'LV04 contain six independent inverters. These devices perform the Boolean function $Y = \overline{A}$.

The SN74LV04 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

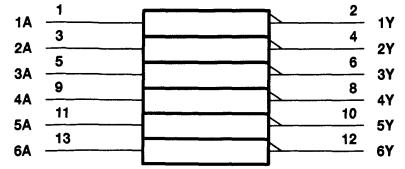
The SN54LV04 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LV04 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, DB, J, PW, and W packages.

logic diagram, each inverter (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 4)

			SN54LV04		SN74LV04		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	5.5	2.7	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		2		V
		V_{CC} = 4.5 V to 5.5 V	3.15		3.15		
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8		0.8	V
		V_{CC} = 4.5 V to 5.5 V		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V to 3.6 V		−6		−6	mA
		V_{CC} = 4.5 V to 5.5 V		−12		−12	
I_{OL}	Low-level output current	V_{CC} = 2.7 V to 3.6 V		6		6	mA
		V_{CC} = 4.5 V to 5.5 V		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	100	0	100	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}†	SN54LV04			SN74LV04			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = –100 μA	MIN to MAX	V_{CC}–0.2			V_{CC}–0.2			V
	I_{OH} = –6 mA	3 V	2.4			2.4			
	I_{OH} = –12 mA	4.5 V	3.6			3.6			
V_{OL}	I_{OL} = 100 μA	MIN to MAX			0.2			0.2	V
	I_{OL} = 6 mA	3 V			0.4			0.4	
	I_{OL} = 12 mA	4.5 V			0.55			0.55	
I_I	V_I = V_{CC} or GND	3.6 V			±1			±1	μA
		5.5 V			±1			±1	
I_{CC}	V_I = V_{CC} or GND I_O = 0	3.6 V			20			20	μA
		5.5 V			20			20	
ΔI_{CC}	One input at V_{CC} – 0.6 V Other inputs at V_{CC} or GND	3 V to 3.6 V			500			500	μA
C_i	V_I = V_{CC} or GND	3.3 V		2.5			2.5		pF
		5 V		1.8			1.8		

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LV04								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y		4	9		6	12		15	ns

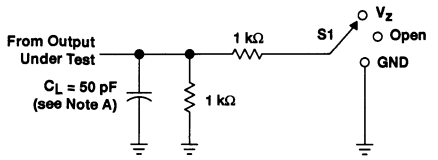
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LV04								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y		4	9		6	12		15	ns

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance per inverter	C_L = 50 pF, f = 10 MHz	3.3 V	18	pF
			5 V	26	

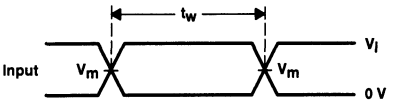
PARAMETER MEASUREMENT INFORMATION



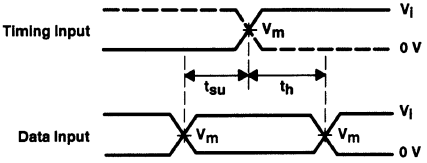
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_Z
t_{PHZ}/t_{PZH}	GND

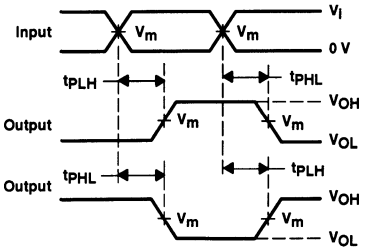
WAVEFORM CONDITION	V_{CC} = 4.5 V to 5.5 V	V_{CC} = 2.7 V to 3.6 V
V_m	$0.5 \times V_{CC}$	1.5 V
V_I	V_{CC}	2.7 V
V_Z	$2 \times V_{CC}$	6 V



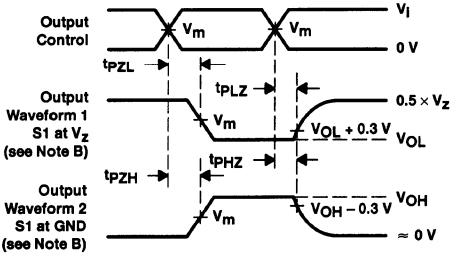
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

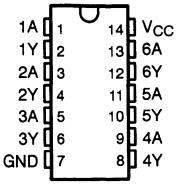
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

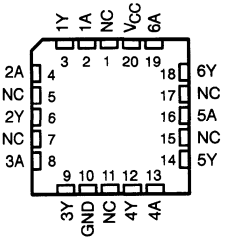
SCLS185B – FEBRUARY 1993 – REVISED APRIL 1996

- *EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC}, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC}, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) 300-mil DIPs

SN54LVU04 . . . J OR W PACKAGE
SN74LVU04 . . . D, DB, OR PW PACKAGE
(TOP VIEW)



SN54LVU04 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These hex inverters are designed for 2.7-V to 5.5-V V_{CC} operation.

The 'LVU04 contain six independent inverters with unbuffered outputs. These devices perform the Boolean function $Y = \overline{A}$.

The SN74LVU04 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVU04 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVU04 is characterized for operation from −40°C to 85°C.

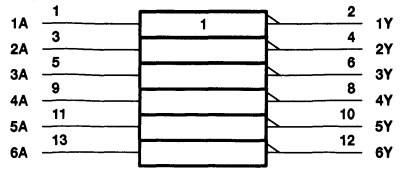
FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

EPIC is a trademark of Texas Instruments Incorporated.

SCLS185B – FEBRUARY 1993 – REVISED APRIL 1996

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, DB, J, PW and W packages.

logic diagram, each inverter (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 4)

			SN54LVU04		SN74LVU04		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	5.5	2.7	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2.4		2.4		V
		V_{CC} = 4.5 V to 5.5 V	3.55		3.55		
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.5		0.5	V
		V_{CC} = 4.5 V to 5.5 V		0.8		0.8	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V to 3.6 V		−6		−6	mA
		V_{CC} = 4.5 V to 5.5 V		−12		−12	
I_{OL}	Low-level output current	V_{CC} = 2.7 V to 3.6 V		6		6	mA
		V_{CC} = 4.5 V to 5.5 V		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	100	0	100	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	SN54LVU04			SN74LVU04			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	$V_I = V_{IL}$,	$I_{OH} = -100\ \mu A$	MIN to MAX	$V_{CC}-0.5$			$V_{CC}-0.5$			V
	V_I = GND,	$I_{OH} = -6$ mA	3 V	2.4			2.4			
	V_I = GND,	$I_{OH} = -12$ mA	4.5 V	3.6			3.6			
V_{OL}	$V_I = V_{IH}$,	$I_{OL} = 100\ \mu A$	MIN to MAX			0.5			0.5	V
	$V_I = V_{CC}$,	$I_{OL} = 6$ mA	3 V			0.4			0.4	
	$V_I = V_{CC}$,	$I_{OL} = 12$ mA	4.5 V			0.55			0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V			±1			±1	µA
			5.5 V			±1			±1	
I_{CC}	$V_I = V_{CC}$ or GND,	$I_O = 0$	3.6 V			20			20	µA
			5.5 V			20			20	
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		3 V to 3.6 V			500			500	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V		7			7		pF
			5 V		7.5			7.5		

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVU04								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y		5	10		8	13		13	ns

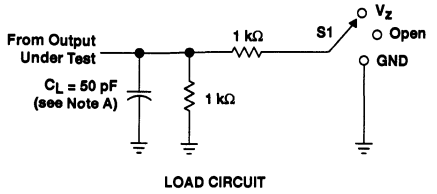
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVU04								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y		5	10		8	13		13	ns

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance per inverter	C_L = 50 pF, f = 10 MHz	3.3 V	7	pF
			5 V	12	

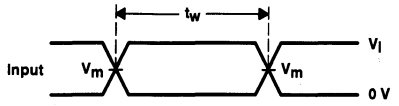
PARAMETER MEASUREMENT INFORMATION



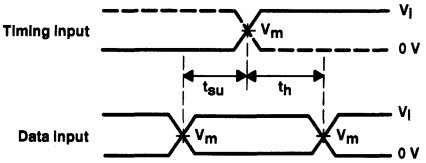
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_Z
t_{PHZ}/t_{PZH}	GND

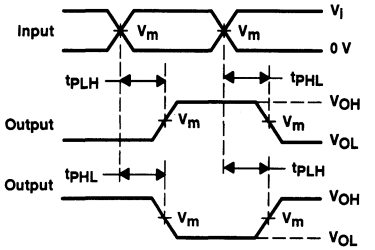
WAVEFORM CONDITION	V_{CC} = 4.5 V to 5.5 V	V_{CC} = 2.7 V to 3.6 V
V_m	0.5 × V_{CC}	1.5 V
V_I	V_{CC}	2.7 V
V_Z	2 × V_{CC}	6 V



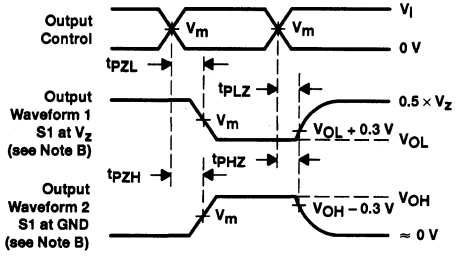
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

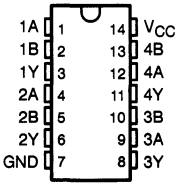
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

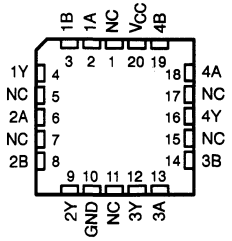
SCLS186C – FEBRUARY 1993 – REVISED APRIL 1996

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC}, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC}, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) 300-mil DIPs**

SN54LV08 . . . J OR W PACKAGE
SN74LV08 . . . D, DB, OR PW PACKAGE
(TOP VIEW)



SN54LV08 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These quadruple 2-input positive-AND gates are designed for 2.7-V to 5.5-V V_{CC} operation.

The 'LV08 perform Boolean function $Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

The SN74LV08 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

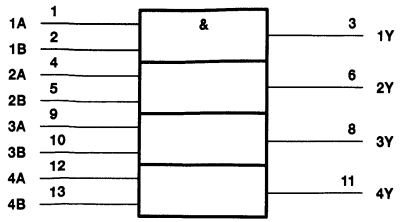
The SN54LV08 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV08 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

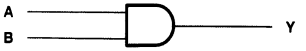
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, DB, J, PW, and W packages.

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): D package ..... 1.25 W
DB or DW package ..... 0.5 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 4)

			SN54LV08		SN74LV08		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	5.5	2.7	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		2		V
		V_{CC} = 4.5 V to 5.5 V	3.15		3.15		
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8		0.8	V
		V_{CC} = 4.5 V to 5.5 V		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V to 3.6 V		–6		–6	mA
		V_{CC} = 4.5 V to 5.5 V		–12		–12	
I_{OL}	Low-level output current	V_{CC} = 2.7 V to 3.6 V		6		6	mA
		V_{CC} = 4.5 V to 5.5 V		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	100	0	100	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	SN54LV08			SN74LV08			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2			V_{CC}–0.2			V
	I_{OH} = –6 mA		3 V	2.4			2.4			
	I_{OH} = –12 mA		4.5 V	3.6			3.6			
V_{OL}	I_{OL} = 100 µA		MIN to MAX			0.2			0.2	V
	I_{OL} = 6 mA		3 V			0.4			0.4	
	I_{OL} = 12 mA		4.5 V			0.55			0.55	
I_I	V_I = V_{CC} or GND		3.6 V			±1			±1	µA
			5.5 V			±1			±1	
I_{CC}	V_I = V_{CC} or GND	I_O = 0	3.6 V			20			20	µA
			5.5 V			20			20	
ΔI_{CC}	One input at V_{CC} – 0.6 V	Other inputs at V_{CC} or GND	3 V to 3.6 V			500			500	µA
C_i	V_I = V_{CC} or GND		3.3 V		2.5			2.5		pF
			5 V		2.6			2.6		

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LV08								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y		7	11		10	15		17	ns

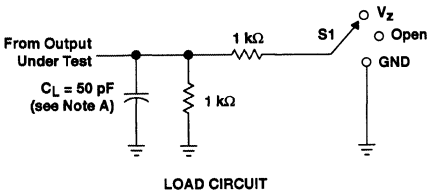
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LV08								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y		7	11		10	15		17	ns

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 10 MHz	3.3 V	24	pF
			5 V	29	

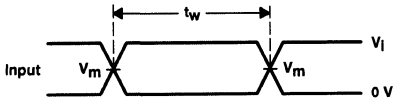
PARAMETER MEASUREMENT INFORMATION



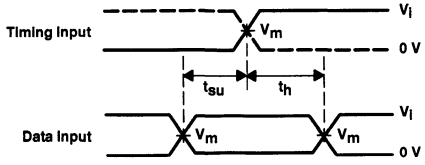
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_Z
t_{PHZ}/t_{PZH}	GND

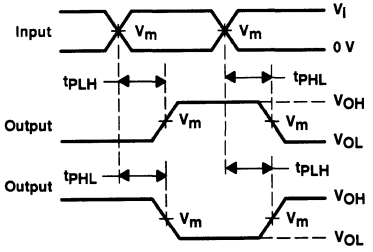
WAVEFORM CONDITION	V_{CC} = 4.5 V to 5.5 V	V_{CC} = 2.7 V to 3.6 V
V_m	$0.5 \times V_{CC}$	1.5 V
V_I	V_{CC}	2.7 V
V_Z	$2 \times V_{CC}$	6 V



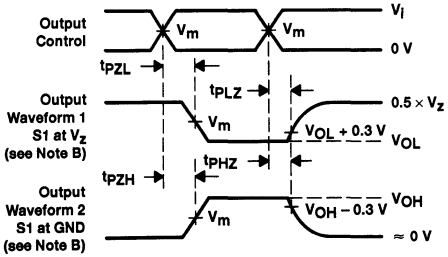
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



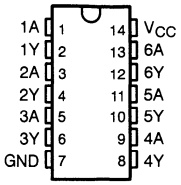
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

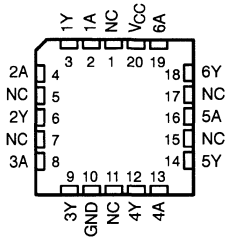
Figure 1. Load Circuit and Voltage Waveforms

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC}, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC}, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Flat (W) Packages, Chip Carriers (FK), and (J) 300-mil DIPs**

SN54LV14 . . . J OR W PACKAGE
SN74LV14 . . . D, DB, OR PW PACKAGE
(TOP VIEW)



SN54LV14 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These hex Schmitt-trigger inverters are designed for 2.7-V to 5.5-V V_{CC} operation.

The 'LV14 contain six independent inverters. These devices perform the Boolean function $Y = \overline{A}$.

The SN74LV14 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

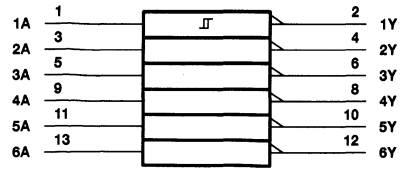
The SN54LV14 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV14 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

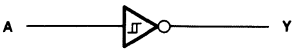
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, DB, J, PW, and W packages.

logic diagram, each inverter (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 4)

			SN54LV14		SN74LV14		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	5.5	2.7	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2.4		2.4		V
		V_{CC} = 4.5 V to 5.5 V	3.55		3.55		
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.4		0.4	V
		V_{CC} = 4.5 V to 5.5 V		1.25		1.25	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V to 3.6 V		–6		–6	mA
		V_{CC} = 4.5 V to 5.5 V		–12		–12	
I_{OL}	Low-level output current	V_{CC} = 2.7 V to 3.6 V		6		6	mA
		V_{CC} = 4.5 V to 5.5 V		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	100	0	100	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}†	SN54LV14			SN74LV14			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{T+} Positive-going threshold		2.7 V	1		2	1		2	V
		3 V	1.2		2.2	1.2		2.2	
		3.6 V	1.5		2.4	1.5		2.4	
		4.5 V	1.7		3.2	1.7		3.2	
		5.5 V	2.1		3.9	2.1		3.9	
V_{T-} Negative-going threshold		2.7 V	0.4		1.4	0.4		1.4	V
		3 V	0.6		1.5	0.6		1.5	
		3.6 V	0.8		1.8	0.8		1.8	
		4.5 V	0.9		2.25	0.9		2.25	
		5.5 V	1.1		2.75	1.1		2.75	
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)		2.7 V	0.3		1.1	0.3		1.1	V
		3 V	0.4		1.2	0.4		1.2	
		3.6 V	0.4		1.2	0.4		1.2	
		4.5 V	0.4		1.4	0.4		1.4	
		5.5 V	0.5		1.5	0.5		1.5	
V_{OH}	I_{OH} = –100 µA	MIN to MAX	V_{CC} – 0.2			V_{CC} – 0.2			V
	I_{OH} = –6 mA	3 V	2.4			2.4			
	I_{OH} = –12 mA	4.5 V	3.6			3.6			
V_{OL}	I_{OL} = 100 µA	MIN to MAX			0.2			0.2	V
	I_{OL} = 6 mA	3 V			0.4			0.4	
	I_{OL} = 12 mA	4.5 V			0.55			0.55	
I_I	$V_I = V_{CC}$ or GND	3.6 V			±1			±1	µA
		5.5 V			±1			±1	
I_{CC}	VI = VCC or GND, I_O = 0	3.6 V			20			20	µA
		5.5 V			20			20	
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			500			500	µA
C_i	$V_I = V_{CC}$ or GND	3.3 V		2.5			2.5		pF
		5 V		3			3		

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LV14								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y		8	18		12	22		25	ns

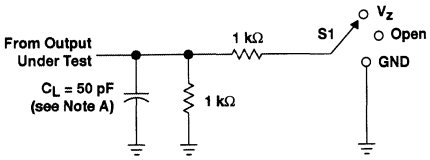
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LV14								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y		8	18		12	22		25	ns

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance per inverter	C_L = 50 pF, f = 10 MHz	3.3 V	22	pF
			5 V	24	

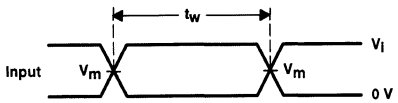
PARAMETER MEASUREMENT INFORMATION



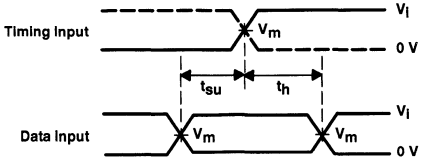
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_z
t_{PHZ}/t_{PZH}	GND

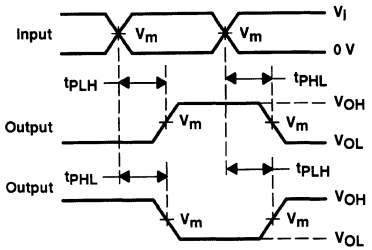
WAVEFORM CONDITION	V_{CC} = 4.5 V to 5.5 V	V_{CC} = 2.7 V to 3.6 V
V_m	0.5 × V_{CC}	1.5 V
V_I	V_{CC}	2.7 V
V_z	2 × V_{CC}	6 V



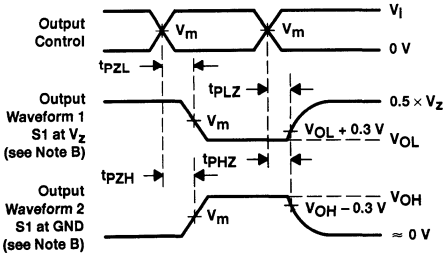
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

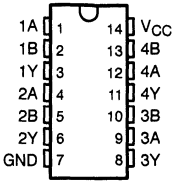
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

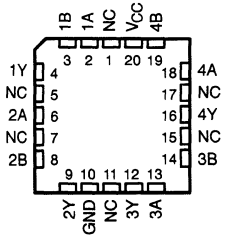
SCLS188C – FEBRUARY 1993 – REVISED APRIL 1996

- *EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC}, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC}, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Flat (W) Packages, Chip Carriers (FK), and (J) 300-mil DIPs

SN54LV32 . . . J OR W PACKAGE
SN74LV32 . . . D, DB, OR PW PACKAGE
(TOP VIEW)



SN54LV32 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These quadruple 2-input positive-OR gates are designed for 2.7-V to 5.5-V V_{CC} operation.

The 'LV32 perform the Boolean function $Y = A + B$ or $Y = \overline{\overline{A} \cdot \overline{B}}$ in positive logic.

The SN74LV32 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

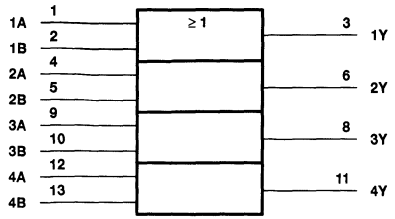
The SN54LV32 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV32 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, DB, J, PW, and W packages.

logic diagram, each gate (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 4)

			SN54LV32		SN74LV32		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	5.5	2.7	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		2		V
		V_{CC} = 4.5 V to 5.5 V	3.15		3.15		
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8		0.8	V
		V_{CC} = 4.5 V to 5.5 V		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V to 3.6 V		–6		–6	mA
		V_{CC} = 4.5 V to 5.5 V		–12		–12	
I_{OL}	Low-level output current	V_{CC} = 2.7 V to 3.6 V		6		6	mA
		V_{CC} = 4.5 V to 5.5 V		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	100	0	100	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	SN54LV32			SN74LV32			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = –100 μA		MIN to MAX	V_{CC}–0.2			V_{CC}–0.2			V
	I_{OH} = –6 mA		3 V	2.4			2.4			
	I_{OH} = –12 mA		4.5 V	3.6			3.6			
V_{OL}	I_{OL} = 100 μA		MIN to MAX			0.2			0.2	V
	I_{OL} = 6 mA		3 V			0.4			0.4	
	I_{OL} = 12 mA		4.5 V			0.55			0.55	
I_I	V_I = V_{CC} or GND		3.6 V			±1			±1	μA
			5.5 V			±1			±1	
I_{CC}	V_I = V_{CC} or GND	I_O = 0	3.6 V			20			20	μA
			5.5 V			20			20	
ΔI_{CC}	One input at V_{CC} – 0.6 V	One input at V_{CC} – 0.6 V	3 V to 3.6 V			500			500	μA
C_i	V_I = V_{CC} or GND		3.3 V		2.5			2.5		pF
			5 V		2			2		

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LV32									UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	A	Y		6	10		9	13			16	ns

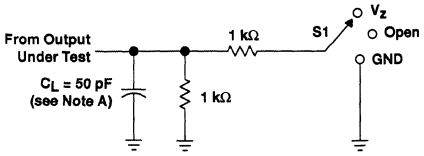
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LV32								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y		6	10		9	13		16	ns

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 10 MHz	3.3 V	23	pF
			5 V	27	

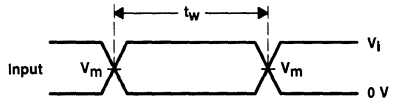
PARAMETER MEASUREMENT INFORMATION



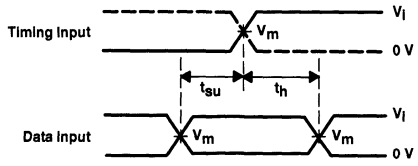
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_z
t_{PHZ}/t_{PZH}	GND

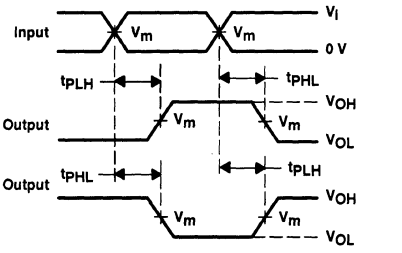
WAVEFORM CONDITION	V_{CC} = 4.5 V to 5.5 V	V_{CC} = 2.7 V to 3.6 V
V_m	0.5 × V_{CC}	1.5 V
V_I	V_{CC}	2.7 V
V_z	2 × V_{CC}	6 V



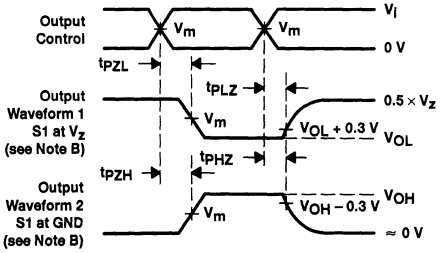
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

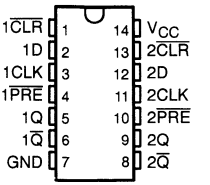
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

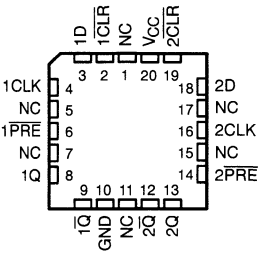
SCLS189C – FEBRUARY 1993 – REVISED APRIL 1996

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC}, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC}, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Flat (W) Packages, Chip Carriers (FK), and (J) 300-mil DIPs**

SN54LV74 . . . J OR W PACKAGE
SN74LV74 . . . D, DP, OR PW PACKAGE
(TOP VIEW)



SN54LV74 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These dual positive-edge-triggered D-type flip-flops are designed for 2.7-V to 5.5-V V_{CC} operation.

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) inputs meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The SN74LV74 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LV74 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV74 is characterized for operation from –40°C to 85°C.

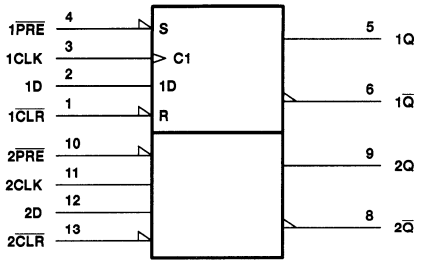
EPIC is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

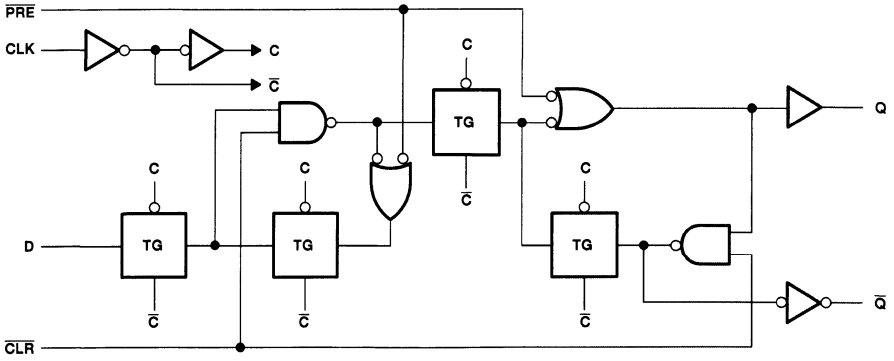
† This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, DB, J, PW, and W packages.

logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 4)

			SN54LV74		SN74LV74		UNIT
			MIN	MAX	MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	5.5	2.7	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		2		V
		V_{CC} = 4.5 V to 5.5 V	3.15		3.15		
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8		0.8	V
		V_{CC} = 4.5 V to 5.5 V		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V to 3.6 V		–6		–6	mA
		V_{CC} = 4.5 V to 5.5 V		–12		–12	
I_{OL}	Low-level output current	V_{CC} = 2.7 V to 3.6 V		6		6	mA
		V_{CC} = 4.5 V to 5.5 V		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	100	0	100	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	SN54LV74			SN74LV74			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = –100 μA		MIN to MAX	V_{CC} – 0.2			V_{CC} – 0.2			V
	I_{OH} = –6 mA		3 V	2.4			2.4			
	I_{OH} = –12 mA		4.5 V	3.6			3.6			
V_{OL}	I_{OL} = 100 μA		MIN to MAX			0.2			0.2	V
	I_{OL} = 6 mA		3 V			0.4			0.4	
	I_{OL} = 12 mA		4.5 V			0.55			0.55	
I_I	V_I = V_{CC} or GND		3.6 V			±1			±1	μA
			5.5 V			±1			±1	
I_{CC}	V_I = V_{CC} or GND	I_O = 0	3.6 V			20			20	μA
			5.5 V			20			20	
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		3 V to 3.6 V			500			500	μA
C_i	V_I = V_{CC} or GND		3.3 V		2.5			2.5		pF
			5 V		3			3		

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			SN54LV74						UNIT
			V_{CC} = 5 V ± 0.5 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	70	0	60	0	50	ns
t_w	Pulse duration, LE high	$\overline{PRE}$ or CLR low	15		20		25		ns
		CLK high or low	15		20		25		
t_{su}	Setup time, data before CLK↑	Data	6		8		12		ns
		$\overline{PRE}$ or CLR inactive	5		6		8		
t_h	Hold time, data after CLK↑		3		3		3		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			SN74LV74						UNIT
			V_{CC} = 5 V ± 0.5 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	70	0	60	0	50	ns
t_w	Pulse duration, LE high	$\overline{PRE}$ or CLR low	15		20		25		ns
		CLK high or low	15		20		25		
t_{su}	Setup time, data before CLK↑	Data	6		8		12		ns
		$\overline{PRE}$ or CLR inactive	5		6		8		
t_h	Hold time, data after CLK↑		3		3		3		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LV74								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
f_{max}			70	100		60	90		50		MHz
t_{pd}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$		11	19		18	27		34	ns
	CLK			10	17		17	26		28	

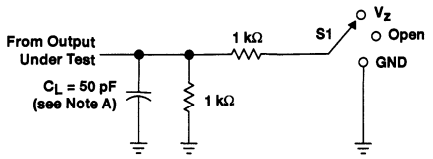
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LV74								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
f_{max}			70	100		60	90		50		MHz
t_{pd}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$		11	19		18	27		34	ns
	CLK			10	17		17	26		28	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	C_L = 50 pF, f = 10 MHz	3.3 V	32	pF
			5 V	68	

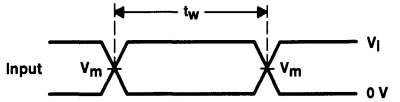
PARAMETER MEASUREMENT INFORMATION



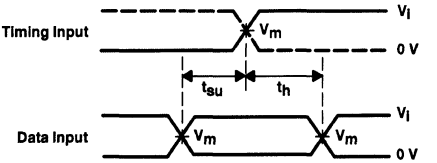
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_z
t_{PHZ}/t_{PZH}	GND

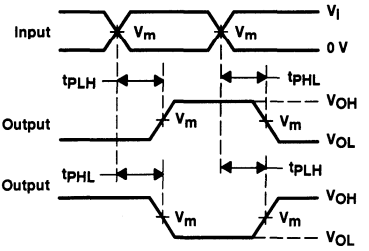
WAVEFORM CONDITION	V_{CC} = 4.5 V to 5.5 V	V_{CC} = 2.7 V to 3.6 V
V_m	0.5 × V_{CC}	1.5 V
V_I	V_{CC}	2.7 V
V_z	2 × V_{CC}	6 V



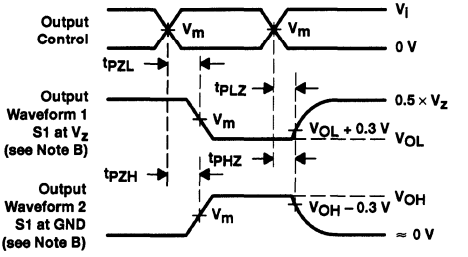
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



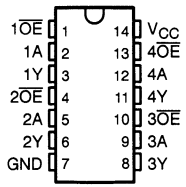
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

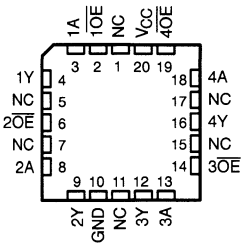
Figure 1. Load Circuit and Voltage Waveforms

- *EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC}, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC}, T_A = 25°C
- ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Flat (W) Packages, Chip Carriers (FK), and (J) 300-mil DIPs

SN54LV125 . . . J OR W PACKAGE
SN74LV125 . . . D, DB, OR PW PACKAGE
(TOP VIEW)



SN54LV125 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These quadruple bus buffer gates are designed for 2.7-V to 5.5-V V_{CC} operation.

The 'LV125 feature independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ($\overline{OE}$) input is high.

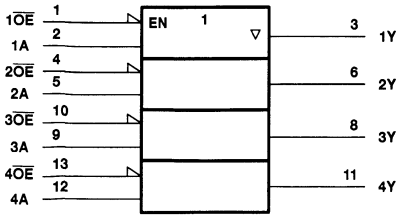
The SN54LV125 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV125 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

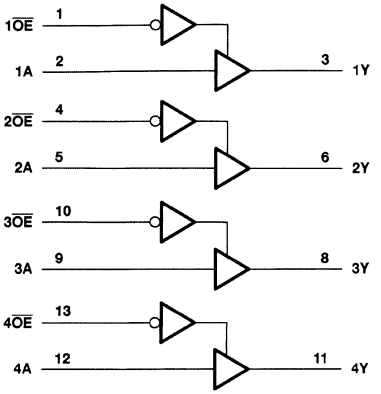
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, DB, J, PW, and W packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 4)

			SN54LV125		SN74LV125		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	5.5	2.7	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		2		V
		V_{CC} = 4.5 V to 5.5 V	3.15		3.15		
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8		0.8	V
		V_{CC} = 4.5 V to 5.5 V		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V to 3.6 V		−8		−8	mA
		V_{CC} = 4.5 V to 5.5 V		−16		−16	
I_{OL}	Low-level output current	V_{CC} = 2.7 V to 3.6 V		8		8	mA
		V_{CC} = 4.5 V to 5.5 V		16		16	
$\Delta t/\Delta V$	Input transition rise or fall rate		0	100	0	100	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}†	SN54LV125			SN74LV125			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	I_{OH} = −100 μA	MIN to MAX‡	V_{CC}−0.2			V_{CC}−0.2			V
	I_{OH} = −8 mA	3 V	2.4			2.4			
	I_{OH} = −16 mA	4.5 V	3.6			3.6			
V_{OL}	I_{OL} = 100 μA	MIN to MAX‡			0.2			0.2	V
	I_{OL} = 8 mA	3 V			0.4			0.4	
	I_{OL} = 16mA	4.5 V			0.55			0.55	
I_I	V_I = V_{CC} or GND	3.6 V			±1			±1	μA
		5.5 V			±1			±1	
I_{OZ}	V_O = V_{CC} or GND	3.6 V			±5			±5	μA
		5.5 V			±5			±5	
I_{CC}	V_I = V_{CC} or GND, I_O = 0	3.6 V			20			20	μA
		5.5 V			20			20	
ΔI_{CC}	One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			500			500	μA
C_i	V_I = V_{CC} or GND	3.3 V		3.5			3.5		pF
		5 V		3.5			3.5		
C_o	V_O = V_{CC} or GND	3.3 V		8			8		pF
		5 V		8			8		

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LV125								UNIT
			V_{CC} = 5.5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	MAX	
t_{pd}	A	Y		7	18		9	19		23	ns
t_{en}	$\overline{OE}$	Y		5	19		7	25		31	ns
t_{dis}	$\overline{OE}$	Y		7	17		9	23		28	ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

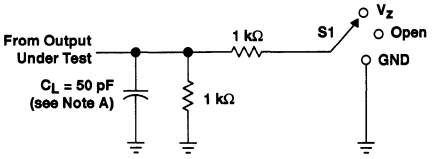
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LV125								UNIT
			V_{CC} = 5.5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	MAX	
t_{pd}	A	Y		7	18		9	19		23	ns
t_{en}	$\overline{OE}$	Y		5	19		7	25		31	ns
t_{dis}	$\overline{OE}$	Y		7	17		9	23		28	ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 10 MHz	3.3 V	45	pF
		Outputs disabled			5	
		Outputs enabled		5 V	48	pF
		Outputs disabled			5	

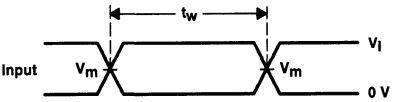
PARAMETER MEASUREMENT INFORMATION



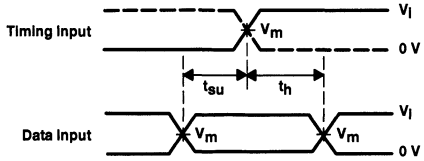
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_z
t_{PHZ}/t_{PZH}	GND

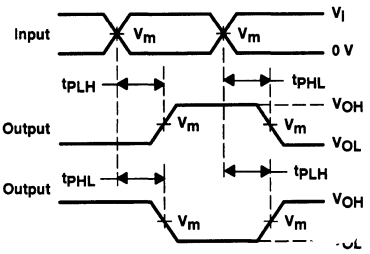
WAVEFORM CONDITION	V_{CC} = 4.5 V to 5.5 V	V_{CC} = 2.7 V to 3.6 V
V_m	0.5 × V_{CC}	1.5 V
V_I	V_{CC}	2.7 V
V_z	2 × V_{CC}	6 V



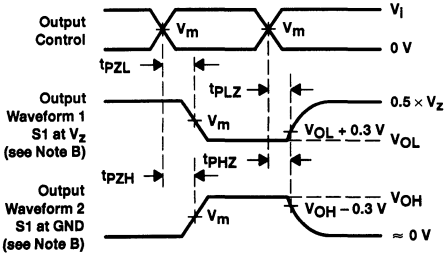
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

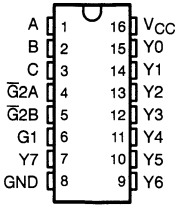
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

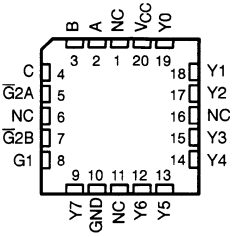
SCLS190D – FEBRUARY 1993 – REVISED JULY 1996

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC}, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC}, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Flat (W) Packages, Chip Carriers (FK), and (J) 300-mil DIPs**

SN54LV138 . . . J OR W PACKAGE
SN74LV138 . . . D, DB, OR PW PACKAGE
(TOP VIEW)



SN54LV138 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These 3-line to 8-line decoders/demultiplexers are designed for 2.7-V to 5.5-V V_{CC} operation.

The 'LV138 are designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN74LV138 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

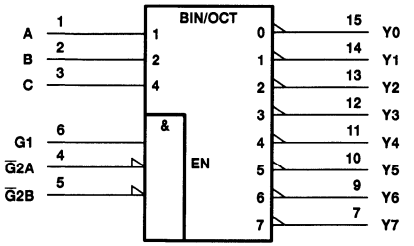
The SN54LV138 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV138 is characterized for operation from –40°C to 85°C.

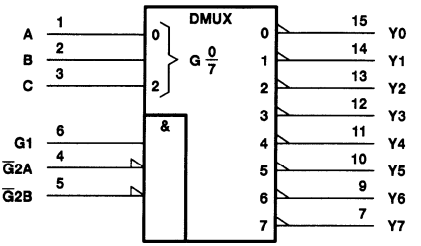
EPIC is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

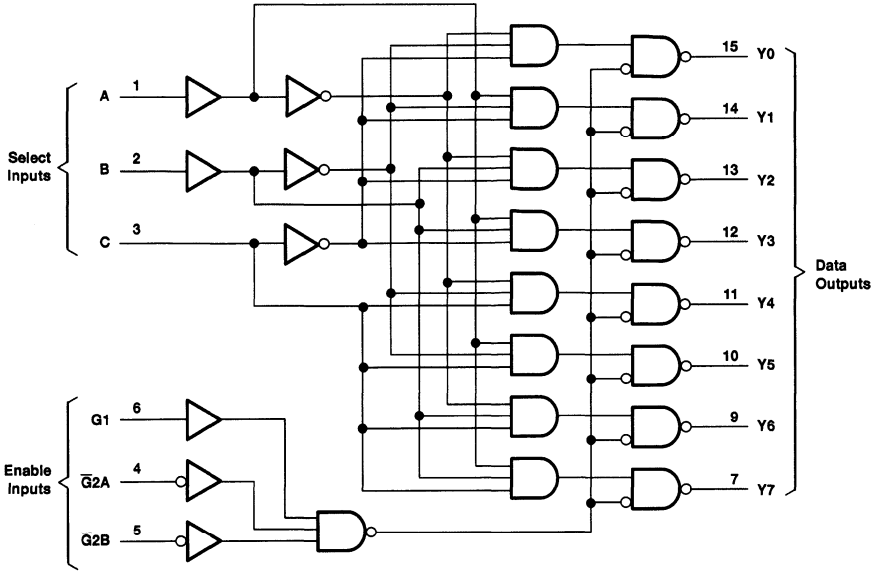
logic symbols (alternatives)†





† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, DB, J, PW, and W packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): D package ..... 1.3 W
DB package ..... 0.55 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 4)

			SN54LV138		SN74LV138		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	5.5	2.7	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		2		V
		V_{CC} = 4.5 V to 5.5 V	3.15		3.15		
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8		0.8	V
		V_{CC} = 4.5 V to 5.5 V		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V to 3.6 V		−6		−6	mA
		V_{CC} = 4.5 V to 5.5 V		−12		−12	
I_{OL}	Low-level output current	V_{CC} = 2.7 V to 3.6 V		6		6	mA
		V_{CC} = 4.5 V to 5.5 V		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	100	0	100	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	SN54LV138			SN74LV138			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = –100 μA		MIN to MAX	V_{CC}–0.2			V_{CC}–0.2			V
	I_{OH} = –6 mA		3 V	2.4			2.4			
	I_{OH} = –12 mA		4.5 V	3.6			3.6			
V_{OL}	I_{OL} = 100 μA		MIN to MAX			0.2			0.2	V
	I_{OL} = 6 mA		3 V			0.4			0.4	
	I_{OL} = 12 mA		4.5 V			0.55			0.55	
I_I	V_I = V_{CC} or GND		3.6 V			±1			±1	μA
			5.5 V			±1			±1	
I_{CC}	V_I = V_{CC} or GND	I_O = 0	3.6 V			20			20	μA
			5.5 V			20			20	
ΔI_{CC}	One input at V_{CC} – 0.6 V	Other inputs at V_{CC} or GND	3 V to 3.6 V			500			500	μA
C_i	V_I = V_{CC} or GND		3.3 V		2.5			2.5		pF
			5 V		2.1			2.1		

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LV138								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y		8	16		10	21		26	ns
	Enable			8	19		10	23		29	

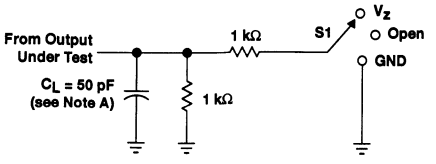
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LV138								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y		8	16		10	21		26	ns
	Enable			8	19		10	23		29	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance per channel	C_L = 50 pF, f = 10 MHz	3.3 V	47	pF
			5 V	49	

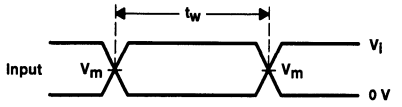
PARAMETER MEASUREMENT INFORMATION



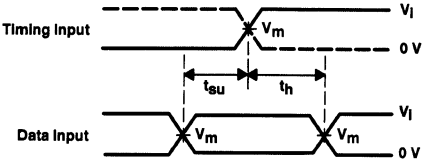
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_z
t_{PHZ}/t_{PZH}	GND

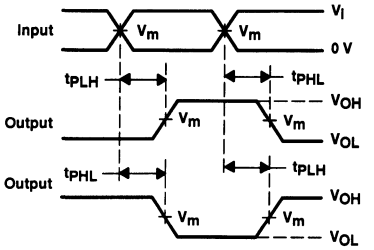
WAVEFORM CONDITION	V_{CC} = 4.5 V to 5.5 V	V_{CC} = 2.7 V to 3.6 V
V_m	0.5 × V_{CC}	1.5 V
V_I	V_{CC}	2.7 V
V_z	2 × V_{CC}	6 V



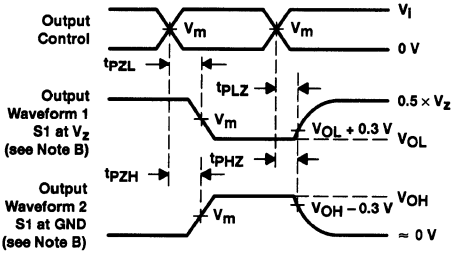
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

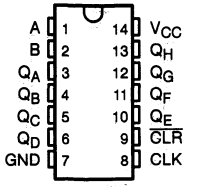
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

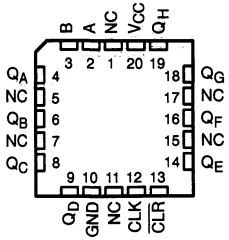
SCLS191B – FEBRUARY 1993 – REVISED APRIL 1996

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC}, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC}, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Flat (W) Packages, Chip Carriers (FK), and (J) 300-mil DIPs**

SN54LV164 . . . J OR W PACKAGE
SN74LV164 . . . D, DB, OR PW PACKAGE
(TOP VIEW)



SN54LV164 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These 8-bit parallel-out serial shift registers are designed for 2.7-V to 5.5-V V_{CC} operation.

The 'LV164 feature AND-gated serial (A and B) inputs and an asynchronous clear ($\overline{CLR}$) input. The gated serial inputs permit complete control over incoming data as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs can be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock (CLK) input.

The SN74LV164 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LV164 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV164 is characterized for operation from –40°C to 85°C.

EPIC is a trademark of Texas Instruments Incorporated.

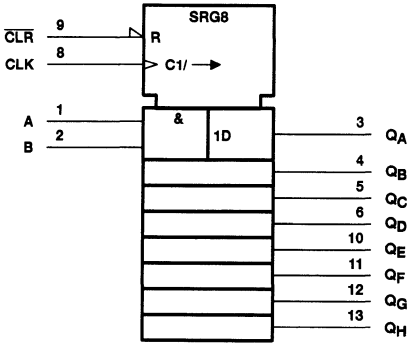
FUNCTION TABLE

INPUTS				OUTPUTS		
$\overline{CLR}$	CLK	A	B	Q_A	$Q_B \ldots Q_H$	
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state inputs conditions were established

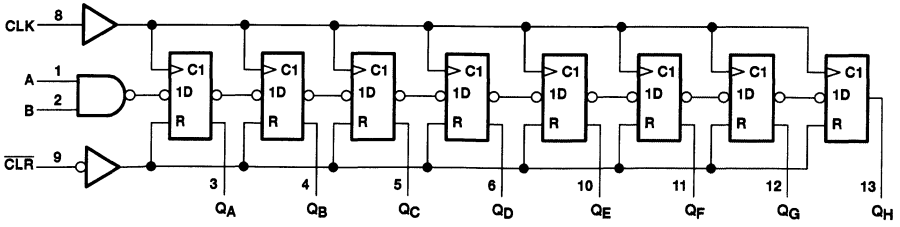
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most recent ↑ transition of the clock: indicates a 1-bit shift

logic symbol†

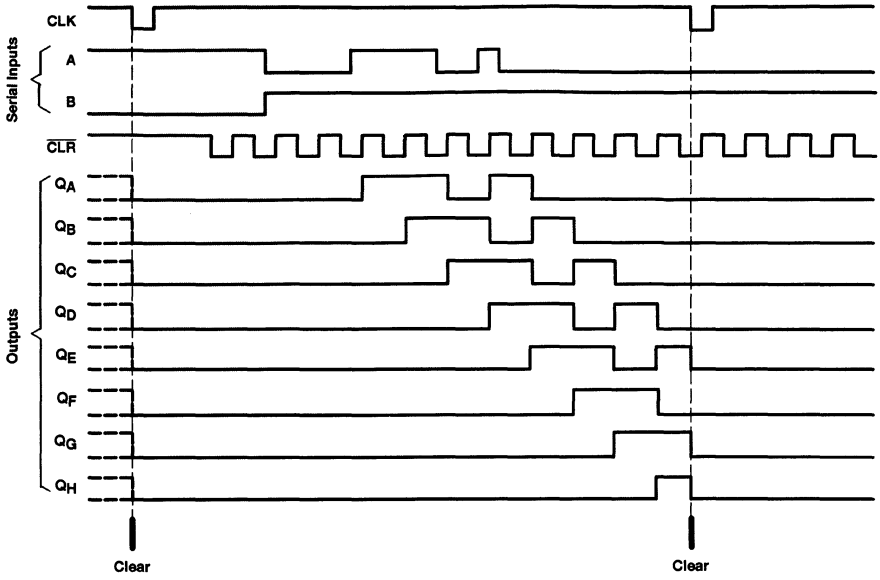


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, DB, J, PW, and W packages.

logic diagram (positive logic)



typical clear, shift, and clear sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): D package ..... 1.25 W
DB or PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 4)

			SN54LV164		SN74LV164		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	5.5	2.7	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		2		V
		V_{CC} = 4.5 V to 5.5 V	3.15		3.15		
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8		0.8	V
		V_{CC} = 4.5 V to 5.5 V		1.35		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V to 3.6 V		–6		–6	mA
		V_{CC} = 4.5 V to 5.5 V		–12		–12	
I_{OL}	Low-level output current	V_{CC} = 2.7 V to 3.6 V		6		6	mA
		V_{CC} = 4.5 V to 5.5 V		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	100	0	100	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}†	SN54LV164			SN74LV164			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = –100 µA	MIN to MAX	V_{CC} – 0.2			V_{CC} – 0.2			V
	I_{OH} = –6 mA	3 V	2.4			2.4			
	I_{OH} = –12 mA	4.5 V	3.6			3.6			
V_{OL}	I_{OL} = 100 µA	MIN to MAX			0.2			0.2	V
	I_{OL} = 6 mA	3 V			0.4			0.4	
	I_{OL} = 12 mA	4.5 V			0.55			0.55	
I_I	V_I = V_{CC} or GND	3.6 V			±1			±1	µA
		5.5 V			±1			±1	
I_{CC}	V_I = V_{CC} or GND, I_O = 0	3.6 V			20			20	µA
		5.5 V			20			20	
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			500			500	µA
C_i	V_I = V_{CC} or GND	3.3 V		2.5			2.5		pF
		5 V		3			3		

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			SN54LV164						UNIT
			V_{CC} = 5.5 V ± 0.5 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	40	0	35	0	30	MHz
t_w	Pulse duration	$\overline{CLR}$ low	14		16		18		ns
		CLK high or low	14		16		18		
t_{su}	Setup time, data before CLK↑	Data	8		10		12		ns
		$\overline{CLR}$ inactive	5		6		7		
t_h	Hold time, data after CLK↑		3		3		3		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			SN74LV164						UNIT
			V_{CC} = 5.5 V ± 0.5 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	40	0	35	0	30	MHz
t_w	Pulse duration	$\overline{CLR}$ low	14		16		18		ns
		CLK high or low	14		16		18		
t_{su}	Setup time, data before CLK↑	Data	8		10		12		ns
		$\overline{CLR}$ inactive	5		6		7		
t_h	Hold time, data after CLK↑		3		3		3		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LV164									UNIT
			V_{CC} = 5.5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			40	90		35	75		30			MHz
t_{pd}	CLK	Q		10	20		14	26			32	ns
t_{PHL}	$\overline{CLR}$	Q		12	20		16	26			32	ns

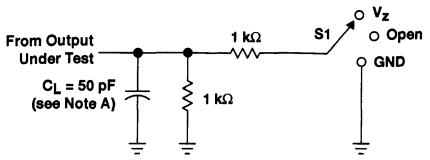
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LV164									UNIT
			V_{CC} = 5.5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			40	90		35	75		30			MHz
t_{pd}	CLK	Q		10	20		14	26			32	ns
t_{PHL}	$\overline{CLR}$	Q		12	20		16	26			32	ns

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	3.3 V	74	pF
			5 V	75	

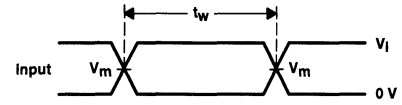
PARAMETER MEASUREMENT INFORMATION



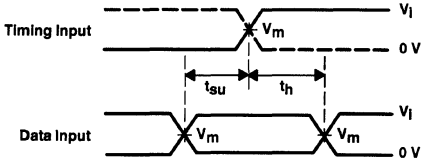
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_z
t_{PHZ}/t_{PZH}	GND

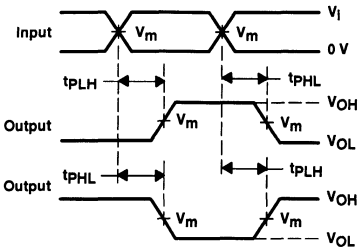
WAVEFORM CONDITION	V_{CC} = 4.5 V to 5.5 V	V_{CC} = 2.7 V to 3.6 V
V_m	0.5 × V_{CC}	1.5 V
V_I	V_{CC}	2.7 V
V_z	2 × V_{CC}	6 V



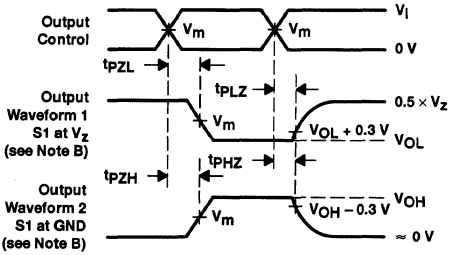
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

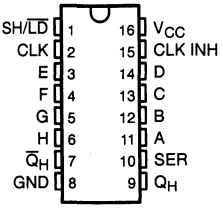
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

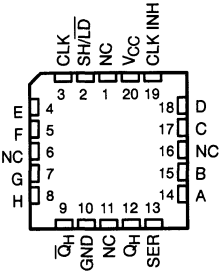
SCES007B – MARCH 1995 – REVISED APRIL 1996

- **EPIC™ (Enhanced-Performance Implanted CMOS) 2-μ Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC}, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) < 2 V at V_{CC}, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Flat (W) Packages, Chip Carriers (FK), and (J) 300-mil DIPs**

SN54LV165 . . . J OR W PACKAGE
SN74LV165 . . . D, DB, OR PW PACKAGE
(TOP VIEW)



SN54LV165 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'LV165 parallel-load, 8-bit shift registers are designed for 2.7-V to 5.5-V V_{CC} operation.

When the device is clocked, data is shifted toward the serial output Q_H. Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the SH/$\overline{LD}$ input. The 'LV165 feature a clock inhibit function and a complemented serial output $\overline{Q}_H$.

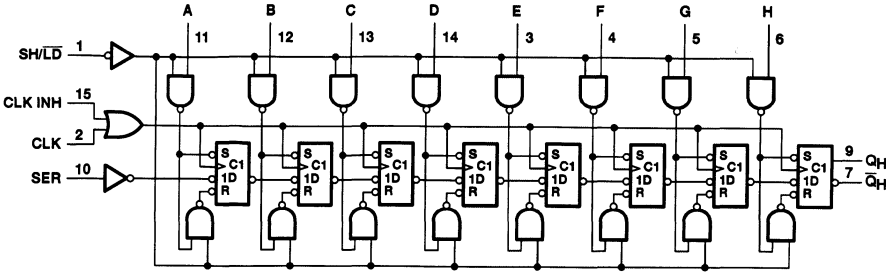
Clocking is accomplished by a low-to-high transition of the clock (CLK) input while SH/$\overline{LD}$ is held high and clock inhibit (CLK INH) is held low. The functions of the CLK and CLK INH inputs are interchangeable. Since a low CLK input and a low-to-high transition of CLK INH accomplishes clocking, CLK INH should be changed to the high level only while CLK is high. Parallel loading is inhibited when SH/$\overline{LD}$ is held high. The parallel inputs to the register are enabled while SH/$\overline{LD}$ is held low independently of the levels of CLK, CLK INH, or SER.

The SN54LV165 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV165 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

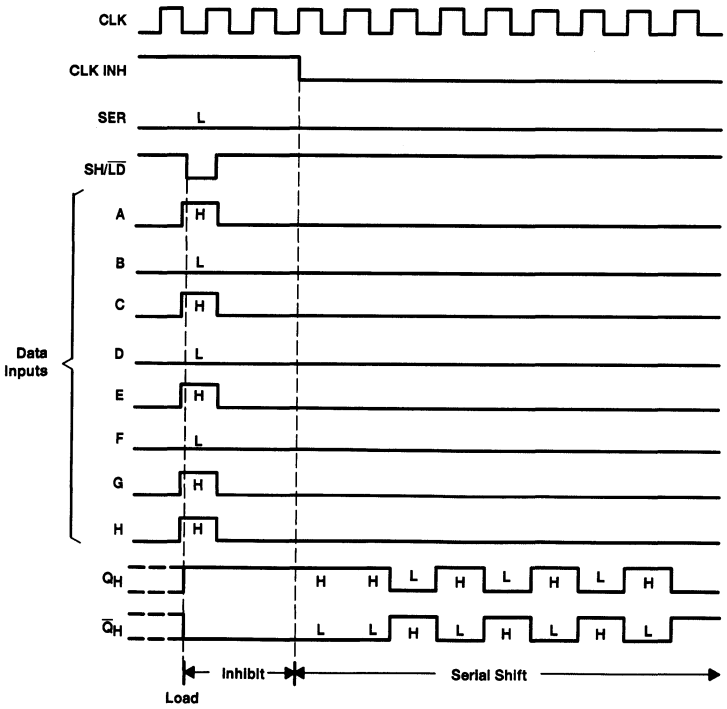
INPUTS			OPERATION
SH/$\overline{LD}$	CLK	CLK INH	
L	X	X	Parallel load
H	H	X	Q_0
H	X	H	Q_0
H	L	↑	Shift
H	↑	L	Shift

logic diagram (positive logic)



Pin numbers shown are for D, DB, J, PW, and W packages.

typical shift, load, and inhibit sequences



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 25 mA
Continuous current through V_{CC} or GND ..... ± 50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): D package ..... 1.30 W
DB package ..... 0.55 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 4)

			SN54LV165		SN74LV165		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	5.5	2.7	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		2		V
		V_{CC} = 4.5 V to 5.5 V	3.15		3.15		
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8		0.8	V
		V_{CC} = 4.5 V to 5.5 V		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V to 3.6 V		−6		−6	mA
		V_{CC} = 4.5 V to 5.5 V		−12		−12	
I_{OL}	Low-level output current	V_{CC} = 2.7 V to 3.6 V		6		6	mA
		V_{CC} = 4.5 V to 5.5 V		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	100	0	100	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}†	SN54LV165			SN74LV165			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = –100 μA	MIN to MAX	V_{CC}–0.2			V_{CC}–0.2			V
	I_{OH} = –6 mA	3 V	2.4			2.4			
	I_{OH} = –12 mA	4.5 V	3.6			3.6			
V_{OL}	I_{OL} = 100 μA	MIN to MAX			0.2			0.2	V
	I_{OL} = 6 mA	3 V			0.4			0.4	
	I_{OL} = 12 mA	4.5 V			0.55			0.55	
I_I	V_I = V_{CC} or GND	3.6 V			±1			±1	μA
		5.5 V			±1			±1	
I_{CC}	V_I = V_{CC} or GND, I_O = 0	3.6 V			20			20	μA
		5.5 V			20			20	
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			500			500	μA
C_i	V_I = V_{CC} or GND	3.3 V		2.5			2.5		pF
		5 V		3			3		

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			SN54LV165						UNIT
			V_{CC} = 5.5 V ± 0.5 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	50	0	40	0	30	MHz
t_w	Pulse duration	$\overline{CLK}$ high or low	14		18		22		ns
		SH/$\overline{LD}$ low	14		18		22		
t_{su}	Setup time	SH/$\overline{LD}$ high before $\overline{CLK}$↑	10		13		17		ns
		SER before $\overline{CLK}$↑	8		11		14		
		CLK INH before $\overline{CLK}$↑	10		12		15		
		Data before SH/$\overline{LD}$↑	8		12		17		
t_h	Hold time	SER data after $\overline{CLK}$↑	6		6		5		ns
		Parallel data after SH/$\overline{LD}$↑	6		6		5		

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			SN74LV165						UNIT
			V_{CC} = 5.5 V ± 0.5 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	50	0	40	0	30	MHz
t_w	Pulse duration	$\overline{CLK}$ high or low	14		18		22		ns
		SH/$\overline{LD}$ low	14		18		22		
t_{su}	Setup time	SH/$\overline{LD}$ high before $\overline{CLK}\uparrow$	10		13		17		ns
		SER before $\overline{CLK}\uparrow$	8		11		14		
		CLK INH before $\overline{CLK}\uparrow$	10		12		15		
		Data before SH/$\overline{LD}\uparrow$	8		12		17		
t_h	Hold time	SER data after $\overline{CLK}\uparrow$	6		6		5		ns
		Parallel data after SH/$\overline{LD}\uparrow$	6		6		5		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LV165								UNIT
			V_{CC} = 5.5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
f_{max}			50	90		40	75		30		MHz
t_{pd}	CLK	Q_H or $\overline{Q}_H$		20	25		20	38		47	ns
	SH/$\overline{LD}$			19	24		19	36		44	
	H			15	20		15	29		36	

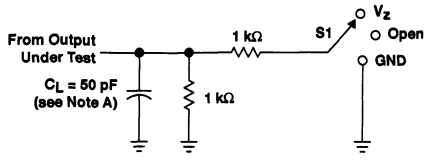
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LV165								UNIT
			V_{CC} = 5.5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
f_{max}			50	90		40	75		30		MHz
t_{pd}	CLK	Q_H or $\overline{Q}_H$		20	24		20	38		47	ns
	SH/$\overline{LD}$			19	24		19	36		44	
	H			15	20		15	29		36	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	3.3 V	33	pF
			5 V	57	

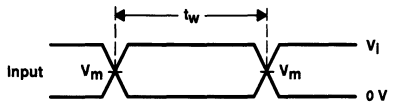
PARAMETER MEASUREMENT INFORMATION



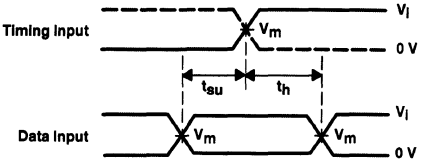
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_z
t_{PHZ}/t_{PZH}	GND

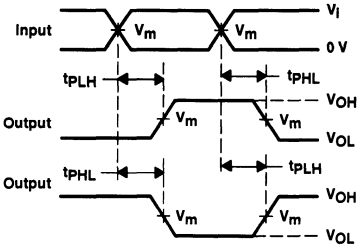
WAVEFORM CONDITION	V_{CC} = 4.5 V to 5.5 V	V_{CC} = 2.7 V to 3.6 V
V_m	0.5 × V_{CC}	1.5 V
V_I	V_{CC}	2.7 V
V_z	2 × V_{CC}	6 V



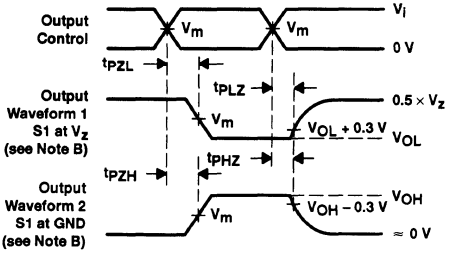
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



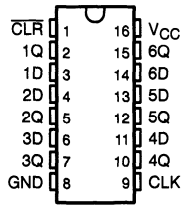
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

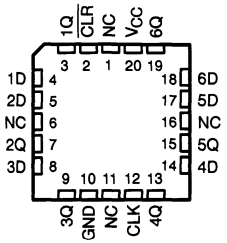
Figure 1. Load Circuit and Voltage Waveforms

- *EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC}, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC}, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Flat (W) Packages, Chip Carriers (FK), and (J) 300-mil DIPs

SN54LV174 . . . J OR W PACKAGE
SN74LV174 . . . D, DB, OR PW PACKAGE
(TOP VIEW)



SN54LV174 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These hex D-type flip-flops are designed for 2.7-V to 5.5-V V_{CC} operation.

The 'LV174 are monolithic positive-edge-triggered flip-flops with a direct clear ($\overline{CLR}$) input. Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of the clock pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

The SN74LV174 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

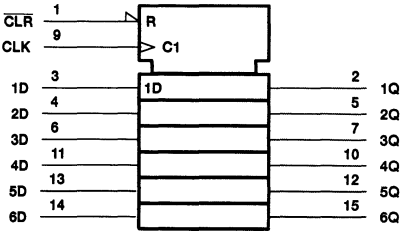
The SN54LV174 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV174 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

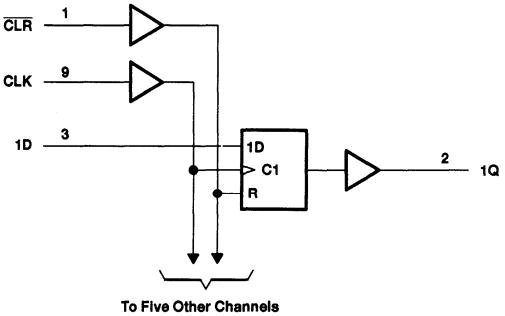
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, DB, J, PW, and W packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): D package ..... 1.3 W
DB package ..... 0.55 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 4)

			SN54LV174		SN74LV174		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	5.5	2.7	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		2		V
		V_{CC} = 4.5 V to 5.5 V	3.15		3.15		
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8		0.8	V
		V_{CC} = 4.5 V to 5.5 V		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V to 3.6 V		–6		–6	mA
		V_{CC} = 4.5 V to 5.5 V		–12		–12	
I_{OL}	Low-level output current	V_{CC} = 2.7 V to 3.6 V		6		6	mA
		V_{CC} = 4.5 V to 5.5 V		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	100	0	100	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}†	SN54LV174			SN74LV174			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = –100 μA	MIN to MAX	V_{CC} – 0.2			V_{CC} – 0.2			V
	I_{OH} = –6 mA	3 V	2.4			2.4			
	I_{OH} = –12 mA	4.5	3.6			3.6			
V_{OL}	I_{OL} = 100 μA	MIN to MAX			0.2			0.2	V
	I_{OL} = 6 mA	3 V			0.4			0.4	
	I_{OL} = 12 mA	4.5 V			0.55			0.55	
I_I	V_I = V_{CC} or GND	3.6 V			±1			±1	μA
		5.5 V			±1			±1	
I_{CC}	V_I = V_{CC} or GND, I_O = 0	3.6 V			20			20	μA
		5.5 V			20			20	
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			500			500	μA
C_i	V_I = V_{CC} or GND	3.3 V		2.5			2.5		pF
		5 V		3			3		

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			SN54LV174						UNIT
			V_{CC} = 5 V ± 0.5 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	40	0	30	0	24	MHz
t_w	Pulse duration	$\overline{CLR}$ low	12		18		22		ns
		CLK high or low	12		18		22		
t_{su}	Setup time before CLK↑	Data	10		12		14		ns
		$\overline{CLR}$ inactive	3		3		3		
t_h	Hold time, data after CLK↑		3		3		3		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			SN74LV174						UNIT
			V_{CC} = 5 V ± 0.5 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	40	0	30	0	24	MHz
t_w	Pulse duration	$\overline{CLR}$ low	12		18		22		ns
		CLK high or low	12		18		22		
t_{su}	Setup time before CLK↑	Data	10		12		14		ns
		$\overline{CLR}$ inactive	3		3		3		
t_h	Hold time, data after CLK↑		3		3		3		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LV174								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
f_{max}			40	90		30	80		24		MHz
t_{pd}	$\overline{CLR}$	Q		9	18		12	23		28	ns
	CLK			8	20		13	29		36	

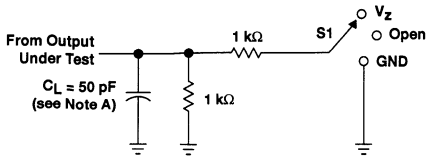
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LV174								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
f_{max}			40	90		30	80		24		MHz
t_{pd}	$\overline{CLR}$	Q		9	18		12	23		28	ns
	CLK			8	20		13	29		36	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	C_L = 50 pF, f = 10 MHz	3.3 V	24	pF
			5 V	52	

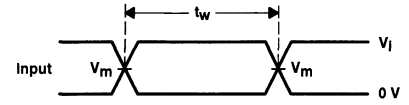
PARAMETER MEASUREMENT INFORMATION



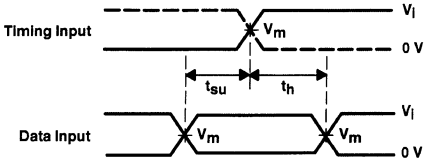
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_z
t_{PHZ}/t_{PZH}	GND

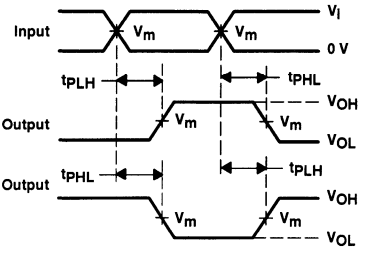
WAVEFORM CONDITION	V_{CC} = 4.5 V to 5.5 V	V_{CC} = 2.7 V to 3.6 V
V_m	$0.5 \times V_{CC}$	1.5 V
V_I	V_{CC}	2.7 V
V_z	$2 \times V_{CC}$	6 V



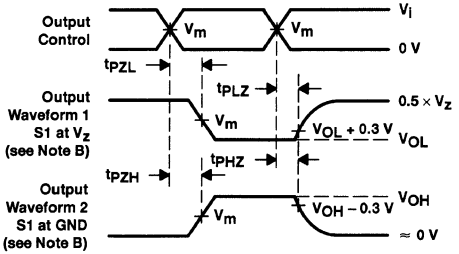
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



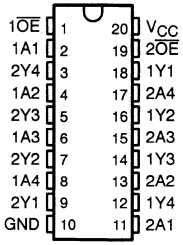
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

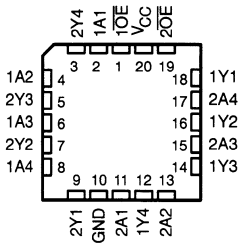
Figure 1. Load Circuit and Voltage Waveforms

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC}, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC}, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Flat (W) Packages, Chip Carriers (FK), and (J) 300-mil DIPs**

SN54LV240 . . . J OR W PACKAGE
SN74LV240 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LV240 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers/drivers are designed for 2.7-V to 5.5-V V_{CC} operation.

The 'LV240 are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The 'LV240 are organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The SN74LV240 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

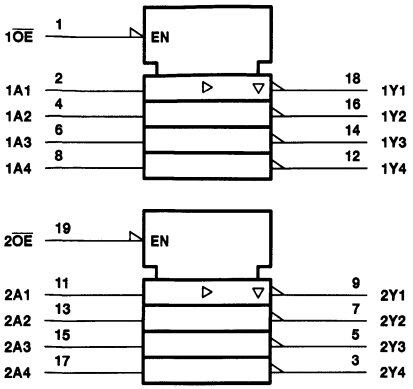
The SN54LV240 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV240 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

EPIC is a trademark of Texas Instruments Incorporated.

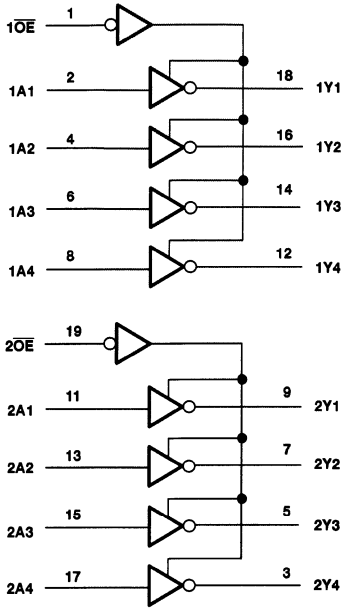
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DB, DW, J, PW, and W packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 4)

			SN54LV240		SN74LV240		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	5.5	2.7	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		2		V
		V_{CC} = 4.5 V to 5.5 V	3.15		3.15		
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8		0.8	V
		V_{CC} = 2.7 V to 3.6 V		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V to 3.6 V		–8		–8	mA
		V_{CC} = 4.5 V to 5.5 V		–16		–16	
I_{OL}	Low-level output current	V_{CC} = 2.7 V to 3.6 V		8		8	mA
		V_{CC} = 4.5 V to 5.5 V		16		16	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	100	0	100	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}†	SN54LV240			SN74LV240			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = –100 μA	MIN to MAX	V_{CC} – 0.2			V_{CC} – 0.2			V
	I_{OH} = –8 mA	3 V	2.4			2.4			
	I_{OH} = –16 mA	4.5 V	3.6			3.6			
V_{OL}	I_{OL} = 100 μA	MIN to MAX			0.2			0.2	V
	I_{OL} = 8 mA	3 V			0.4			0.4	
	I_{OL} = 16 mA	4.5 V			0.55			0.55	
I_I	V_I = V_{CC} or GND	3.6 V			±1			±1	μA
		5.5 V			±1			±1	
I_{OZ}	V_O = V_{CC} or GND	3.6 V			±5			±5	μA
		5.5 V			±5			±5	
I_{CC}	V_I = V_{CC} or GND, I_O = 0	3.6 V			20			20	μA
		5.5 V			20			20	
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			500			500	μA
C_i	V_I = V_{CC} or GND	3.3 V		3			3		pF
		5 V		3			3		
C_o	V_O = V_{CC} or GND	3.3 V		8			8		pF
		5 V		8			8		

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LV240								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y		7	13		9	16		18	ns
t_{en}	$\overline{OE}$	Y		11	18		14	24		28	ns
t_{dis}	$\overline{OE}$	Y		12	23		14	24		25	ns

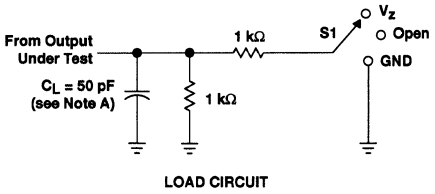
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LV240								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y		7	13		9	16		18	ns
t_{en}	$\overline{OE}$	Y		11	18		14	24		28	ns
t_{dis}	$\overline{OE}$	Y		12	23		14	24		25	ns

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	C_L = 50 pF, f = 10 MHz	3.3 V	45	pF
		Outputs disabled			2.5	
		Outputs enabled		5 V	78	
		Outputs disabled			3	

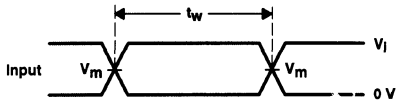
PARAMETER MEASUREMENT INFORMATION



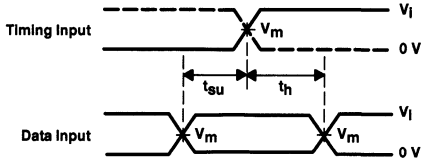
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_Z
t_{PHZ}/t_{PZH}	GND

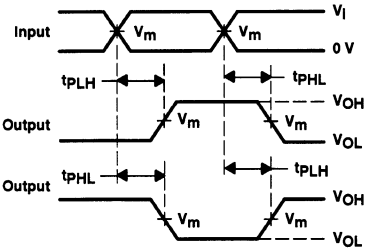
WAVEFORM CONDITION	V_{CC} = 4.5 V to 5.5 V	V_{CC} = 2.7 V to 3.6 V
V_m	0.5 × V_{CC}	1.5 V
V_I	V_{CC}	2.7 V
V_Z	2 × V_{CC}	6 V



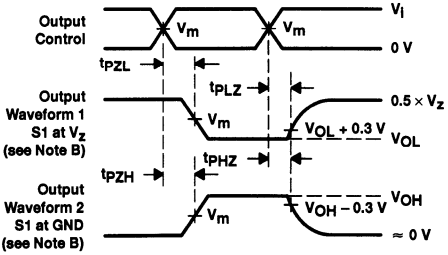
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



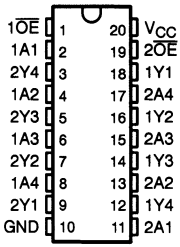
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

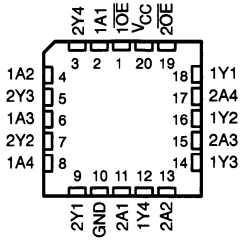
Figure 1. Load Circuit and Voltage Waveforms

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC}, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC}, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Flat (W) Packages, Chip Carriers (FK), and (J) 300-mil DIPs**

SN54LV244 . . . J OR W PACKAGE
SN74LV244 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LV244 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers/line drivers are designed for 2.7-V to 5.5-V V_{CC} operation.

The 'LV244 are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The 'LV244 are organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The SN74LV244 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

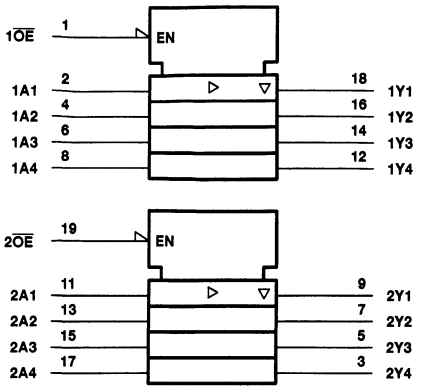
The SN54LV244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV244 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

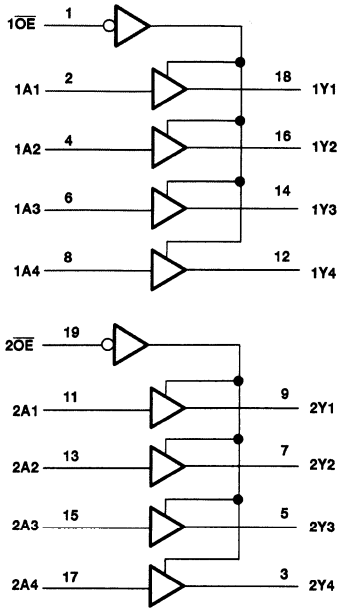
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DB, DW, J, PW, and W packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 4)

			SN54LV244		SN74LV244		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	5.5	2.7	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		2		V
		V_{CC} = 4.5 V to 5.5 V	3.15		3.15		
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8		0.8	V
		V_{CC} = 4.5 V to 5.5 V		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V to 3.6 V		–8		–8	mA
		V_{CC} = 4.5 V to 5.5 V		–16		–16	
I_{OL}	Low-level output current	V_{CC} = 2.7 V to 3.6 V		8		8	mA
		V_{CC} = 4.5 V to 5.5 V		16		16	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	100	0	100	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}†	SN54LV244			SN74LV244			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = –100 µA	MIN to MAX	V_{CC} – 0.2			V_{CC} – 0.2			V
	I_{OH} = –8 mA	3 V	2.4			2.4			
	I_{OH} = –16 mA	4.5 V	3.6			3.6			
V_{OL}	I_{OL} = 100 µA	MIN to MAX			0.2			0.2	V
	I_{OL} = 8 mA	3 V			0.4			0.4	
	I_{OL} = 16 mA	4.5 V			0.55			0.55	
I_I	V_I = V_{CC} or GND	3.6 V			±1			±1	µA
		5.5 V			±1			±1	
I_{OZ}	V_O = V_{CC} or GND	3.6 V			±5			±5	µA
		5.5 V			±5			±5	
I_{CC}	V_I = V_{CC} or GND, I_O = 0	3.6 V			20			20	µA
		5.5 V			20			20	
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			500			500	µA
C_i	V_I = V_{CC} or GND	3.3 V		3			3		pF
		5 V		3			3		
C_o	V_O = V_{CC} or GND	3.3 V		8			8		pF
		5 V		8			8		

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LV244								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y		7	12		9	14		17	ns
t_{en}	$\overline{OE}$	Y		10	19		13	23		29	ns
t_{dis}	$\overline{OE}$	Y		10	20		13	21		24	ns

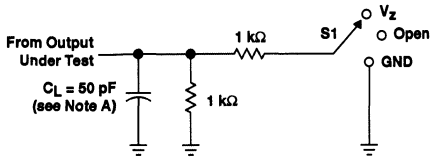
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LV244								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y		7	12		9	14		17	ns
t_{en}	$\overline{OE}$	Y		10	19		13	23		29	ns
t_{dis}	$\overline{OE}$	Y		10	20		13	21		24	ns

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	C_L = 50 pF,	f = 10 MHz	3.3 V	40	pF
		Outputs disabled				4	
		Outputs enabled			5 V	73	
		Outputs disabled				4	

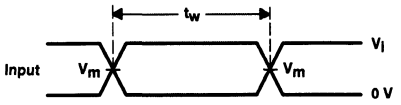
PARAMETER MEASUREMENT INFORMATION



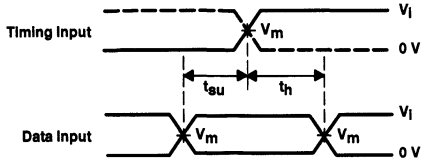
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_z
t_{PHZ}/t_{PZH}	GND

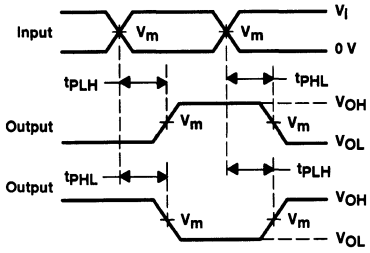
WAVEFORM CONDITION	V_{CC} = 4.5 V to 5.5 V	V_{CC} = 2.7 V to 3.6 V
V_m	0.5 × V_{CC}	1.5 V
V_I	V_{CC}	2.7 V
V_z	2 × V_{CC}	6 V



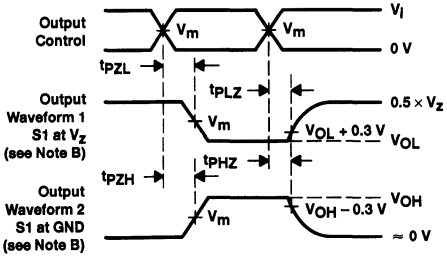
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



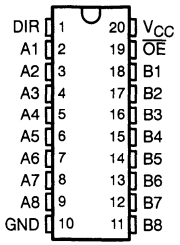
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

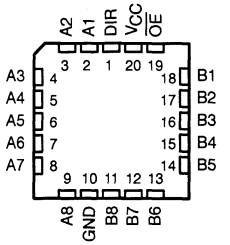
Figure 1. Load Circuit and Voltage Waveforms

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC}, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC}, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Flat (W) Packages, Chip Carriers (FK), and (J) 300-mil DIPs**

SN54LV245 . . . J OR W PACKAGE
SN74LV245 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LV245 . . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for 2.7-V to 5.5-V V_{CC} operation.

The 'LV245 are designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

The SN74LV245 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

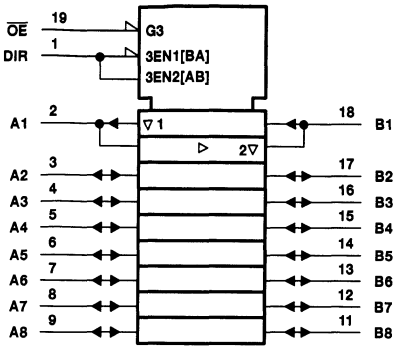
The SN54LV245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

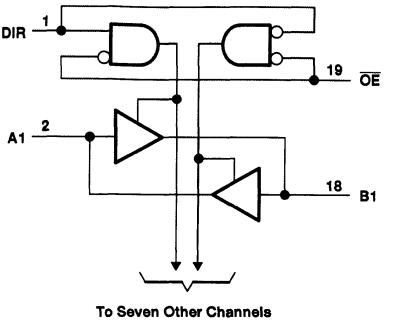
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DB, DW, J, PW, and W packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I: Except I/O ports (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
I/O ports (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 4)

			SN54LV245		SN74LV245		UNIT
			MIN	MAX	MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	5.5	2.7	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		2		V
		V_{CC} = 4.5 V to 5.5 V	3.15		3.15		
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8		0.8	V
		V_{CC} = 4.5 V to 5.5 V		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V to 3.6 V		–8		–8	mA
		V_{CC} = 4.5 V to 5.5 V		–16		–16	
I_{OL}	Low-level output current	V_{CC} = 2.7 V to 3.6 V		8		8	mA
		V_{CC} = 4.5 V to 5.5 V		16		16	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	50	0	50	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}†	SN54LV245			SN74LV245			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}		I_{OH} = –100 μA	MIN to MAX	V_{CC}–0.2			V_{CC}–0.2			V
		I_{OH} = –8 mA	3 V	2.4			2.4			
		I_{OH} = –16 mA	4.5 V	3.6			3.6			
V_{OL}		I_{OL} = 100 μA	MIN to MAX			0.2			0.2	V
		I_{OL} = 8 mA	3 V			0.4			0.4	
		I_{OL} = 16 mA	4.5 V			0.55			0.55	
I_I		V_I = V_{CC} or GND	3.6 V			±1			±1	μA
			5.5 V			±1			±1	
I_{OZ}‡		V_O = V_{CC} or GND	3.6 V			±5			±5	μA
			5.5 V			±5			±5	
I_{CC}		V_I = V_{CC} or GND, I_O = 0	3.6 V			20			20	μA
			5.5 V			20			20	
ΔI_{CC}		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			500			500	μA
C_i	Control inputs	V_I = V_{CC} or GND	3.3 V		2.5			2.5		pF
			5 V		3			3		
C_o	A or B port	V_O = V_{CC} or GND	3.3 V		7			7		pF
			5 V		8			8		

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LV245								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	B or A		8	11		8	14		18	ns
t_{en}	$\overline{OE}$	A or B		6	14		12	21		25	ns
t_{dis}	$\overline{OE}$	A or B		8	16		12	20		24	ns

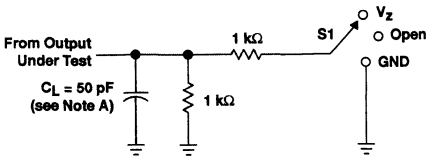
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LV245								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	B or A		8	11		8	14		18	ns
t_{en}	$\overline{OE}$	A or B		6	14		12	21		25	ns
t_{dis}	$\overline{OE}$	A or B		8	16		12	20		24	ns

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF,	f = 10 MHz	3.3 V	36	pF
		Outputs disabled				4	
		Outputs enabled			5 V	46	
		Outputs disabled				4	

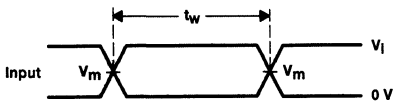
PARAMETER MEASUREMENT INFORMATION



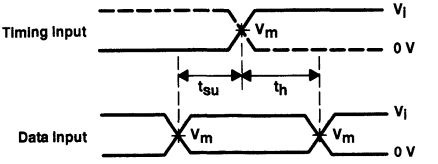
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_Z
t_{PHZ}/t_{PZH}	GND

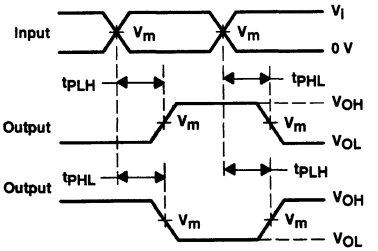
WAVEFORM CONDITION	V_{CC} = 4.5 V to 5.5 V	V_{CC} = 2.7 V to 3.6 V
V_m	0.5 × V_{CC}	1.5 V
V_I	V_{CC}	2.7 V
V_Z	2 × V_{CC}	6 V



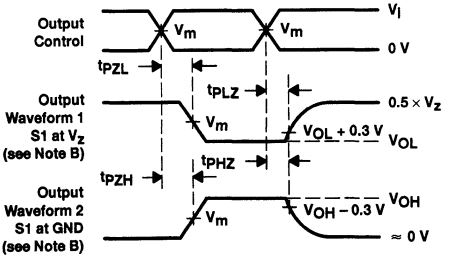
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



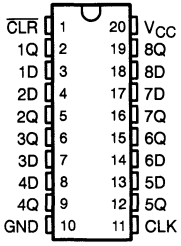
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

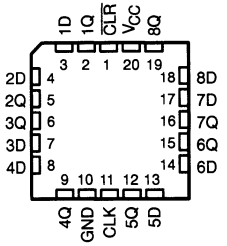
Figure 1. Load Circuit and Voltage Waveforms

- *EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC}, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC}, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Flat (W) Packages, Chip Carriers (FK), and (J) 300-mil DIPs

SN54LV273 . . . J OR W PACKAGE
SN74LV273 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LV273 . . . FK PACKAGE
(TOP VIEW)



description

These octal D-type flip-flops are designed for 2.7-V to 5.5-V V_{CC} operation.

The 'LV273 are positive-edge-triggered flip-flops with direct clear ($\overline{CLR}$) input. Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

The SN74LV273 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

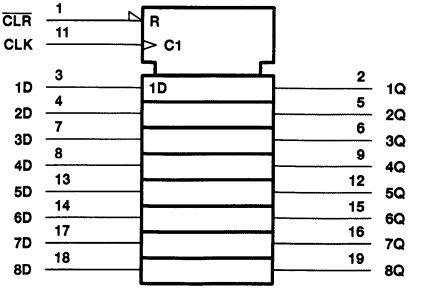
The SN54LV273 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV273 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

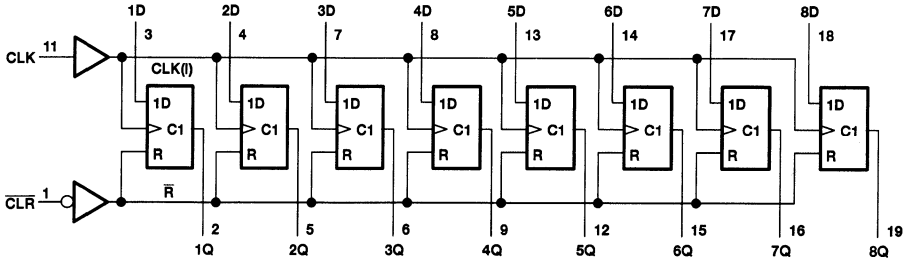
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DB, DW, J, PW, and W packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 4)

			SN54LV273		SN74LV273		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	5.5	2.7	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		2		V
		V_{CC} = 4.5 V to 5.5 V	3.15		3.15		
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8		0.8	V
		V_{CC} = 4.5 V to 5.5 V		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V to 3.6 V		–6		–6	mA
		V_{CC} = 4.5 V to 5.5 V		–12		–12	
I_{OL}	Low-level output current	V_{CC} = 2.7 V to 3.6 V		6		6	mA
		V_{CC} = 4.5 V to 5.5 V		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	100	0	100	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}†	SN54LV273			SN74LV273			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = –100 μA		MIN to MAX	V_{CC}–0.2			V_{CC}–0.2			V
	I_{OH} = –6 mA		3 V	2.4			2.4			
	I_{OH} = –12 mA		4.5 V	3.6			3.6			
V_{OL}	I_{OL} = 100 μA		MIN to MAX			0.2			0.2	V
	I_{OL} = 6 mA		3 V			0.4			0.4	
	I_{OL} = 12 mA		4.5 V			0.55			0.55	
I_I	V_I = V_{CC} or GND		3.6 V			±1			±1	μA
			5.5 V			±1			±1	
I_{OZ}	V_O = V_{CC} or GND,	I_O = 0	3.6 V			±5			±5	μA
			5.5 V			±5			±5	
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V			20			20	μA
			5.5 V			20			20	
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		3 V to 3.6 V			500			500	μA
C_i	V_I = V_{CC} or GND		3.3 V		2.5			2.5		pF
			5 V		3			3		

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			SN54LV273						UNIT
			V_{CC} = 5.5 V ± 0.5 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	60	0	50	0	40	MHz
t_w	Pulse duration	$\overline{CLR}$ low	6		10		12		ns
		CLK high or low	7		10		12		
t_{su}	Setup time before CLK↑	Data	8		12		14		ns
		$\overline{CLR}$ inactive	2		2		2		
t_h	Hold time, data after CLK↑		3		2		2		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			SN74LV273						UNIT
			V_{CC} = 5.5 V ± 0.5 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	60	0	50	0	40	MHz
t_w	Pulse duration	$\overline{CLR}$ low	6		10		12		ns
		CLK high or low	7		10		12		
t_{su}	Setup time before CLK↑	Data	8		12		14		ns
		$\overline{CLR}$ inactive	2		2		2		
t_h	Hold time, data after CLK↑		3		2		2		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LV273								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
f_{max}			60	100		50	80		40		MHz
t_{pd}	CLK	Q		11	16		16	22		26	ns
t_{PHL}	$\overline{CLR}$	Q		13	22		14	24		30	ns

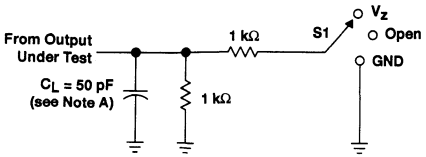
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LV273								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
f_{max}			60	100		50	80		40		MHz
t_{pd}	CLK	Q		11	16		16	22		26	ns
t_{PHL}	$\overline{CLR}$	Q		13	22		14	24		30	ns

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	C_L = 50 pF, f = 10 MHz	3.3 V	32	pF
			5 V	41	

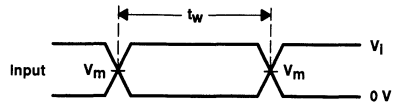
PARAMETER MEASUREMENT INFORMATION



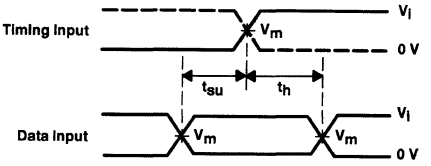
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_Z
t_{PHZ}/t_{PZH}	GND

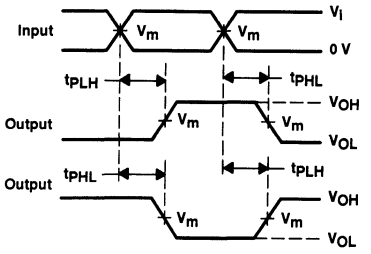
WAVEFORM CONDITION	V_{CC} = 4.5 V to 5.5 V	V_{CC} = 2.7 V to 3.6 V
V_m	$0.5 \times V_{CC}$	1.5 V
V_I	V_{CC}	2.7 V
V_Z	$2 \times V_{CC}$	6 V



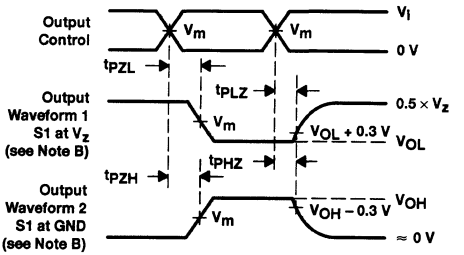
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



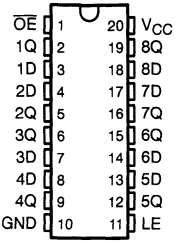
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

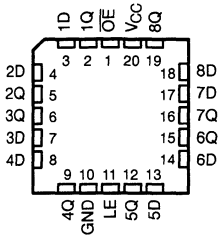
Figure 1. Load Circuit and Voltage Waveforms

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC}, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC}, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Flat (W) Packages, Chip Carriers (FK), and (J) 300-mil DIPs**

SN54LV373 . . . J OR W PACKAGE
SN74LV373 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LV373 . . . FK PACKAGE
(TOP VIEW)



description

These octal transparent D-type latches are designed for 2.7-V to 5.5-V V_{CC} operation.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LV373 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

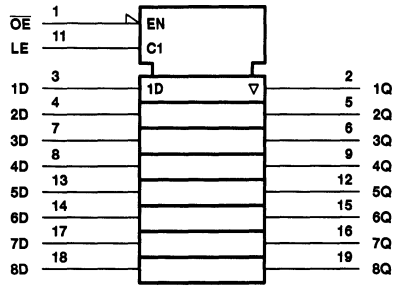
The SN54LV373 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV373 is characterized for operation from –40°C to 85°C.

EPIC is a trademark of Texas Instruments Incorporated.

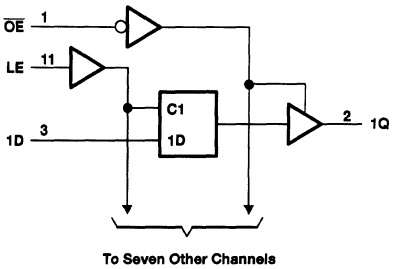
FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DB, DW, J, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 4)

			SN54LV373		SN74LV373		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	5.5	2.7	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		2		V
		V_{CC} = 4.5 V to 5.5 V	3.15		3.15		
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8		0.8	V
		V_{CC} = 4.5 V to 5.5 V		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V to 3.6 V		–8		–8	mA
		V_{CC} = 4.5 V to 5.5 V		–16		–16	
I_{OL}	Low-level output current	V_{CC} = 2.7 V to 3.6 V		8		8	mA
		V_{CC} = 4.5 V to 5.5 V		16		16	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	100	0	100	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}†	SN54LV373			SN74LV373			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = –100 µA	MIN to MAX	V_{CC}–0.2			V_{CC}–0.2			V
	I_{OH} = –8 mA	3 V	2.4			2.4			
	I_{OH} = –16 mA	4.5 V	3.6			3.6			
V_{OL}	I_{OL} = 100 µA	MIN to MAX			0.2			0.2	V
	I_{OL} = 8 mA	3 V			0.4			0.4	
	I_{OL} = 16 mA	4.5 V			0.55			0.55	
I_I	V_I = V_{CC} or GND	3.6 V			±1			±1	µA
		5.5 V			±1			±1	
I_{OZ}	V_O = V_{CC} or GND	3.6 V			±5			±5	µA
		5.5 V			±5			±5	
I_{CC}	V_I = V_{CC} or GND, I_O = 0	3.6 V			20			20	µA
		5.5 V			20			20	
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			500			500	µA
C_i	V_I = V_{CC} or GND	3.3 V		2.5			2.5		pF
		5 V		3			3		
C_o	V_O = V_{CC} or GND	3.3 V		7			7		pF
		5 V		7.5			7.5		

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			SN54LV373						UNIT
			V_{CC} = 5 V ± 0.5 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high		10		10		8		ns
t_{su}	Setup time, data before LE↓	High or low	4		6		6		ns
t_h	Hold time, data after LE↓	High or low	6		6		6		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			SN74LV373						UNIT
			V_{CC} = 5 V ± 0.5 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high		10		10		8		ns
t_{su}	Setup time, data before LE↓	High or low	4		6		6		ns
t_h	Hold time, data after LE↓	High or low	6		6		6		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LV373									UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN		MAX	
t_{pd}	D	Q		8	16		11	22			28	ns
	LE			11	19		15	25			26	
t_{en}	$\overline{OE}$	Q		15	23		15	27			28	ns
t_{dis}	$\overline{OE}$	Q		15	23		15	27			28	ns

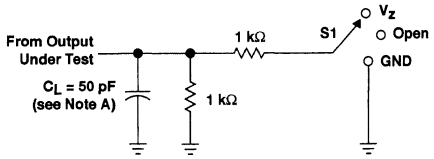
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LV373									UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN		MAX	
t_{pd}	D	Q		8	16		11	22			28	ns
	LE			11	19		15	25			26	
t_{en}	$\overline{OE}$	Q		15	23		15	27			28	ns
t_{dis}	$\overline{OE}$	Q		15	23		15	27			28	ns

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 10 MHz	3.3 V	47	pF
		Outputs disabled			29	
		Outputs enabled		5 V	112	
		Outputs disabled			62	

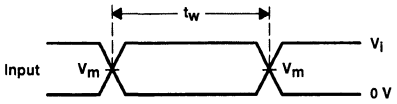
PARAMETER MEASUREMENT INFORMATION



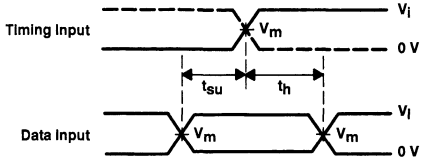
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_z
t_{PHZ}/t_{PZH}	GND

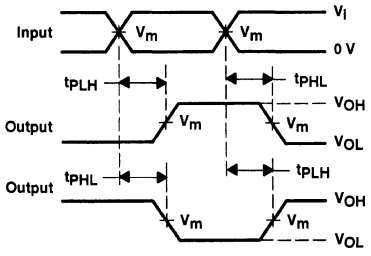
WAVEFORM CONDITION	V_{CC} = 4.5 V to 5.5 V	V_{CC} = 2.7 V to 3.6 V
V_m	0.5 × V_{CC}	1.5 V
V_I	V_{CC}	2.7 V
V_z	2 × V_{CC}	6 V



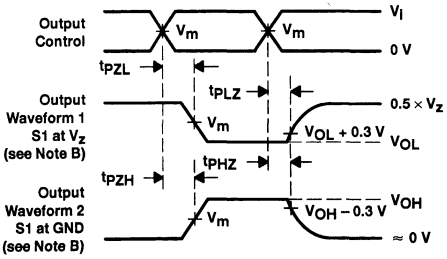
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



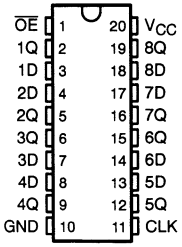
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

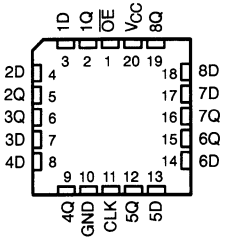
Figure 1. Load Circuit and Voltage Waveforms

- *EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC}, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC}, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Flat (W) Packages, Chip Carriers (FK), and (J) 300-mil DIPs

SN54LV374 . . . J OR W PACKAGE
SN74LV374 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LV374 . . . FK PACKAGE
(TOP VIEW)



description

These octal edge-triggered D-type flip-flops are designed for 2.7-V to 5.5-V V_{CC} operation.

The 'LV374 feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either as normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LV374 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

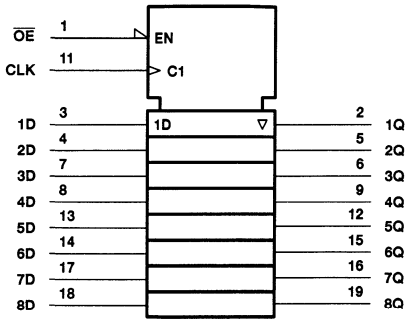
The SN54LV374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV374 is characterized for operation from –40°C to 85°C.

EPIC is a trademark of Texas Instruments Incorporated.

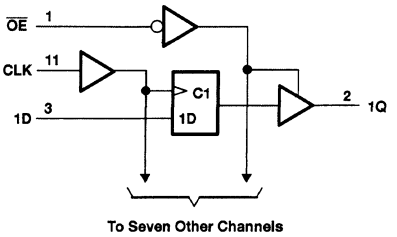
FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DB, DW, J, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 4)

			SN54LV374		SN74LV374		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	5.5	2.7	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		2		V
		V_{CC} = 4.5 V to 5.5 V	3.15		3.15		
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8		0.8	V
		V_{CC} = 4.5 V to 5.5 V		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V to 3.6 V		−8		−8	mA
		V_{CC} = 4.5 V to 5.5 V		−16		−16	
I_{OL}	Low-level output current	V_{CC} = 2.7 V to 3.6 V		8		8	mA
		V_{CC} = 4.5 V to 5.5 V		16		16	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	100	0	100	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}†	SN54LV374			SN54LV374			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = −100 μA	MIN to MAX	V_{CC}−0.2			V_{CC}−0.2			V
	I_{OH} = −8 mA	3 V	2.4			2.4			
	I_{OH} = −16 mA	4.5 V	3.6			3.6			
V_{OL}	I_{OL} = 100 μA	MIN to MAX			0.2			0.2	V
	I_{OL} = 8 mA	3 V			0.4			0.4	
	I_{OL} = 16 mA	4.5 V			0.55			0.55	
I_I	V_I = V_{CC} or GND	3.6 V			±1			±1	μA
		5.5 V			±1			±1	
I_{OZ}	V_O = V_{CC} or GND	3.6 V			±5			±5	μA
		5.5 V			±5			±5	
I_{CC}	V_I = V_{CC} or GND, I_O = 0	3.6 V			20			20	μA
		5.5 V			20			20	
ΔI_{CC}	One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			500			500	μA
C_i	V_I = V_{CC} or GND	3.3 V		2.5			2.5		pF
		5 V		3			3		
C_o	V_O = V_{CC} or GND	3.3 V		7			7		pF
		5 V		8			8		

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			SN54LV374						UNIT
			V_{CC} = 5 V ± 0.5 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	45	0	40	0	35	MHz
t_w	Pulse duration, CLK high or low		9		10		13		ns
t_{su}	Setup time before CLK↑	High or low	7		10		11		ns
t_h	Hold time, data after CLK↑		3		2		2		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			SN74LV374						UNIT
			V_{CC} = 5 V ± 0.5 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	45	0	40	0	35	MHz
t_w	Pulse duration, CLK high or low		9		10		13		ns
t_{su}	Setup time before CLK↑	High or low	7		10		11		ns
t_h	Hold time, data after CLK↑		3		2		2		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LV374								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
f_{max}			45	80		40	70		35		MHz
t_{pd}	CLK	Q		11	19		15	24		29	ns
t_{en}	$\overline{OE}$	Q		10	20		13	24		28	ns
t_{dis}	$\overline{OE}$	Q		8	21		12	24		29	ns

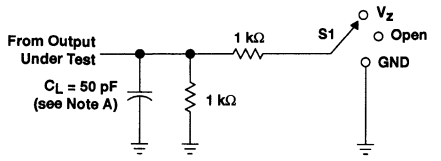
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LV374								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
f_{max}			45	80		40	70		35		MHz
t_{pd}	CLK	Q		11	19		15	24		29	ns
t_{en}	$\overline{OE}$	Q		10	20		13	24		28	ns
t_{dis}	$\overline{OE}$	Q		8	21		12	24		29	ns

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	C_L = 50 pF, f = 10 MHz	3.3 V	52	pF
		Outputs disabled			34	
		Outputs enabled		5 V	60	
		Outputs disabled			35	

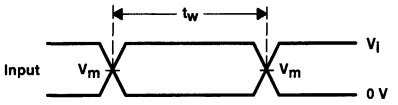
PARAMETER MEASUREMENT INFORMATION



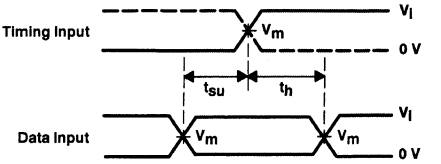
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_Z
t_{PHZ}/t_{PZH}	GND

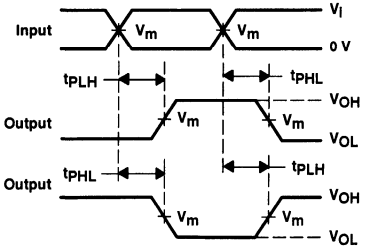
WAVEFORM CONDITION	V_{CC} = 4.5 V to 5.5 V	V_{CC} = 2.7 V to 3.6 V
V_m	$0.5 \times V_{CC}$	1.5 V
V_I	V_{CC}	2.7 V
V_Z	$2 \times V_{CC}$	6 V



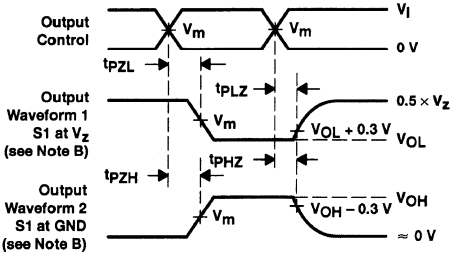
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



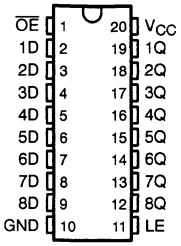
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

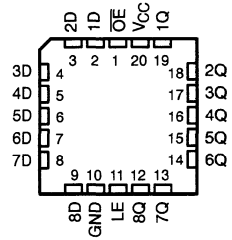
Figure 1. Load Circuit and Voltage Waveforms

- *EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC}, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC}, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Flat (W) Packages, Chip Carriers (FK), and (J) 300-mil DIPs

SN54LV573 . . . J OR W PACKAGE
SN74LV573 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LV573 . . . FK PACKAGE
(TOP VIEW)



description

These octal transparent D-type latches are designed for 2.7-V to 5.5-V V_{CC} operation.

The 'LV573 feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LV573 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

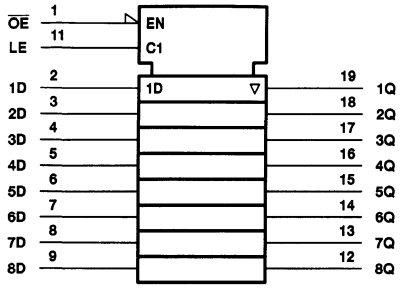
The SN54LV573 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV573 is characterized for operation from –40°C to 85°C.

EPIC is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE
(each latch)

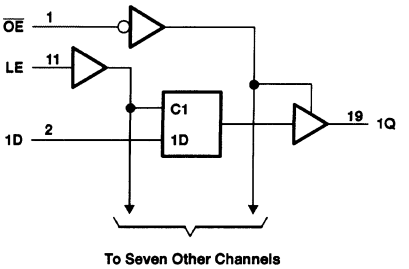
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DB, DW, J, PW, and W packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 4)

			SN54LV573		SN74LV573		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	5.5	2.7	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		2		V
		V_{CC} = 4.5 V to 5.5 V	3.15		3.15		
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8		0.8	V
		V_{CC} = 4.5 V to 5.5 V		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V to 3.6 V		–8		–8	mA
		V_{CC} = 4.5 V to 5.5 V		–16		–16	
I_{OL}	Low-level output current	V_{CC} = 2.7 V to 3.6 V		8		8	mA
		V_{CC} = 4.5 V to 5.5 V		16		16	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	100	0	100	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}†	SN54LV573			SN74LV573			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = –100 µA	MIN to MAX	V_{CC}–0.2			V_{CC}–0.2			V
	I_{OH} = – 8 mA	3 V	2.4			2.4			
	I_{OH} = – 16 mA	4.5 V	3.6			3.6			
V_{OL}	I_{OL} = 100 µA	MIN to MAX			0.2			0.2	V
	I_{OL} = 8 mA	3 V			0.4			0.4	
	I_{OL} = 16 mA	4.5 V			0.55			0.55	
I_I	V_I = V_{CC} or GND	3.6 V			±1			±1	µA
		5.5 V			±1			±1	
I_{OZ}	V_O = V_{CC} or GND	3.6 V			±5			±5	µA
		5.5 V			±5			±5	
I_{CC}	V_I = V_{CC} or GND, I_O = 0	3.6 V			20			20	µA
		5.5 V			20			20	
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			500			500	µA
C_i	V_I = V_{CC} or GND	3.3 V		2.5			2.5		pF
		5 V		3			3		
C_o	V_O = V_{CC} or GND	3.3 V		7			7		pF
		5 V		10			10		

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		SN54LV573						UNIT
		V_{CC} = 5.5 V ± 0.5 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	9		12		14		ns
t_{su}	Setup time, data before LE↓	4		6		7		ns
t_h	Hold time, data after LE↓	4		6		6		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		SN74LV573						UNIT
		V_{CC} = 5.5 V ± 0.5 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	9		12		14		ns
t_{su}	Setup time, data before LE↓	4		6		7		ns
t_h	Hold time, data after LE↓	4		6		6		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LV573								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}	D	Q		9	19		13	23		29	ns
	LE			12	21		19	25		31	
t_{en}	$\overline{OE}$	Q		11	18		16	22		28	ns
t_{dis}	$\overline{OE}$	Q		15	21		21	28		29	ns

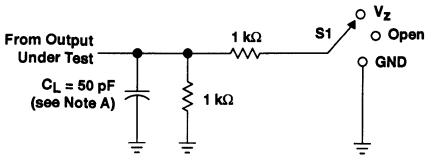
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LV573								UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}	D	Q		9	19		13	23		29	ns
	LE			12	21		19	25		31	
t_{en}	$\overline{OE}$	Q		11	18		16	22		28	ns
t_{dis}	$\overline{OE}$	Q		15	21		21	28		29	ns

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	VCC	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 10 MHz	3.3 V	30	pF
		Outputs disabled			14	
		Outputs enabled		5 V	36	
		Outputs disabled			16	

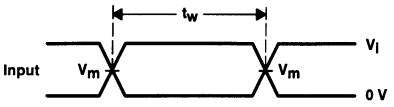
PARAMETER MEASUREMENT INFORMATION



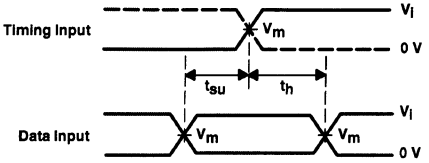
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_z
t_{PHZ}/t_{PZH}	GND

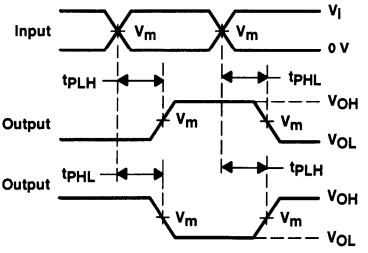
WAVEFORM CONDITION	V_{CC} = 4.5 V to 5.5 V	V_{CC} = 2.7 V to 3.6 V
V_m	0.5 × V_{CC}	1.5 V
V_I	V_{CC}	2.7 V
V_z	2 × V_{CC}	6 V



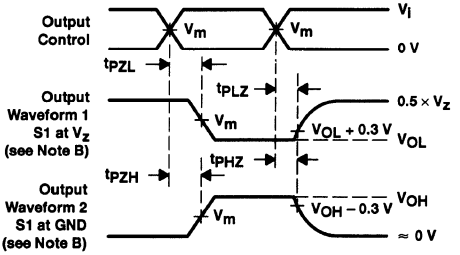
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



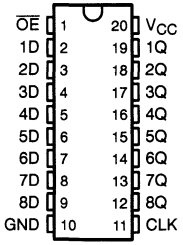
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

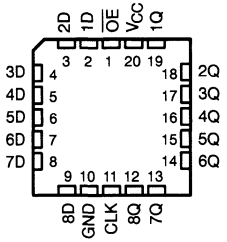
Figure 1. Load Circuit and Voltage Waveforms

- *EPIC*™ (Enhanced-Performance Implanted CMOS) 2-μ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC}, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC}, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Flat (W) Packages, Chip Carriers (FK), and (J) 300-mil DIPs

SN54LV574 . . . J OR W PACKAGE
SN74LV574 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LV574 . . . FK PACKAGE
(TOP VIEW)



description

These octal edge-triggered D-type flip-flops are designed for 2.7-V to 5.5-V V_{CC} operation.

The 'LV574 feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LV574 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

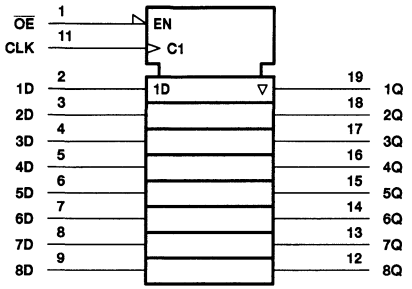
The SN54LV574 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV574 is characterized for operation from –40°C to 85°C.

EPIC is a trademark of Texas Instruments Incorporated.

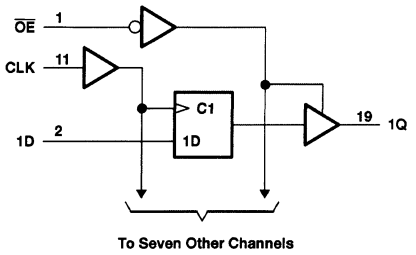
FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DB, DW, J, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±35 mA
Continuous current through V_{CC} or GND ..... ±70 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 4)

			SN54LV574		SN74LV574		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	5.5	2.7	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		2		V
		V_{CC} = 4.5 V to 5.5 V	3.15		3.15		
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8		0.8	V
		V_{CC} = 4.5 V to 5.5 V		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V to 3.6 V		–8		–8	mA
		V_{CC} = 4.5 V to 5.5 V		–16		–16	
I_{OL}	Low-level output current	V_{CC} = 2.7 V to 3.6 V		8		8	mA
		V_{CC} = 4.5 V to 5.5 V		16		16	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	100	0	100	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}†	SN54LV574			SN74LV574			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = –100 μA	MIN to MAX	V_{CC} – 0.2			V_{CC} – 0.2			V
	I_{OH} = – 8 mA	3 V	2.4			2.4			
	I_{OH} = – 16 mA	4.5	3.6			3.6			
V_{OL}	I_{OL} = 100 μA	MIN to MAX			0.2			0.2	V
	I_{OL} = 8 mA	3 V			0.4			0.4	
	I_{OL} = 16 mA	4.5 V			0.55			0.55	
I_I	V_I = V_{CC} or GND	3.6 V			±1			±1	μA
		5.5 V			±1			±1	
I_{OZ}	V_O = V_{CC} or GND	3.6 V			±5			±5	μA
		5.5 V			±5			±5	
I_{CC}	V_I = V_{CC} or GND, I_O = 0	3.6 V			20			20	μA
		5.5 V			20			20	
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			500			500	μA
C_i	V_I = V_{CC} or GND	3.3 V		2.5			2.5		pF
		5 V		3			3		
C_o	V_O = V_{CC} or GND	3.3 V		7			7		pF
		5 V		10			10		

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			SN54LV574						UNIT
			V_{CC} = 5 V ± 0.5 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			50		40		30	MHz
t_w	Pulse duration, CLK high or low		8		12		14		ns
t_{su}	Setup time before CLK↑	High or low	5		8		9		ns
t_h	Hold time, data after CLK↑		4		3		3		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			SN74LV574						UNIT
			V_{CC} = 5 V ± 0.5 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			50		40		30	MHz
t_w	Pulse duration, CLK high or low		8		12		14		ns
t_{su}	Setup time before CLK↑	High or low	5		8		9		ns
t_h	Hold time, data after CLK↑		4		3		3		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LV574									UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			50	70		40	50		30			MHz
t_{pd}	CLK	Q		12	17		17	24			26	ns
t_{en}	$\overline{OE}$	Q		11	17		16	22			25	ns
t_{dis}	$\overline{OE}$	Q		14	19		18	27			28	ns

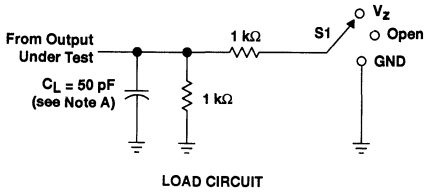
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LV574									UNIT
			V_{CC} = 5 V ± 0.5 V			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			50	70		40	50		30			MHz
t_{pd}	CLK	Q		12	17		17	24			26	ns
t_{en}	$\overline{OE}$	Q		11	17		16	22			25	ns
t_{dis}	$\overline{OE}$	Q		14	19		18	27			28	ns

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	C_L = 50 pF, f = 10 MHz	3.3 V	40	pF
		Outputs disabled			22	
		Outputs enabled		5 V	44	
		Outputs disabled			24	

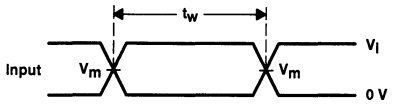
PARAMETER MEASUREMENT INFORMATION



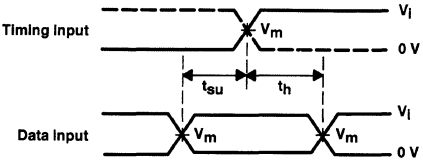
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_Z
t_{PHZ}/t_{PZH}	GND

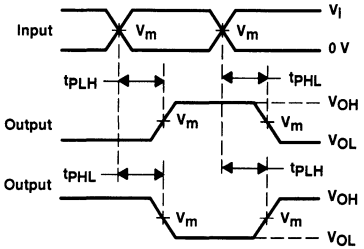
WAVEFORM CONDITION	V_{CC} = 4.5 V to 5.5 V	V_{CC} = 2.7 V to 3.6 V
V_m	0.5 × V_{CC}	1.5 V
V_I	V_{CC}	2.7 V
V_Z	2 × V_{CC}	6 V



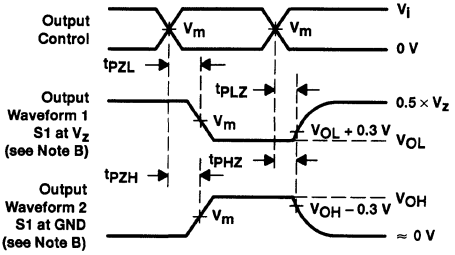
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

7 Explanation of Logic Symbols

Overview of IEEE Standard 91-1984

Explanation of Logic Symbols

Semiconductor Group

SDYZ001A

TEXAS INSTRUMENTS

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Contents

List of Tables

List of Illustrations

1 Introduction

The International Electrotechnical Commission (IEC) has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without showing explicitly the internal logic. At the heart of the system is dependency notation, which will be explained in Section 4.

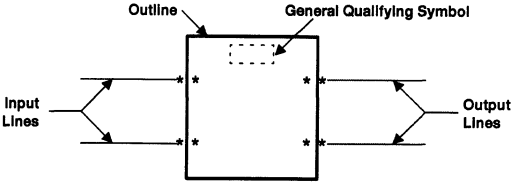
The system was introduced in the USA in a rudimentary form in IEEE/ANSI Standard Y32.14-1973. Lacking at that time a complete development of dependency notation, it offered little more than a substitution of rectangular shapes for the familiar distinctive shapes for representing the basic functions of AND, OR, negation, etc. This is no longer the case.

Internationally, Working Group 2 of IEC Technical Committee TC-3 has prepared a new document (Publication 617-12) that consolidates the original work started in the mid 1960s and published in 1972 (Publication 117-15) and the amendments and supplements that have followed. Similarly for the USA, IEEE Committee SCC 11.9 has revised the publication IEEE Std 91/ANSI Y32.14. Now numbered simply IEEE Std 91-1984, the IEEE standard contains all of the IEC work that has been approved, and also a small amount of material still under international consideration. Texas Instruments is participating in the work of both organizations and this document introduces new logic symbols in accordance with the new standards. When changes are made as the standards develop, future editions will take those changes into account.

The following explanation of the new symbolic language is necessarily brief and greatly condensed from what the standards publications will contain. This is not intended to be sufficient for those people who will be developing symbols for new devices. It is primarily intended to make possible the understanding of the symbols used in various data books, and the comparison of the symbols with logic diagrams, functional block diagrams, and/or function tables will further help that understanding.

2 Symbol Composition

A symbol comprises an outline or a combination of outlines together with one or more qualifying symbols. The shape of the symbols is not significant. As shown in Figure 1, general qualifying symbols are used to tell exactly what logical operation is performed by the elements. Table 1 shows general qualifying symbols defined in the new standards. Input lines are placed on the left and output lines are placed on the right. When an exception is made to that convention, the direction of signal flow is indicated by an arrow, as shown in Figure 1.



* Possible positions for qualifying symbols relating to inputs and outputs

Figure 1. Symbol Composition

All outputs of a single, unsubdivided element always have identical internal logic states determined by the function of the element, except when otherwise indicated by an associated qualifying symbol or label inside the element.

The outlines of elements may be abutted or embedded, in which case the following conventions apply. There is no logic connection between the elements when the line common to their outlines is in the direction of signal flow. There is at least one logic connection between the elements when the line common to their outlines is perpendicular to the direction of signal flow. The number of logic connections between elements will be clarified by the use of qualifying symbols, and this is discussed further under that topic. If no indications are shown on either side of the common line, it is assumed there is only one connection.

When a circuit has one or more inputs that are common to more than one element of the circuit, the common-control block may be used. This is the only distinctively shaped outline used in the IEC system. Figure 2 shows that, unless otherwise qualified by dependency notation, an input to the common-control block is an input to each of the elements below the common-control block.

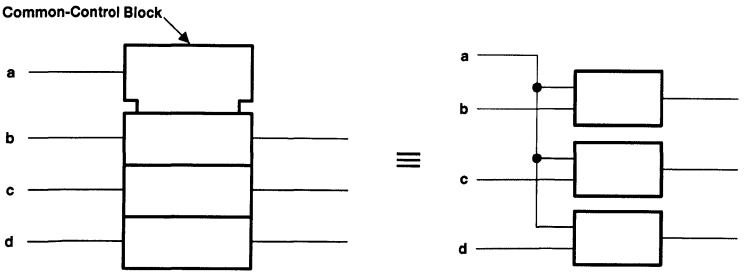
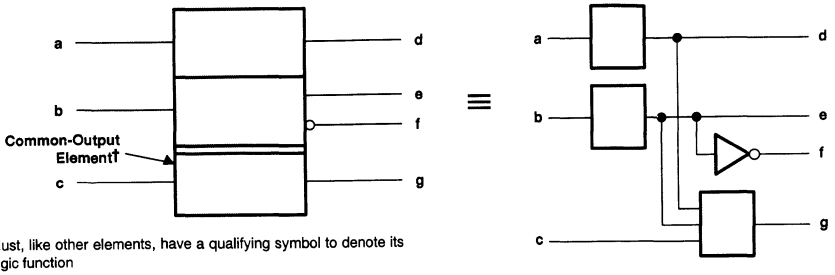


Figure 2. Common-Control Block

A common output depending on all elements of the array can be shown as the output of a common-output element. Its distinctive visual feature is the double line at its top. In addition, the common-output element may have other inputs as shown in Figure 3. The function of the common-output element must be shown by use of a general qualifying symbol.



† Must, like other elements, have a qualifying symbol to denote its logic function

Figure 3. Common-Output Element

3 Qualifying Symbols

3.1 General Qualifying Symbols

Table 1 shows general qualifying symbols defined by IEEE Standard 91. These characters are placed near the top center or the geometric center of a symbol or symbol element to define the basic function of the device represented by the symbol or of the element.

Table 1. General Qualifying Symbols†

SYMBOL	DESCRIPTION
&	AND gate or function
≥1	OR gate or function. The symbol was chosen to indicate that at least one active input is needed to activate the output.
=1	Exclusive OR. One and only one input must be active to activate the output.
=	Logic identity. All inputs must stand at the same state.
2k	An even number of inputs must be active.
2k + 1	An odd number of inputs must be active.
1	The one input must be active.
▷ or ◁	A buffer or element with more than usual output capability. Symbol is oriented in the direction of signal flow.
⨍	Schmitt trigger; element with hysteresis
X/Y	Coder, code converter (DEC/BCD, BIN/OUT, BIN/7-SEG, etc.)
MUX	Multiplexer/data selector
DMUX or DX	Demultiplexer
Σ	Adder
P–Q	Subtracter
CPG	Look-ahead carry generator
π	Multiplier
COMP	Magnitude comparator
ALU	Arithmetic logic unit
⎍	Retriggerable monostable
1 ⎍	Nonretriggerable monostable (one shot)
G ⎍⎍	Astable element. Showing waveform is optional.
!G ⎍⎍	Synchronously starting astable
G! ⎍⎍	Astable element that stops with a completed pulse
SRGm	Shift register. m = number of bits
CTRm	Counter. m = number of bits; cycle length = 2^m
CTR DIVm	Counter with cycle length = m
RCTRm	Asynchronous (ripple-carry) counter; cycle length = 2^m
ROM	Read-only memory
RAM	Random-access read/write memory
FIFO	First-in, first-out memory
I = 0	Element powers up cleared to 0 state
I = 1	Element powers up set to 1 state
Φ	Highly complex function; *gray-box* symbol with limited detail shown under special rules

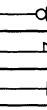
† Not all of the general qualifying symbols have been used in TI's data books, but they are included here for completeness.

3.2 Qualifying Symbols for Inputs and Outputs

Qualifying symbols for inputs and outputs are shown in Table 2 and are familiar to most users, with the possible exception of the logic polarity symbol for directly indicating active-low inputs and outputs (negation). The older logic negation indicator means that the external 0 state produces the internal 1 state. The internal 1 state means the active state. Logic negation may be used in pure logic diagrams; in order to tie the external 1 and 0 logic states to the levels high (H) and low (L), a statement of whether positive logic (1 = H, 0 = L) or negative logic (1 = L, 0 = H) is being used is required or must be assumed. Logic polarity indicators eliminate the need for calling out the logic convention and are used in various data books in the symbology for actual devices. The presence of the triangular polarity indicator indicates that the L logic level produces the internal 1 state (active state) or that, in the case of an output, the internal 1 state produces the external L level. Note how the active direction of transition for a dynamic input is indicated in positive logic, negative logic, and with polarity indication.

The internal connections between logic elements abutted together in a symbol may be indicated by the symbols shown in Table 2. Each logic connection may be shown by the presence of qualifying symbols at one or both sides of the common line and, if confusion can arise about the numbers of connections, use can be made of one of the internal connection symbols.

Table 2. Qualifying Symbols for Inputs and Outputs

SYMBOL	DESCRIPTION
	Logic negation at input. External 0 produces internal 1.
	Logic negation at output. Internal 1 produces external 0.
	Active-low input. Equivalent to in positive logic.
	Active-low output. Equivalent to in positive logic.
	Active-low input in the case of right-to-left signal flow
	Active-low output in the case of right-to-left signal flow
	Signal flow from right to left. If not otherwise indicated, signal flow is from left to right.
	Bidirectional signal flow
	Dynamic inputs active on indicated transition **Positive Logic**: 1→0 not used; not used 0→1 **Negative Logic**: 1→0 not used; not used 0→1 **Polarity Indication**: not used; H→L not used; not used L→H
	Nonlogic connection. A label inside the symbol usually defines the nature of this pin.
	Input for analog signals (on a digital symbol) (see Figure 14)
	Input for digital signals (on an analog symbol) (see Figure 14)
	Internal connection. 1 state on left produces 1 state on right.
	Negated internal connection. 1 state on left produces 0 state on right.
	Dynamic internal connection. Transition from 0 to 1 on left produces transitory 1 state on right.
	Internal input (virtual input). It always stands at its internal 1 state unless affected by an overriding dependency relationship.
	Internal output (virtual output). Its effect on an internal input to which it is connected is indicated by dependency notation.

The internal (virtual) input is an input originating somewhere else in the circuit and is not connected directly to a terminal. The internal (virtual) output is likewise not connected directly to a terminal. The application of internal inputs and outputs requires an understanding of dependency notation, which is explained in Section 4.

In an array of elements, if the same general qualifying symbol and the same qualifying symbols associated with inputs and outputs would appear inside each of the elements of the array, these qualifying symbols usually are shown only in the first element. This is done to reduce clutter and to save time in recognition. Similarly, large identical elements that are subdivided into smaller elements may each be represented by an unsubdivided outline.

3.3 Symbols Inside the Outline

Table 3 shows some symbols used inside the outline. Note particularly that open-collector (open-drain), open-emitter (open-source), and 3-state outputs have distinctive symbols. An EN input affects all the external outputs of the element in which it is placed, plus the external outputs of any elements shown to be influenced by that element. It has no effect on inputs. When an enable input affects only certain outputs, affects outputs located outside the indicated influence of the element in which the enable input is placed, and/or affects one or more inputs, a form of dependency notation indicates this (see 4.10). The effects of the EN input on the various types of outputs are shown.

It is particularly important to note that a D input is always the data input of a storage element. At its internal 1 state, the D input sets the storage element to its 1 state, and at its internal 0 state it resets the storage element to its 0 state.

The binary grouping symbol is explained more fully in Section 8. Binary-weighted inputs are arranged in order and the binary weights of the least-significant and the most-significant lines are indicated by numbers. In this document, weights of input and output lines are represented by powers of two, usually only when the binary grouping symbol is used, otherwise, decimal numbers are used. The grouped inputs generate an internal number on which a mathematical function can be performed or that can be an identifying number for dependency notation (Figure 28). A frequent use is in addresses for memories.

Reversed in direction, the binary grouping symbol can be used with outputs. The concept is analogous to that for the inputs, and the weighted outputs indicate the internal number assumed to be developed within the circuit.

Other symbols are used inside the outlines in accordance with the IEC/IEEE standards, but are not shown here. Generally, these are associated with arithmetic operations and are self-explanatory.

When nonstandardized information is shown inside an outline, it is usually enclosed in square brackets [ ]. The square brackets are omitted when associated with a nonlogic input, which is indicated by an X superimposed on the connection line outside the symbol.

Table 3. Symbols Inside the Outline

SYMBOL	DESCRIPTION
⌐|	Postponed output (of a pulse-triggered flip-flop). The output changes when input initiating change (e.g., a C input) returns to its initial external state or level (see Section 5).
—| ⎍	Bi-threshold input (input with hysteresis)
⏢|	N-P-N open-collector or similar output that can supply a relatively low-impedance L level when not turned off. Requires external pullup. Capable of positive-logic wired-AND connection.
⏢|	Passive pullup output is similar to N-P-N open-collector output but is supplemented with a built-in passive pullup.
⏛|	N-P-N open-emitter or similar output that can supply a relatively low-impedance H level when not turned off. Requires external pulldown. Capable of positive-logic wired-OR connection.
⏛|	Passive pulldown output is similar to N-P-N open-emitter output but is supplemented with a built-in passive pulldown.
▽|	3-state output
▷|	Output with more than usual output capability (symbol is oriented in the direction of signal flow)
—| EN	Enable input. When at its internal 1 state, all outputs are enabled. When at its internal 0 state, open-collector and open-emitter outputs are off, 3-state outputs are at normally defined internal logic states and at external high-impedance state, and all other outputs (e.g., totem-poles) are at the internal 0 state.
J, K, R, S	Usual meanings associated with flip-flops (e.g., R = reset to 0, S = reset to 1)
—▷ T	Toggle input causes internal state of output to change to its complement.
—| D	Data input to a storage element equivalent to: S, R
—|→ m —|← m	Shift right (left) inputs, m = 1, 2, 3, etc. If m = 1, it usually is not shown.
—| +m —| –m	Counting up (down) inputs, m = 1, 2, 3, etc. If m = 1, it usually is not shown.
0 … m	Binary grouping. m is highest power of 2.
—| CT=15	The contents-setting input, when active, causes the content of a register to take on the indicated value.
CT=9 |—	The content output is active if the content of the register is as indicated.
⎡ ⎤	Input line grouping . . . indicates two or more terminals used to implement a single logic input. X, $\overline{X}$, E
"1" |—	Fixed-state output always stands at its internal 1 state.

4 Dependency Notation

4.1 General Explanation

Dependency notation is the powerful tool that sets the IEC symbols apart from previous systems and makes compact, meaningful symbols possible. It provides the means of denoting the relationship between inputs, outputs, or inputs and outputs without actually showing all the elements and interconnections involved. The information provided by dependency notation supplements that provided by the qualifying symbols for an element's function.

In the convention for the dependency notation, the terms *affecting* and *affected* are used. In cases where it is not evident which inputs must be considered as being the affecting or the affected ones (e.g., if they stand in an AND relationship), the choice may be made in any convenient way.

So far, 11 types of dependency have been defined and all of these are used in various TI data books. X dependency is used mainly with CMOS circuits. They are listed below in the order in which they are presented and are summarized in Table 4.

SECTION	DEPENDENCY TYPE OR OTHER SUBJECT
4.2	G, AND
4.3	General Rules for Dependency Notation
4.4	V, OR
4.5	N, Negate (Exclusive-OR)
4.6	Z, Interconnection
4.7	X, Transmission
4.8	C, Control
4.9	S, Set and R, Reset
4.10	EN, Enable
4.11	M, Mode
4.12	A, Address

4.2 G (AND) Dependency

A common relationship between two signals is to have them ANDed together. This traditionally has been shown by explicitly drawing an AND gate with the signals connected to the inputs of the gate. The 1972 IEC publication and the 1973 IEEE/ANSI standard showed several ways to represent this AND relationship using dependency notation. While ten other forms of dependency have since been defined, the ways to invoke AND dependency are now reduced to one.

In Figure 4, input **b** is ANDed with input **a** and the complement of **b** is ANDed with **c**. The letter G has been chosen to indicate AND relationships and is placed at input **b**, inside the symbol. A number considered appropriate by the symbol designer (1 has been used here) is placed after the letter G and also at each affected input. Note the bar over the 1 at input **c**.

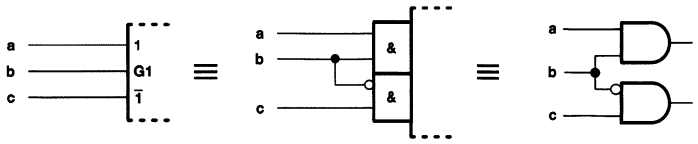


Figure 4. G Dependency Between Inputs

In Figure 5, output **b** affects input **a** with an AND relationship. The lower example shows that it is the internal logic state of **b** unaffected by the negation sign that is ANDed. Figure 6 shows input **a** to be ANDed with a dynamic input **b**.

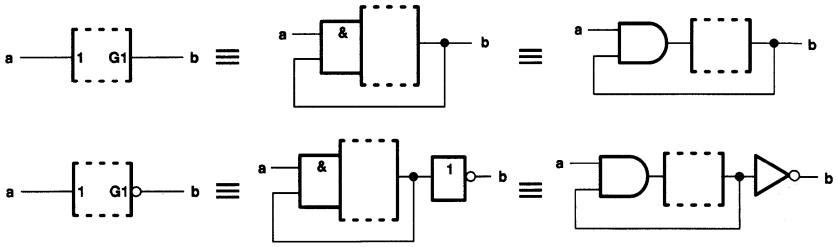


Figure 5. G Dependency Between Outputs and Inputs

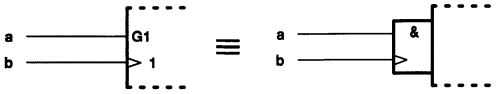


Figure 6. G Dependency With a Dynamic Input

The rules for G dependency can be summarized thus:

- When a Gm input or output (m is the number) stands at its internal 1 state, all inputs and outputs affected by Gm stand at their normally defined internal logic states.
- When the Gm input or output stands at its 0 state, all inputs and outputs affected by Gm stand at their internal 0 states.

4.3 Conventions for the Application of Dependency Notation in General

The rules for applying dependency relationships in general follow the same pattern as was illustrated for G dependency. Application of dependency notation is accomplished by:

1. labeling the input (or output) *affecting* other inputs or outputs with the letter symbol indicating the relationship involved (e.g., G for AND) followed by an identifying number, appropriately chosen, and
2. labeling each input or output *affected* by that affecting input (or output) with that same number.

If it is the complement of the internal logic state of the affecting input or output that does the affecting, then a bar is placed over the identifying numbers at the affected inputs or outputs (Figure 4).

If two affecting inputs or outputs have the same letter and same identifying number, they stand in an OR relationship to each other (Figure 7).

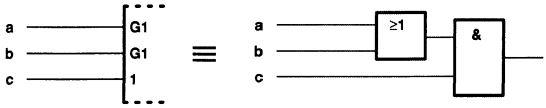


Figure 7. ORed Affecting Inputs

If the affected input or output requires a label to denote its function (e.g., D), this label is *prefixed* by the identifying number of the affecting input (Figure 15).

If an input or output is affected by more than one affecting input, the identifying numbers of each of the affecting inputs appear in the label of the affected one, separated by commas. The normal reading order of these numbers is the same as the sequence of the affecting relationships (Figure 15).

If the labels denoting the functions of affected inputs or outputs must be numbers (e.g., outputs of a coder), the identifying numbers to be associated with both affecting inputs and affected inputs or outputs are replaced by another character selected to avoid ambiguity, e.g., Greek letters (Figure 8).

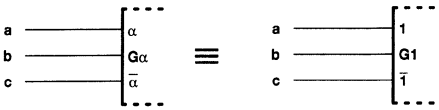


Figure 8. Substitution for Numbers

4.4 V (OR) Dependency

The symbol denoting OR dependency is the letter V (Figure 9).

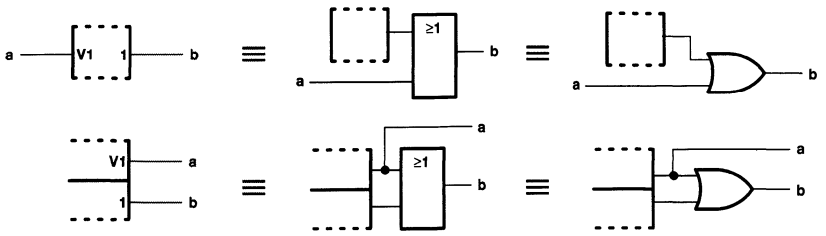


Figure 9. V (OR) Dependency

When a Vm input or output stands at its internal 1 state, all inputs and outputs affected by Vm stand at their internal 1 states. When the Vm input or output stands at its internal 0 state, all inputs and outputs affected by Vm stand at their normally defined internal logic states.

4.5 N (Negate) (Exclusive-OR) Dependency

The symbol denoting negate dependency is the letter N (Figure 10).

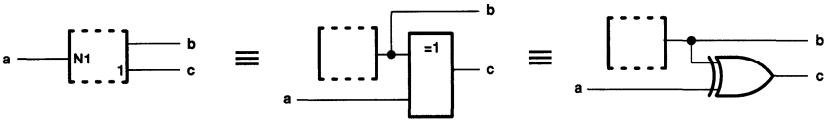


Figure 10. N (Negate) (Exclusive-OR) Dependency

Each input or output affected by an Nm input or output stands in an exclusive-OR relationship with the Nm input or output.

When an Nm input or output stands at its internal 1 state, the internal logic state of each input and each output affected by Nm is the complement of what it otherwise would be. When an Nm input or output stands at its internal 0 state, all inputs and outputs affected by Nm stand at their normally defined internal logic states.

4.6 Z (Interconnection) Dependency

The symbol denoting interconnection dependency is the letter Z.

Interconnection dependency is used to indicate the existence of internal logic connections between inputs, outputs, internal inputs, and/or internal outputs.

The internal logic state of an input or output affected by a Zm input or output is the same as the internal logic state of the Zm input or output, unless modified by additional dependency notation (Figure 11).

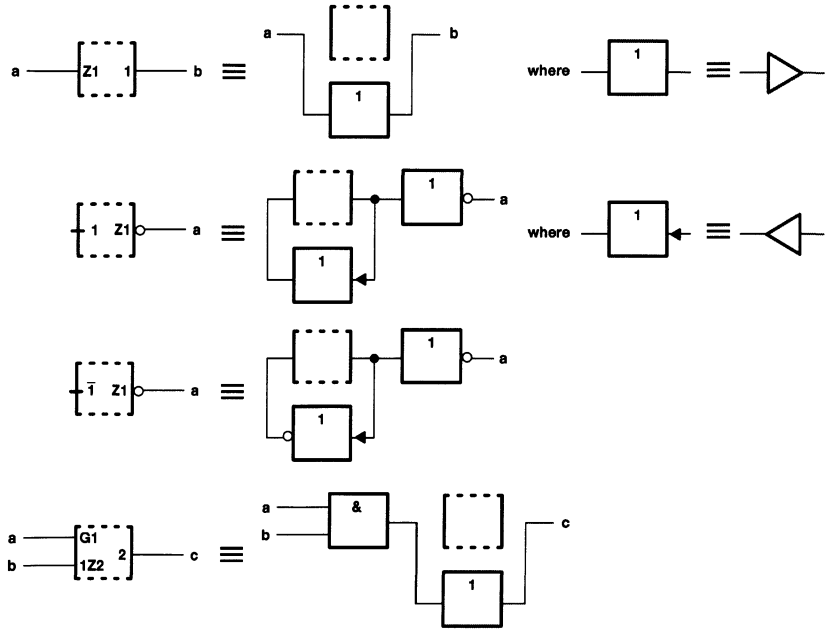


Figure 11. Z (Interconnection) Dependency

4.7 X (Transmission) Dependency

The symbol denoting transmission dependency is the letter X.

Transmission dependency is used to indicate controlled bidirectional connections between affected input/output ports (Figure 12).

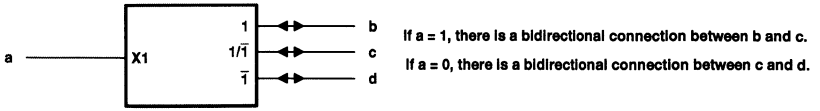


Figure 12. X (Transmission) Dependency

When an Xm input or output stands at its internal 1 state, all I/O ports affected by this Xm input or output are bidirectionally connected and stand at the same internal logic state or analog signal level. When an Xm input or output stands at its internal 0 state, the connection associated with this set of dependency notation does not exist.

Although the transmission paths represented by X dependency are inherently bidirectional, use is not always made of this property. This is analogous to a piece of wire, that may be constrained to carry current in only one direction. If this is the case in a particular application, then the directional arrows shown in Figures 12, 13, and 14 would be omitted.

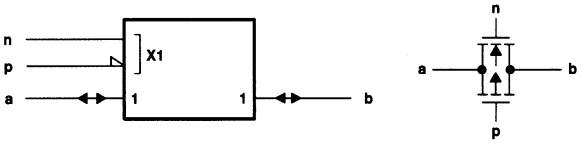


Figure 13. CMOS Transmission Gate Symbol and Schematic

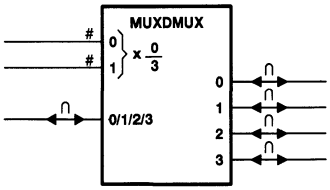


Figure 14. Analog Data Selector (Multiplexer/Demultiplexer)

4.8 C (Control) Dependency

The symbol denoting control dependency is the letter C.

Control inputs typically are used to enable or disable the data (D, J, K, R, or S) inputs of storage elements. They may take on their internal 1 states (be active) either statically or dynamically. In the latter case, the dynamic input symbol is used as shown in the third example of Figure 15.

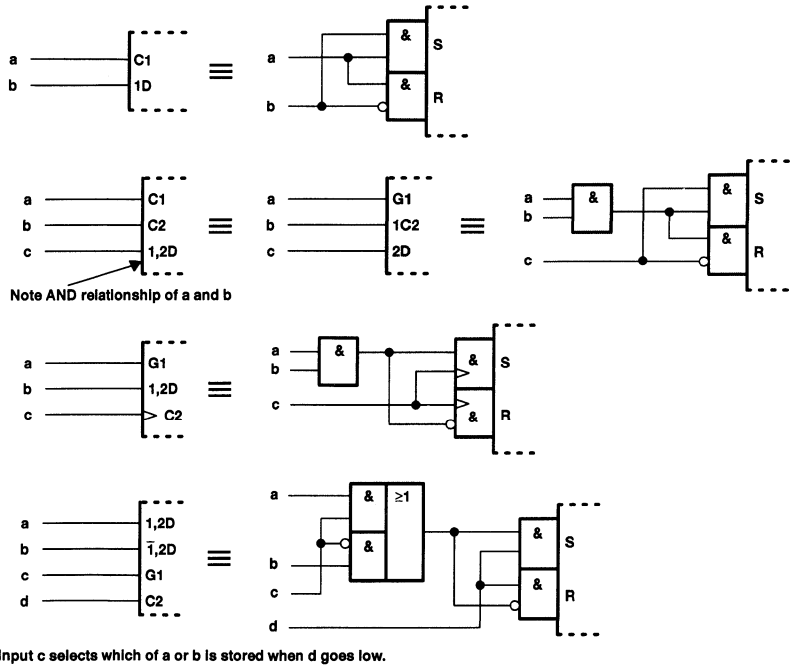


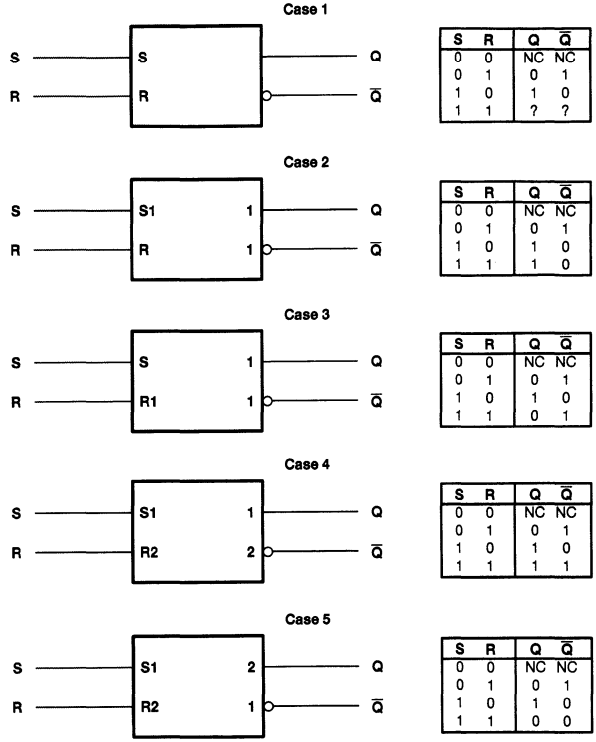
Figure 15. C (Control) Dependency

When a Cm input or output stands at its internal 1 state, the inputs affected by Cm have their normally defined effect on the function of the element, i.e., these inputs are enabled. When a Cm input or output stands at its internal 0 state, the inputs affected by Cm are disabled and have no effect on the function of the element.

4.9 S (Set) and R (Reset) Dependencies

The symbol denoting set dependency is the letter S. The symbol denoting reset dependency is the letter R.

Set and reset dependencies are used if it is necessary to specify the effect of the combination R = S = 1 on a bistable element. Case 1 in Figure 16 does not use S or R dependency.



S	R	Q	$\overline{Q}$
0	0	NC	NC
0	1	0	1
1	0	1	0
1	1	?	?

S	R	Q	$\overline{Q}$
0	0	NC	NC
0	1	0	1
1	0	1	0
1	1	1	0

S	R	Q	$\overline{Q}$
0	0	NC	NC
0	1	0	1
1	0	1	0
1	1	0	1

S	R	Q	$\overline{Q}$
0	0	NC	NC
0	1	0	1
1	0	1	0
1	1	1	1

S	R	Q	$\overline{Q}$
0	0	NC	NC
0	1	0	1
1	0	1	0
1	1	0	0

0 = external 0 state, 1 = external 1 state, NC = no change, ? = unspecified

Figure 16. S (Set) and R (Reset) Dependencies

When an Sm input is at its internal 1 state, outputs affected by the Sm input react, regardless of the state of an R input, as they normally would react to the combination S = 1, R = 0. See cases 2, 4, and 5 in Figure 16.

When an Rm input is at its internal 1 state, outputs affected by the Rm input react, regardless of the state of an S input, as they normally would react to the combination S = 0, R = 1. See cases 3, 4, and 5 in Figure 16.

When an Sm or Rm input is at its internal 0 state, it has no effect.

Note that the noncomplementary output patterns in cases 4 and 5 are only pseudo stable. The simultaneous return of the inputs to S = R = 0 produces an unforeseeable stable and complementary output pattern.

4.10 EN (Enable) Dependency

The symbol denoting enable dependency is the combination of letters EN.

The ENm input has the same effect on outputs as an EN input, see 3.1, but it affects only those outputs labeled with the identifying number m. It also affects those inputs labeled with the identifying number m. By contrast, an EN input affects all outputs and no inputs. The effect of an ENm input on an affected input is identical to that of a Cm input (Figure 17).

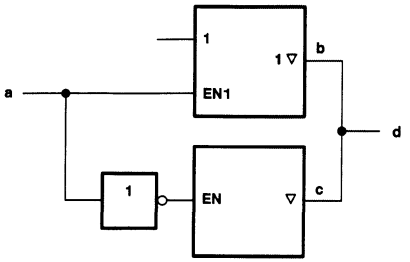


Figure 17. EN (Enable) Dependency

When an ENm input stands at its internal 1 state, the inputs affected by ENm have their normally defined effect on the function of the element and the outputs affected by this input stand at their normally defined internal logic states, i.e., these inputs and outputs are enabled.

When an ENm input stands at its internal 0 state, the inputs affected by ENm are disabled and have no effect on the function of the element, and the outputs affected by ENm are also disabled. Open-collector outputs are turned off, 3-state outputs stand at their normally defined internal logic states but externally exhibit high impedance, and all other outputs (e.g., totem-pole outputs) stand at their internal 0 states.

4.11 M (Mode) Dependency

The symbol denoting mode dependency is the letter M.

Mode dependency is used to indicate that the effects of particular inputs and outputs of an element depend on the mode in which the element is operating.

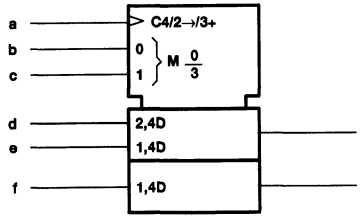
If an input or output has the same effect in different modes of operation, the identifying numbers of the relevant affecting Mm inputs will appear in the label of that affected input or output between parentheses and separated by solidi (Figure 22).

4.11.1 M Dependency Affecting Inputs

M dependency affects inputs the same as C dependency. When an Mm input or Mm output stands at its internal 1 state, the inputs affected by this Mm input or Mm output have their normally defined effect on the function of the element, i.e., the inputs are enabled.

When an Mm input or Mm output stands at its internal 0 state, the inputs affected by this Mm input or output have no effect on the function of the element. When an affected input has several sets of labels separated by solidi (e.g., C4/2→/3+), any set in which the identifying number of the Mm input or Mm output appears has no effect and is to be ignored. This represents disabling of some of the functions of a multifunction input.

The circuit in Figure 18 has two inputs, **b** and **c**, that control which one of four modes (0, 1, 2, or 3) will exist at any time. Inputs **d**, **e**, and **f** are D inputs subject to dynamic control (clocking) by the **a** input. The numbers 1 and 2 are in the series chosen to indicate the modes so inputs **e** and **f** are only enabled in mode 1 (for parallel loading) and input **d** is only enabled in mode 2 (for serial loading). Note that input **a** has three functions. It is the clock for entering data. In mode 2, it causes right shifting of data, which means a shift away from the control block. In mode 3, it causes the contents of the register to be incremented by one count.



Note that all operations are synchronous.

In mode 0 (b = 0, c = 0), the outputs remain at their existing states as none of the inputs has an effect.

In mode 1 (b = 1, c = 0), parallel loading takes place through inputs e and f.

In mode 2 (b = 0, c = 1), shifting down and serial loading through input d take place.

In mode 3 (b = c = 1), counting up by increment of one per clock pulse takes place.

Figure 18. M (Mode) Dependency Affecting Inputs

4.11.2 M Dependency Affecting Outputs

When an Mm input or output stands at its internal 1 state, the affected outputs stand at their normally defined internal logic states, i.e., the outputs are enabled.

When an Mm input or output stands at its internal 0 state, at each affected output any set of labels containing the identifying number of the Mm input or Mm output has no effect and is to be ignored. When an output has several different sets of labels separated by solidi (e.g., 2,4/3,5), only those sets in which the identifying number of this Mm input or Mm output appears are to be ignored.

Figure 19 shows a symbol for a device whose output can behave like either a 3-state output or an open-collector output, depending on the signal applied to input **a**. Mode 1 exists when input **a** stands at its internal 1 state and, in that case, the 3-state symbol applies and the open-element symbol has no effect. When **a** = 0, mode 1 does not exist, so the 3-state symbol has no effect and the open-element symbol applies.

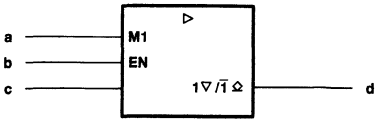


Figure 19. Type of Output Determined by Mode

In Figure 20, if input **a** stands at its internal 1 state, establishing mode 1, output **b** stands at its internal 1 state only when the content of the register equals 9. Since output **b** is located in the common-control block with no defined function outside of mode 1, the state of this output outside of mode 1 is not defined by the symbol.

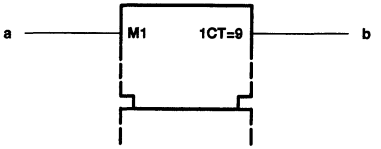


Figure 20. An Output of the Common-Control Block

In Figure 21, if input **a** stands at its internal 1 state, establishing mode 1, output **b** stands at its internal 1 state only when the content of the register equals 15. If input **a** stands at its internal 0 state, output **b** stands at its internal 1 state only when the content of the register equals 0.

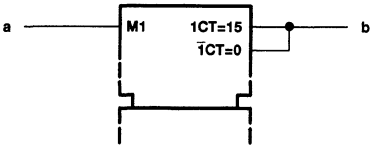


Figure 21. Determining an Output's Function

In Figure 22, inputs **a** and **b** are binary weighted to generate the numbers 0, 1, 2, or 3. This determines which one of the four modes exists.

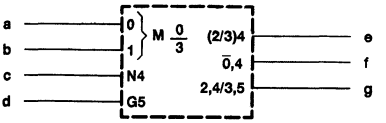


Figure 22. Dependent Relationships Affected by Mode

At output **e**, the label set causing negation (if **c** = 1) is effective only in modes 2 and 3. In modes 0 and 1, this output stands at its normally defined state as if it had no labels. At output **f**, the label set has effect when the mode is not 0, so output **e** is negated (if **c** = 1) in modes 1, 2, and 3. In mode 0, the label set has no effect, so the output stands at its normally defined state. In this example, 0̄,4 is equivalent to (1/2/3)4. At output **g** there are two label sets. The first set, causing negation (if **c** = 1), is effective only in mode 2. The second set, subjecting **g** to AND dependency on **d**, has effect only in mode 3.

Note that in mode 0 none of the dependency relationships has any effect on the outputs, so **e**, **f**, and **g** stand at the same state.

4.12 A (Address) Dependency

The symbol denoting address dependency is the letter A.

Address dependency provides a clear representation of those elements, particularly memories, that use address control inputs to select specified sections of multidimensional arrays. Such a section of a memory array usually is called a word. The purpose of address dependency is to allow a symbolic presentation of the entire array. An input of the array shown at a particular element of this general section is common to the corresponding elements of all selected sections of the array. An output of the array shown at a particular element of this general section is the result of the OR function of the outputs of the corresponding elements of selected sections.

Inputs that are not affected by any affecting address input have their normally defined effect on all sections of the array, whereas, inputs affected by an address input have their normally defined effect only on the section selected by that address input.

An affecting address input is labeled with the letter A, followed by an identifying number that corresponds with the address of the particular section of the array selected by this input. Within the general section presented by the symbol, inputs and outputs affected by an Am input are labeled with the letter A, which stands for the identifying numbers, i.e., the addresses of the particular sections.

Figure 23 shows a 3-word by 2-bit memory having a separate address line for each word, and uses EN dependency to explain the operation. To select word 1, input **a** is taken to its 1 state, which establishes mode 1. Data can now be clocked in the inputs marked 1,4D. Unless words 2 and 3 are also selected, data cannot be clocked in at the inputs marked 2,4D and 3,4D. The outputs will be the OR functions of the selected outputs, i.e., only those enabled by the active EN functions.

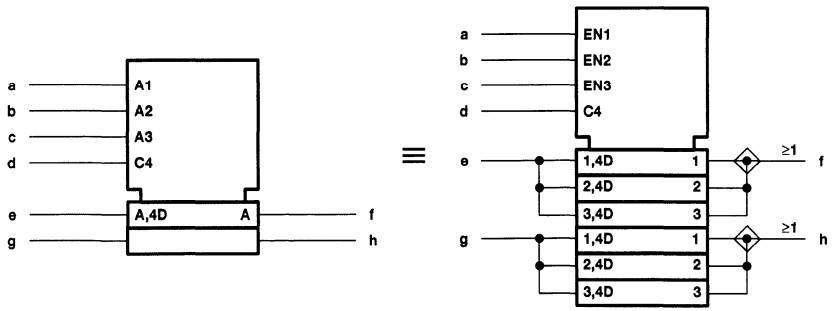


Figure 23. A (Address) Dependency

The identifying numbers of affecting address inputs correspond with the addresses of the sections selected by these inputs. They need not necessarily differ from those of other affecting dependency inputs (e.g., G, V, N, . . .) because in the general section presented by the symbol they are replaced by the letter A.

If there are several sets of affecting Am inputs for the purpose of independent and possibly simultaneous access to sections of the array, then the letter A is modified to 1A, 2A, etc. Because they have access to the same sections of the array, these sets of A inputs may have the same identifying numbers.

Figure 24 is another illustration of the concept.

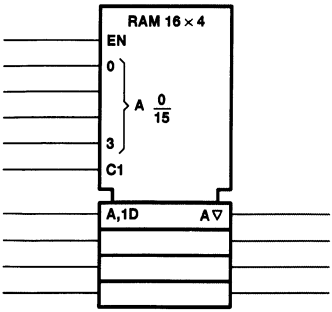


Figure 24. Array of 16 Sections of Four Transparent Latches With 3-State Outputs Comprising a 16-Word × 4-Bit Random-Access Memory

Table 4. Summary of Dependency Notation

TYPE OF DEPENDENCY	LETTER SYMBOL†	AFFECTING INPUT AT ITS 1 STATE	AFFECTING INPUT AT ITS 0 STATE
Address	A	Permits action (address selected)	Prevents action (address not selected)
Control	C	Permits action	Prevents action
Enable	EN	Permits action	Prevents action of inputs ◇outputs off ▽outputs at external high impedance, no change in internal logic state. Other outputs at internal 0 state.
AND	G	Permits action	Imposes 0 state
Mode	M	Permits action (mode selected)	Prevents action (mode not selected)
Negate (Exclusive-OR)	N	Complements state	No effect
Reset	R	Affected output reacts as it would to S = 0, R = 1	No effect
Set	S	Affected output reacts as it would to S = 1, R = 0	No effect
OR	V	Imposes 1 state	Permits action
Transmission	X	Bidirectional connection exists	Bidirectional connection does not exist
Interconnection	Z	Imposes 1 state	Imposes 0 state

† These letter symbols appear at the *affecting* input (or output) and are followed by a number. Each input (or output) *affected* by that input is labeled with that same number. When the labels EN, R, and S appear at inputs without the following numbers, the descriptions above do not apply. The action of these inputs is described under Section 3.3.

5 Bistable Elements

The dynamic input symbol, the postponed output symbol, and dependency notation provide the tools to differentiate four main types of bistable elements and make synchronous and asynchronous inputs easily recognizable (Figure 25). The first column shows the essential distinguishing features; the other columns show examples.

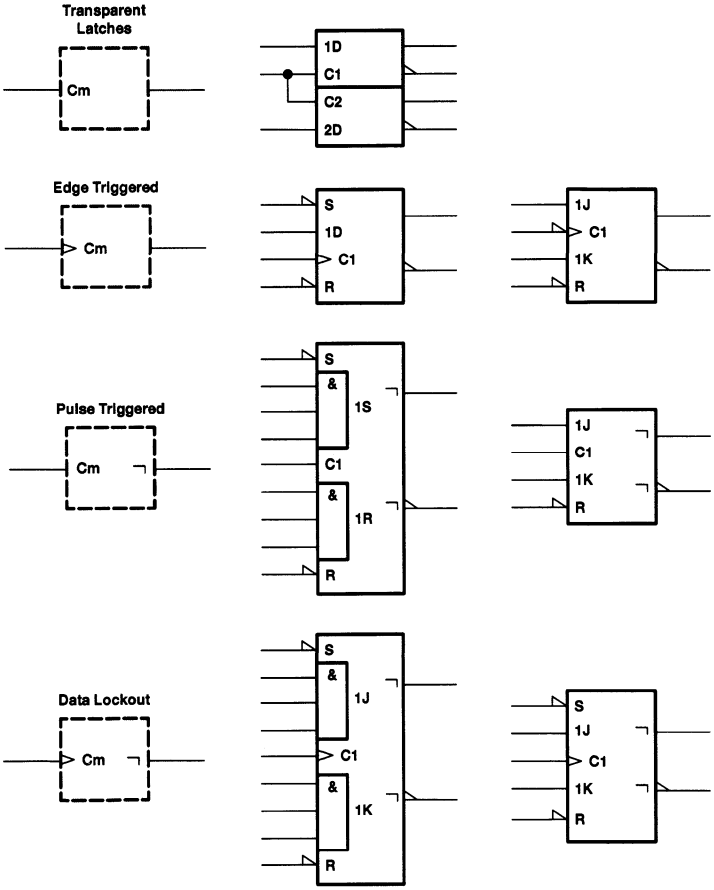


Figure 25. Four Types of Bistable Circuits

Transparent latches have a level-operated control input. The D input is active as long as the C input is at its internal 1 state. The outputs respond immediately. Edge-triggered elements accept data from D, J, K, R, or S inputs on the active transition of C. Pulse-triggered elements require the setup of data before the start of the control pulse; the C input is considered static since the data must be maintained as long as C is at its 1 state. The output is postponed until C returns to its 0 state. The data lock-out element is similar to the pulse-triggered version except that the C input is considered dynamic, in that shortly after C goes through its active transition, the data inputs are disabled and data does not have to be held. However, the output is still postponed until the C input returns to its initial external level.

Notice that synchronous inputs can be readily recognized by their dependency labels (1D, 1J, 1K, 1S, 1R) compared to the asynchronous inputs (S, R), which are not dependent on the C inputs.

6 Coders

The general symbol for a coder or code converter is shown in Figure 26. X and Y may be replaced by appropriate indications of the code used to represent the information at the inputs and at the outputs, respectively.

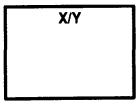


Figure 26. Coder General Symbol

Indication of code conversion is based on the following rule:

> Depending on the input code, the internal logic states of the inputs determine an internal value. This value is reproduced by the internal logic states of the outputs, depending on the output code.

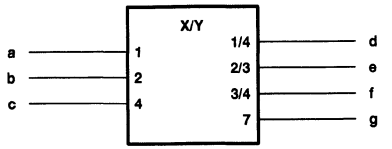
The indication of the relationships between the internal logic states of the inputs and the internal value is accomplished by:

1. labeling the inputs with numbers. In this case the internal value equals the sum of the weights associated with those inputs that stand at their internal 1 state, or by
2. replacing X by an appropriate indication of the input code and labeling the inputs with characters that refer to this code.

The relationships between the internal value and the internal logic states of the outputs are indicated by:

1. labeling each output with a list of numbers representing those internal values that lead to the internal 1 state of that output. These numbers shall be separated by solidi, as shown in Figure 27. This labeling may also be applied when Y is replaced by a letter denoting a type of dependency (see Section 7). If a continuous range of internal values produces the internal 1 state of an output, this can be indicated by two numbers that are inclusively the beginning and the end of the range, with these two numbers separated by three dots (e.g., 4 . . . 9 = 4/5/6/7/8/9) or by
2. replacing Y by an appropriate indication of the output code and labeling the outputs with characters that refer to this code, as shown in Figure 28.

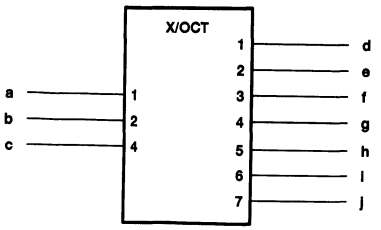
Alternatively, the general symbol may be used, together with an appropriate reference to a table, in which the relationship between the inputs and outputs is indicated. This is a recommended way to symbolize a PROM after it has been programmed.



FUNCTION TABLE

INPUTS			OUTPUTS			
c	b	a	g	f	e	d
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	1	0
0	1	1	0	1	1	0
1	0	0	0	1	0	1
1	0	1	0	0	0	0
1	1	0	0	0	0	0
1	1	1	1	0	0	0

Figure 27. An X/Y Code Converter



FUNCTION TABLE

INPUTS			OUTPUTS						
c	b	a	j	i	h	g	f	e	d
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	0
0	1	1	0	0	0	0	1	0	0
1	0	0	0	0	0	1	0	0	0
1	0	1	0	0	1	0	0	0	0
1	1	0	0	1	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0

Figure 28. An X/Octal Code Converter

7 Use of a Coder to Produce Affecting Inputs

It often occurs that a set of affecting inputs for dependency notation is produced by decoding the signals on certain inputs to an element. In such a case, use can be made of the symbol for a coder as an embedded symbol (Figure 29).

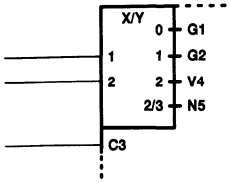


Figure 29. Producing Various Types of Dependencies

If all affecting inputs produced by a coder are of the same type and their identifying numbers are shown at the outputs of the coder, Y (in the qualifying symbol X/Y) may be replaced by the letter denoting the type of dependency. The indications of the affecting inputs should then be omitted (Figure 30).

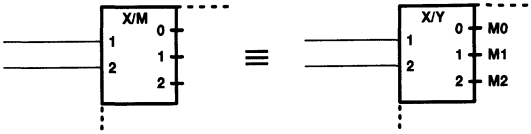


Figure 30. Producing One Type of Dependency

8 Use of Binary Grouping to Produce Affecting Inputs

If all affecting inputs produced by a coder are of the same type and have consecutive identifying numbers not necessarily corresponding with the numbers that would have been shown at the outputs of the coder, use can be made of the binary grouping symbol. k external lines effectively generate 2^k internal inputs. The bracket is followed by the letter denoting the type of dependency, followed by m1/m2. The m1 is to be replaced by the smallest identifying number and the m2 by the largest one, as shown in Figure 31.

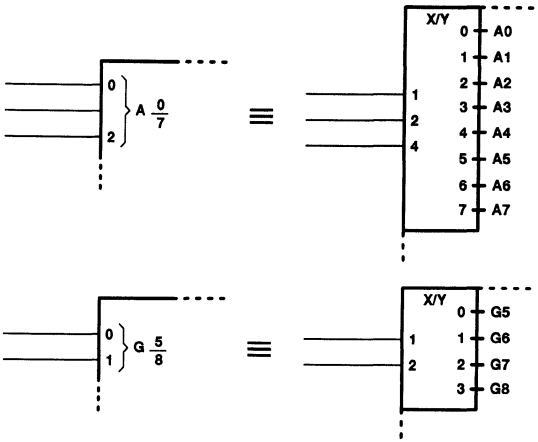


Figure 31. Use of the Binary Grouping Symbol

9 Sequence of Input Labels

If an input having a single functional effect is affected by other inputs, the qualifying symbol (if there is any) for that functional effect is preceded by the labels corresponding to the affecting inputs. The left-to-right order of these preceding labels is the order in which the effects or modifications must be applied. The affected input has no functional effect on the element if the logic state of any one of the affecting inputs, considered separately, would cause the affected input to have no effect, regardless of the logic states of other affecting inputs.

If an input has several different functional effects or has several different sets of affecting inputs, depending on the mode of action, the input may be shown as often as required. However, there are cases in which this method of presentation is not advantageous. In those cases the input may be shown once with the different sets of labels separated by solidi (Figure 32). No meaning is attached to the order of these sets of labels. If one of the functional effects of an input is that of an unlabeled input to the element, a solidus precedes the first set of labels shown.

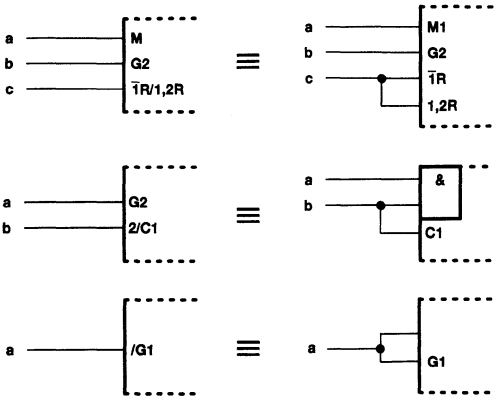


Figure 32. Input Labels

If all inputs of a combinational element are disabled (caused to have no effect on the function of the element), the internal logic states of the outputs of the element are not specified by the symbol. If all inputs of a sequential element are disabled, the content of this element is not changed and the outputs remain at their existing internal logic states.

Labels may be factored using algebraic techniques (Figure 33).

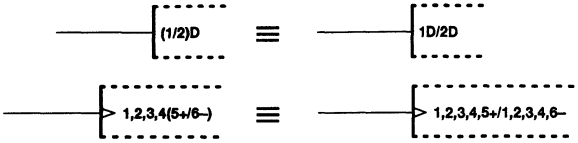


Figure 33. Factoring Input Labels

10 Sequence of Output Labels

If an output has a number of different labels, regardless of whether they are identifying numbers of affecting inputs or outputs or not, these labels are shown in the following order:

1. If the postponed output symbol has to be shown, this comes first, if necessary, preceded by the indications of the inputs to which it must be applied
2. Followed by the labels indicating modifications of the internal logic state of the output, such that the left-to-right order of these labels corresponds with the order in which their effects must be applied
3. Followed by the label indicating the effect of the output on inputs and other outputs of the element.

Symbols for open circuit or 3-state outputs, where applicable, are placed just inside the outside boundary of the symbol, adjacent to the output line (Figure 34).

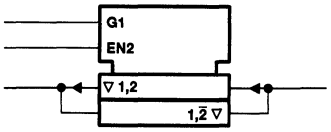


Figure 34. Placement of 3-State Symbols

If an output needs several different sets of labels that represent alternative functions (e.g., depending on the mode of action), these sets may be shown on different output lines that must be connected outside the outline. However, there are cases in which this method of presentation is not advantageous. In those cases, the output may be shown once, with the different sets of labels separated by solidi (Figure 35).

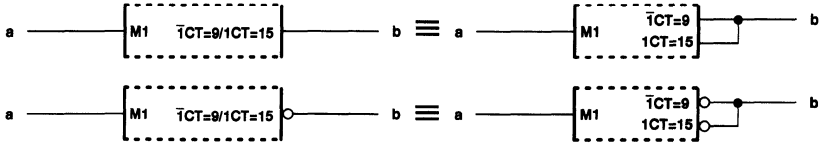


Figure 35. Output Labels

Two adjacent identifying numbers of affecting inputs in a set of labels that are not already separated by a nonnumeric character should be separated by a comma.

If a set of labels of an output not containing a solidus contains the identifying number of an affecting Mm input standing at its internal 0 state, this set of labels has no effect on that output.

Labels may be factored using algebraic techniques (Figure 36).

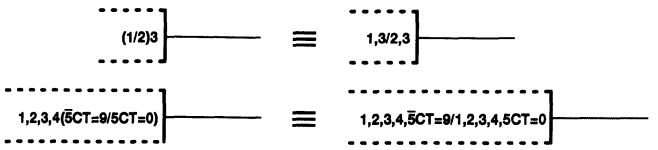


Figure 36. Factoring Output Labels

Contents

HCMOS Design Information

SCLA007
April 1996

TEXAS INSTRUMENTS

Contents

Contents (continued)

List of Illustrations

List of Illustrations (continued)

Tables

Introduction

Present HCMOS data sheets specify, under recommended operating conditions, input t_t = 1000 ns, (10%–90%) for V_{CC} = 2 V. If certain devices are used in the threshold region (from V_{IL}max = 0.5 V to V_{IH}min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V will not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

Devices susceptible to the above condition are: HC112, HC161, HC163, HC164, HC165, HC166, HC191, HC193, HC393, HC590A, and HC4040.

HCMOS Designer's Information

CMOS Circuitry

The elementary CMOS building blocks are the inverter and the transmission gate. Each uses a complementary pair of one N-channel and one P-channel enhancement-type field-effect transistor. Figures 1 and 2 show these together with various logic symbols[1] used to represent them.

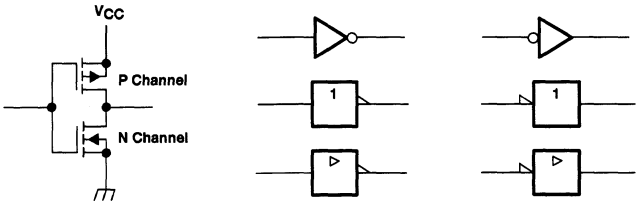


Figure 1. Inverters

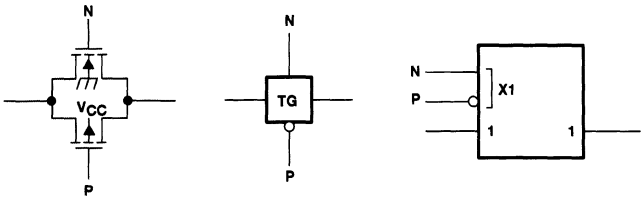


Figure 2. Transmission Gates

[1] The various logic symbols are equivalent. The distinctive-shape form of the inverter and gate symbols and the "TG" form of the transmission gate are typically used in the device logic diagrams. The logic inversion symbol (○) is shown at the input or the output, whichever maintains logical consistency with the driving output or the driven input. This technique is used to indicate the true/complement levels of the signal as it progresses through the circuit. For example, refer to Figure 7 in this section. The rectangular forms of the inverter and gate symbols and the polarity indicator (⊏) replacing the inversion symbol are usually used in this book only in the device logic symbols. The ▷ indicates a high-current output.

Logic gates are created by adding transistors in parallel or series to the transistors making up the elementary inverter. Thus, the simplest gates are inverting (see Figure 3). An odd number of additional inverters are sometimes added to the outputs of gates to make them noninverting. Basic CMOS gates usually have no more than three inputs. Arrays of gates are used when more than three signals are ANDed or ORed.

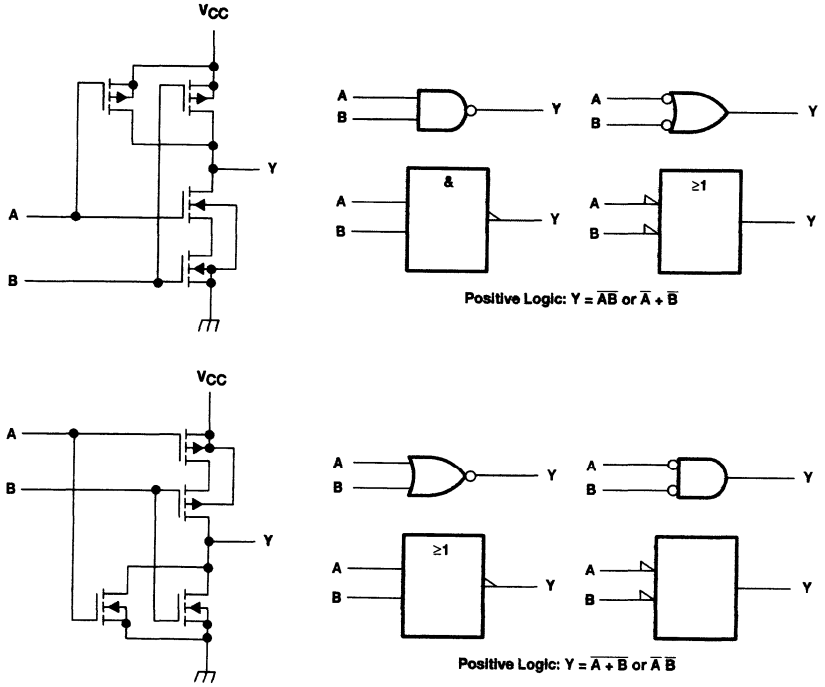


Figure 3. Gates

The exclusive-OR or exclusive-NOR gate is most easily implemented using two inverters and two transmission gates as shown in Figure 4. In complex chains of gates, the inverters can be made unnecessary by complementary signals that are already available.

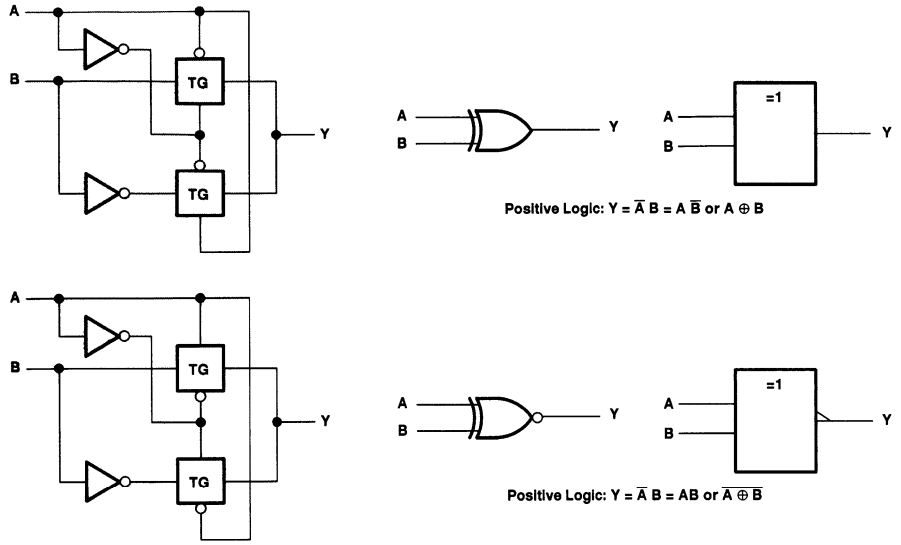


Figure 4. Exclusive-OR/NOR Gates

The 3-state output buffer has logic elements in the gate connections to each of the transistors in the final inverter so that both can be turned off under the control of an enable function. Figure 5 illustrates an inverting output buffer.

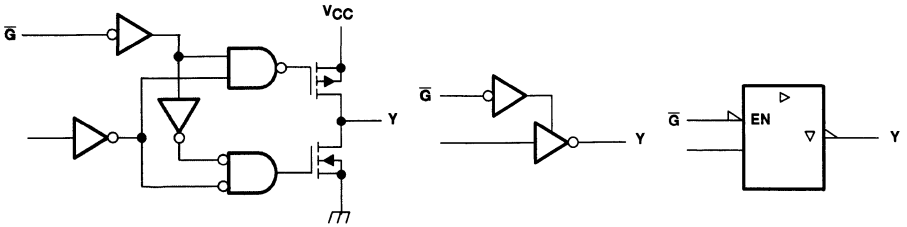


Figure 5. Inverting 3-State Output Buffer With Active-Low Enable

The transparent latch typically is implemented as shown in Figure 6. This is the simplest form. Logic diagrams show that additional inverters can be added as buffers or to optimize timing. The true and complementary outputs (Q and $\overline{Q}$) may be taken off at other points. Outputs brought out to terminals are always buffered to minimize any feedback effects. The exception to this is the HCU device, which has unbuffered outputs.

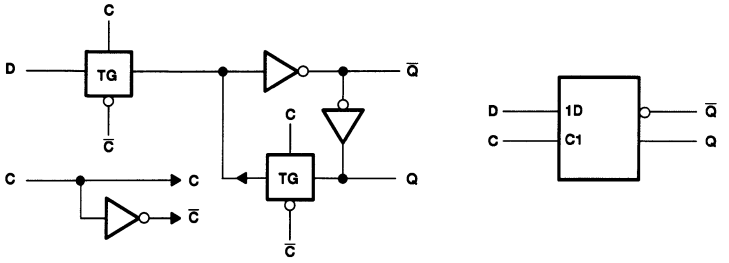


Figure 6. Transparent Latches

Putting two transparent latches in series produces an edge-triggered D-type flip-flop. Inverters can be converted to 2-input gates to provide asynchronous set and reset functions. Figure 7 illustrates a negative-edge-triggered circuit. Exchanging the connections of C and $\overline{C}$ produces a positive-edge-triggered version.

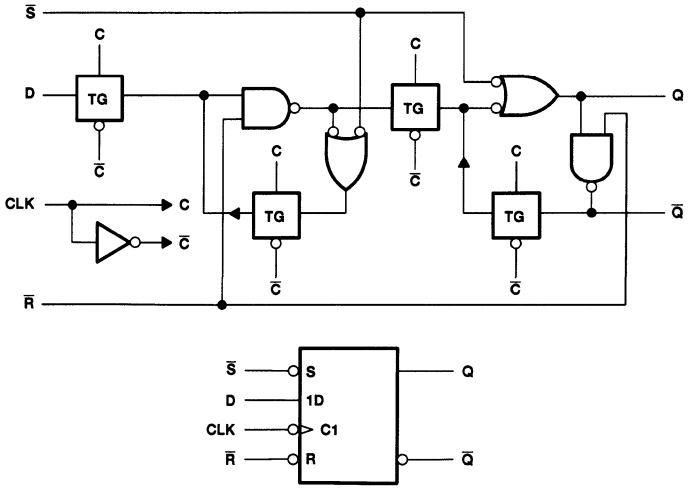


Figure 7. Negative-Edge-Triggered D-Type Flip-Flops

Detailed logic diagrams for flip-flops are given in the data sheets, when useful, to illustrate special features such as synchronous clearing, J/K inputs, and toggle enabling.

In general, the logic diagrams have been simplified. They indicate the logic implementation, but should not be used to predict dynamic performance. Inverters existing in series can be combined or eliminated in the diagrams, as shown in Figure 8.

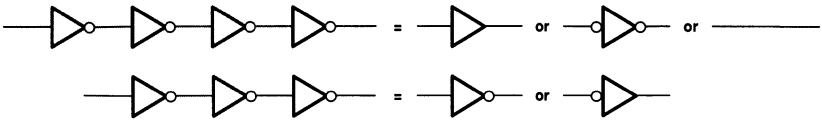


Figure 8. Simplification of Diagrams by Combining Inverters

High-Speed CMOS Characteristics

Table 1 compares the main characteristics of the high-speed CMOS family with those of standard TTL, LS, S, ALS, AS, and metal-gate CMOS.

Table 1. Performance Comparison of High-Speed CMOS With Several Other Logic Families

TECHNOLOGY†	SILICON-GATE CMOS	AHC	METAL-GATE CMOS	STD TTL	LOW-POWER SCHOTTKY TTL	ADVANCED LOW-POWER SCHOTTKY TTL	ADVANCED SCHOTTKY TTL
Device series	SN74HC		4000	SN74	SN74LS	SN74ALS	SN74AS
Power dissipation per gate (mW)							
Static	0.0000025	0.00009	0.001	10	2	1	8.5
At 100 kHz	0.17	0.006	0.1	10	2	1	8.5
Propagation delay time (ns) (C_L = 15 pF)	8	3.7	105	10	10	4	1.5
Maximum clock frequency (MHz) (C_L = 15 pF)	40	130	12	35	40	70	200
Minimum output drive (mA) (V_O = 0.4 V)							
Standard outputs	4	8	1.6	16	8	8	20
High-current outputs	6	8	1.6	48	24	24/48	48/64
Fan-out (LS loads)							
Standard outputs	10	20	4	40	20	20	50
High-current outputs	15	20	4	120	60	60/120	120/160
Maximum input current, I_{IL} (mA) (V_I = 0.4 V)	±0.001	±0.001	−0.001	−1.6	−0.4	−0.1	−0.5

† Family characteristics at 25°C, V_{CC} = 5 V; all values typical unless otherwise noted. This table is provided for broad comparisons only. Parameters for specific devices within a family may vary. For detailed comparisons, please consult the appropriate data book.

The major advantages of high-speed CMOS can be summarized as follows:

1. The high-speed CMOS family can operate at speeds comparable to LS. The high-speed CMOS family has ac parameters guaranteed at a supply voltage of 2 V, 4.5 V, and 6 V over the full operating temperature range into a 50-pF load (also, 150 pF for high-current outputs). Note that at the higher operating frequencies, the power consumption is also comparable to LS (see Figure 9).
2. Figure 9 also shows that the high-speed CMOS family covers a wide range of applications: low-power drain for low-speed systems and a slightly higher drain for higher-speed systems.

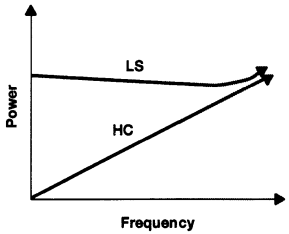


Figure 9. Power Consumed Versus Frequency for High-Speed CMOS Compared to LS

3. Minimum system power. Only the gates that are switching contribute to system power consumption. This reduces the size of the power supply required, resulting in lower system cost and improved reliability through lower heat dissipation.

   As mentioned previously, the power consumption for an individual gate at the maximum speed is comparable to LS. However, in typical systems, only a fraction of the gates are switching at the clock frequency; therefore, significant power savings can be realized. On a system level where the individual gate switching frequencies are distributed between zero and the system clock frequency (see Figure 10), the power saved with high-speed CMOS can be quite significant, as shown in Figure 11. The total system power is the area under each curve. The graph in Figure 11 is obtained by multiplying the individual gate characteristics (see Figure 9) by the frequency distribution in Figure 10.

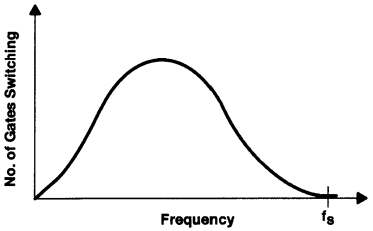


Figure 10. Typical Distribution of Switching Frequencies for Gates Within a System With Maximum Clock Frequency, f_S

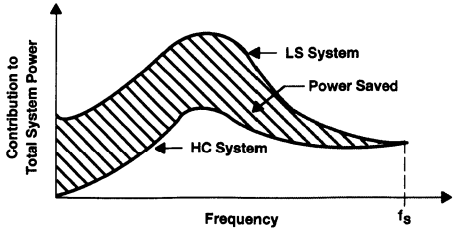


Figure 11. Contribution to Total Power by Gates Running at Frequencies From 0 to f_S

4. High-speed CMOS is ideal for battery-operated systems or systems requiring battery backup because there is virtually no static power dissipation (see Figure 9).

5. Improved noise immunity over bipolar devices is due to the rail-to-rail (V_{CC} to ground) output voltage swings. Figure 12 illustrates the noise immunity provided by the high-speed CMOS family as it compares to the LS family. This noise immunity makes it ideal for high-noise environments. Minimum and maximum output voltages are guaranteed at 4 mA (6 mA for high-current devices). If the output currents exceed these limits, the noise immunity will be impaired. HCT devices have input noise margins similar to LS because their inputs are TTL-voltage compatible. The outputs of HCT are the same as standard HC outputs.

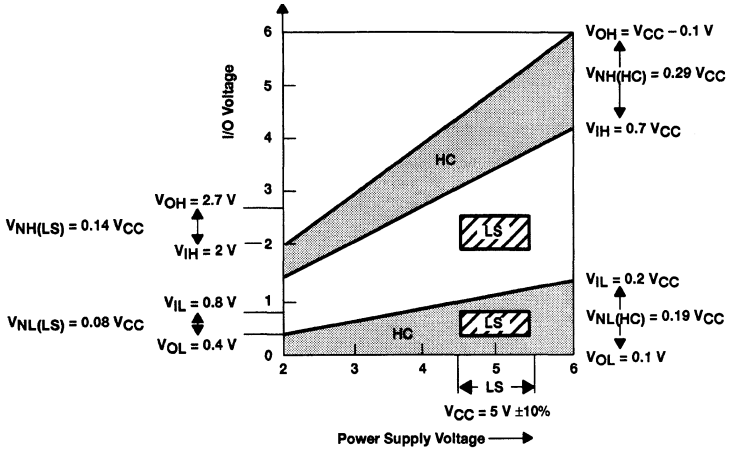


Figure 12. High-Speed CMOS and LS Noise Margins

6. High-speed CMOS devices can drive up to 10 LS loads (15 LS loads for high-current outputs) while maintaining good noise immunity. Although V_{OH}min and V_{OL}max are guaranteed for output currents up to 4 mA (6 mA for high-current outputs), currents up to ±25 mA (±35 mA for high-current outputs) can be obtained to drive LEDs or relays (see driving LEDs and relays in this section).
7. High-speed CMOS devices are specified for operation over an extended temperature range:

   SN54HC/HCT –55°C to 125°C (military)

   SN74HC/HCT –40°C to 85°C (industrial)

All specified ac and dc characteristics are ensured over this range with the exception of power dissipation capacitance (C_{pd}), which is specified as a typical value at 25°C.

Protection Circuitry

Electrostatic discharge (ESD) and latch-up are two traditional causes of CMOS device failure. To protect HCMOS devices from ESD and latch-up, additional circuitry has been implemented on the inputs and outputs.

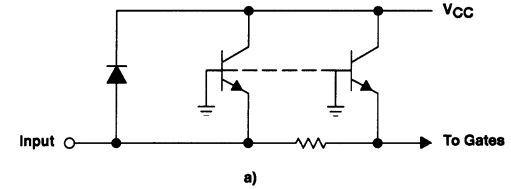
ESD Protection

ESD occurs when a buildup of static charges on one surface arcs through a dielectric to another surface that has the opposite charge. If this discharge current flows through an integrated circuit, the high currents can damage delicate devices on the chip. The protection circuits designed by Texas Instruments (TI) operate by shunting any excessive current safely around the sensitive circuitry on the chip. This provides ESD immunity on inputs and outputs, which exceeds MIL-STD-883B, Method 3015 requirements for ESD protection (2000 V, 1500 Ω, and 100 pF).

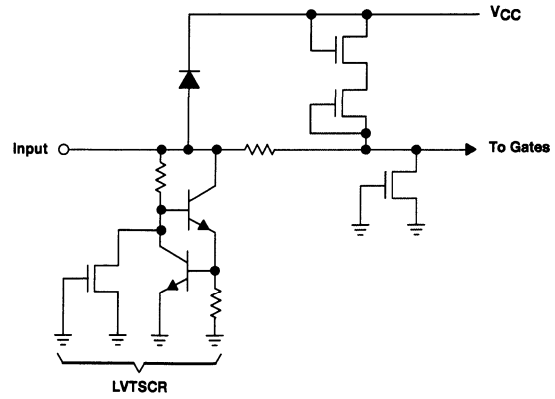
There are two types of input protection used, depending on device type. Figures 13a and 13b show the two input protection circuits. Both contain diodes that are forward biased for input voltages greater than V_{CC} + 0.5 V.

In Figure 13a, the two transistors and resistor are merged into a single geometry. The transistor is distributed along the length of the resistor to clamp negative-going transients.

In Figure 13b, the main protection is provided by a low-voltage-triggered SCR (LVTSCR) which fires for positive-going transients and acts as diode to ground for negative-going transients. The MOS devices shown are located at the gates of the input circuitry and provide further clamping.



a)



b)

Figure 13. ESD Input Protection Circuitry

There are two types of output protection used, depending on device type. Both include parasitic diodes (D1 and D2) that clamp the voltage to within 0.5 V of the power supply rails.

In Figure 14a, an additional diode (D3) is used to augment the parasitic diodes. In Figure 14b, and LVTSCR is used to provide additional clamping.

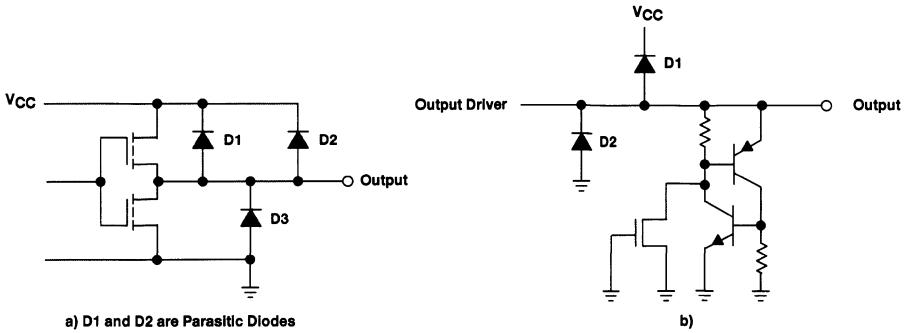


Figure 14. ESD Output Protection Circuitry

Latch-Up Protection

Latch-up cannot be completely eliminated. The alternative is to impede the triggering of the thyristor. Additional diffusions called guard rings are used to collect trigger currents before they can reach the junctions of the thyristor.

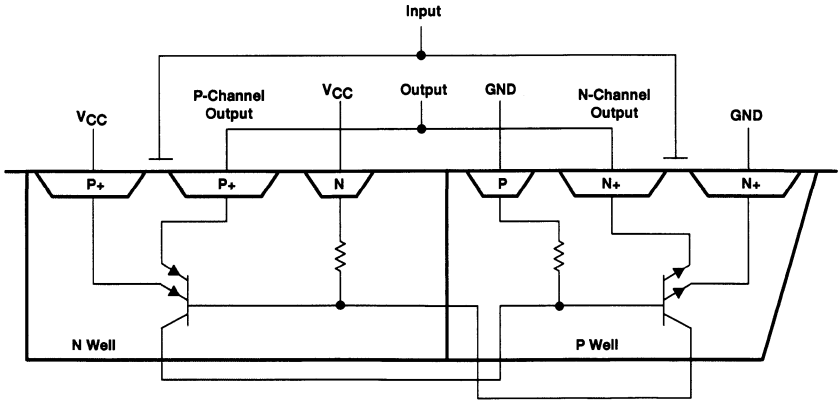


Figure 15. Parasitic Bipolar Transistors in CMOS

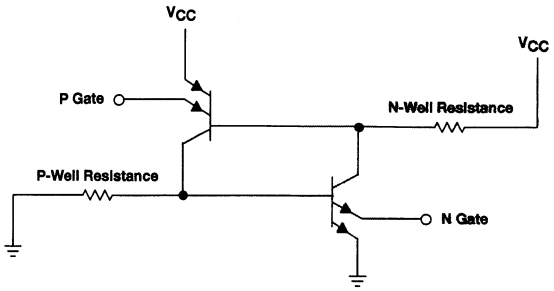


Figure 16. Schematic of Parasitic SCR With P-Gate and N-Gate Electrodes Connected

Two guard-ringing schemes are used, depending on device type. In one, any diffusion that is connected to a package pin is surrounded by four guard rings alternately connected to V_{CC} and ground, as shown in Figure 17. These guard rings collect any currents that can be injected into the substrate by signals on the device pins. Internal p-n junctions are separated by two guard rings.

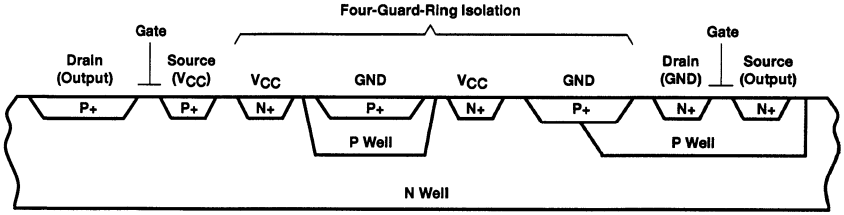


Figure 17. Unique Latch-Up Suppression Utilizes Guard Rings to Virtually Eliminate Latch-Up

In the second guard-ringing scheme, any diffusion that is connected to a package pin is surrounded by a grounded p-type guard ring. Internal p-n junctions do not have a guard ring.

Tests have shown effective latch-up protection typically greater than 250 mA at 125°C, higher at 25°C.

Fan-Out and Capacitance Loading Effects

High-speed CMOS can support up to 10 LS loads from a single standard output, or 15 loads from a high-current output. From the dc values in the individual data sheets, the fan-out of high-speed CMOS devices is unlimited for all practical purposes. However, from an ac point of view, there is a definite limit to the fan-out. The limiting constraint is the input rise time.

With a worst-case model, about 15 pF of capacitance is associated with the input of a high-speed CMOS device (10 pF from the device itself plus 5 pF of stray capacitance; typically, the input capacitance is 3 pF for all devices except the transceivers, which are 6 pF). The input resistance, r_i, and the output resistance, r_o, can be approximated with the following equations using the information contained in the electrical characteristics chart of the device.

$$r_i = \frac{V_I}{I_I} \tag{1}$$

where:

$V_I = V_{CC} = 6$ V
$I_I = 0.1$ nA

$$r_o = \frac{V_{CC} - V_{OH}}{I_{OH}} \tag{2}$$

where:

$V_{CC} = 4.5$ V
$V_{OH} = 4.3$ V (typical)
$I_{OH} = 4$ mA

The calculated input resistance is about 60 MΩ and the maximum output resistance is approximately 50 Ω. Figure 18 shows the schematic of the output and the input models using the values previously determined.

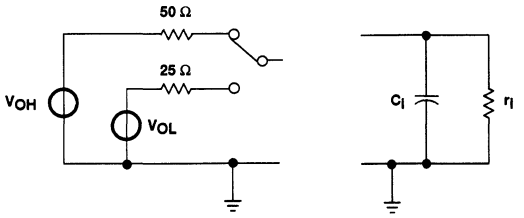


Figure 18. Worst-Case Output and Input Circuits of High-Speed CMOS

For a fan-out of n high-speed CMOS devices, the input capacitance will be (n × 15) pF (capacitances are in parallel). When the driving device switches its output from the low level to the high level, the input capacitance of all devices in the fan-out must be charged up and reach V_{IH}min within 500 ns (the recommended rise time). Therefore,

$$V_{IH}\text{min} = V_{OH}\text{typ}\left(1 - e^{-t/RC}\right) \tag{3}$$

where:

$R = 50\ \Omega$
$C = (15 \times n)$ pF
$t = 500$ ns
n = number of devices in the fan-out

Taking the natural log of both sides:

$$\frac{-t}{RC} = \ln\left(1 - \frac{V_{IH}min}{V_{OH}typ}\right) \quad (4)$$

Substituting the appropriate values and solving for n indicates that the maximum fan-out of high-speed CMOS devices is approximately 505. Solving for t in terms of n shows that each high-speed CMOS device added to the fan-out increases the propagation delay from the input of the driving device to the input of the driven devices by about 0.989 ns. This corresponds to an added delay of approximately 0.066 ns/pF. Table 2 contains typical values of fan-out and capacitive loading effects at different values of V_{CC}.

Table 2. Typical Fan-Out of High-Speed CMOS Devices and Propagation Delay Per pF at Various Values of V_{CC}

V_{CC} (V)	V_{OH}min (V)	V_{IH}min (V)	n	t_{pd}/pF (ns)
2	1.9	1.4	936	0.0667
4.5	4.4	3.15	993	0.0629
6	5.9	4.2	1004	0.0623

$$n = \frac{\frac{-t}{RC}}{\ln\left(1 - \frac{V_{IH}min}{V_{OH}min}\right)} \quad (5)$$

where:

R = 50 Ω
C = 8 pF
n = number of devices in the fan-out

$$\frac{t_{pd}}{pF} = \frac{500\ ns}{n \times 8\ pF} \quad (6)$$

Power Dissipation

The total power dissipation of high-speed CMOS devices is the sum of three components: quiescent power dissipation, P_Q; transient power dissipation, P_T; and capacitive power dissipation, P_C.

The quiescent power is the product of V_{CC} and the quiescent current, I_{CC}. The quiescent current is the reverse current through the diodes that are reverse biased. This reverse current is generally very small (a few nA), which makes the quiescent power almost insignificant. However, for circuits that are in static conditions for long periods of time, the quiescent power becomes a factor to be considered.

The transient power is due to the current that flows only when the transistors are switching from one logic level to the other. During this time, both transistors are partially on (one turning off, the other turning on), which produces a low-impedance path between V_{CC} and ground and results in a current spike. The rise (and fall) time of the input signal has a direct effect on the duration of the current spike. This is because the faster the input signal goes through the transition region, the less time both transistors are partially on. The transient power is dependent on the characteristics of the transistors, the switching frequency, and the rise time of the input signal. This component can be calculated using the following equation:

$$P_T = C_{pd} \times V_{CC}^2 \times f_i \tag{7}$$

where:

C_{pd} = power dissipation capacitance (specified on each data sheet) (8)

V_{CC} = supply voltage

f_i = output signal frequency

Additional capacitive power dissipation is caused by the charging and discharging of the external load capacitance and is dependent on the switching frequency. To calculate this power, the following equation may be used:

$$P_C = C_L \times V_{CC}^2 \times f_i \tag{9}$$

where:

C_{pd} = power dissipation capacitance (specified on each data sheet)
V_{CC} = supply voltage
f_i = input signal frequency

$$P_C = C_L \times V_{CC}^2 \times f_o \tag{10}$$

where:

C_L = external (load) capacitance
V_{CC} = supply voltage
f_o = output signal frequency

HCT Power Dissipation

HCT devices are used primarily to interface TTL output signals to high-speed CMOS inputs. To make the inputs of the HCT devices TTL-voltage compatible, the input transistor geometries were changed. This increased the power consumption compared to the equivalent HC device; however, HCT still provides a considerable savings in power over TTL. The increase in power consumption results from the TTL input levels causing both transistors in the transistor pair to be partially turned on. Included in the electrical characteristics table for HCT devices is a parameter, ΔI_{CC}, that enables the designer to compute how much additional current the HCT device draws per input when at a TTL voltage level.

Power Supply Decoupling

When an SN54/74HC gate switches, there is a brief period (about a nanosecond) during which both transistors in the gate output buffer (see Figure 19) are partially on. In this interval, the device draws a substantial supply current, producing a current spike on the V_{CC} and ground leads to the gate. This spike can exhibit di/dt as high as 5000 A/s. These spikes react with the distributed inductance of the supply wiring to produce significant voltage transients on V_{CC} and ground unless adequate supply decoupling is provided. These transients, if allowed, couple directly into the gate outputs, which in normal usage switch from rail to rail.

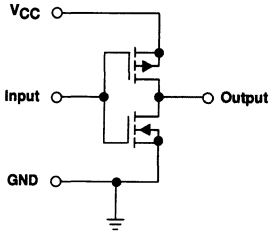


Figure 19. Gate Output Buffer

Decoupling Procedure

Figure 20 shows a circuit for testing the effectiveness of decoupling. In this test circuit, the V_{CC} and ground connections consist of two parallel runs of one-eighth-inch copper on a G-10 epoxy-glass circuit board. As a 0.01-μF decoupling capacitor between V_{CC} and ground is physically moved away from a driven gate in 1.5-inch increments, V_{CC} transients increase, as shown in Figure 21.

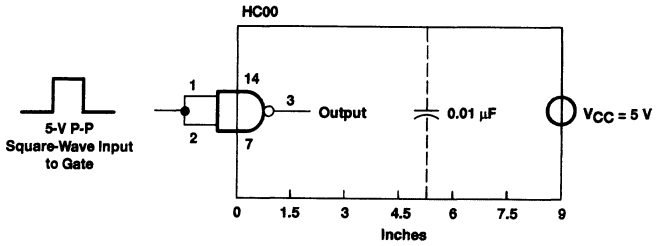


Figure 20. Test Circuit for Decoupling Effects

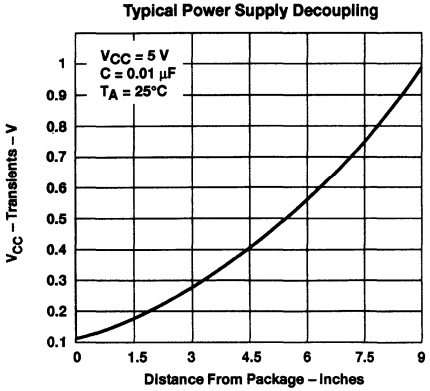


Figure 21. V_{CC} Transients vs Decoupling Capacitor Distance From DIP

The results indicate the importance of adequate decoupling and illustrate the correct procedure for obtaining it. This procedure consists of locating decoupling capacitors as close as possible to the integrated-circuit package to maximize noise margins.

Connecting Unused Inputs

Unused inputs should be tied to V_{CC} or ground to prevent the input from floating. If left to float, the power consumption of the device increases.

Matching

Another factor to consider when designing with high-speed CMOS is the V_{OH}min-to-V_I matching. This is important when the V_{OH}min of the driving device exceeds the V_{CC} + 0.5 V of the driven device. If this occurs, the ESD protection diode on the inputs is forward biased. At this point, the driving device attempts to power up the driven device's power supply. No damage occurs to the driven device if the current flowing through the diode does not exceed 20 mA.

Powering Up/Down Sequence for High-Speed CMOS

To avoid any possible damage and reliability problems to the high-speed CMOS devices when applying power, the following steps should be followed:

1. Connect ground
2. Connect V_{CC}
3. Connect the input signal

When powering down a high-speed CMOS device, follow the above steps in reverse order.

High-Speed CMOS Interfacing

Introduction

The high-speed CMOS logic family from TI contains a broad spectrum of SSI/MSI functions. Within this family are TTL functions, HCT devices, HC4000 series, and an HCU device.[2] Entire CMOS systems can be implemented using this logic family. There is also a broad range of CMOS-system to non-CMOS-system interfaces that need to be considered. The design engineer inevitably encounters these interfaces. To develop the necessary interfaces, a thorough understanding of data sheet parameters of both systems and an organized approach is recommended. This report uses basic examples to present one possible approach to the SN54/74HC interface solution.

There are two types of interfacing that must be considered:

1. Interfacing CMOS system signals to non-CMOS systems
2. Interfacing non-CMOS system signals to CMOS systems

The first type requires an understanding of the CMOS output parameters and the non-CMOS input parameters, and vice versa for the second type. In both cases, a model of the inputs and outputs of both systems may be useful.

General Interfacing Solution

An interfacing problem arises when the output logic levels and/or the current requirements of the driving system (or device) are different from the input logic levels and/or the current requirements of the driven system (or device). When determining the compatibility of the systems (or devices), the most important system/device parameters are V_{IH}, V_{IL}, V_{OH}, V_{OL}, I_{IH}, I_{IL}, I_{OH}, and V_{OL}.

Figure 22 is the voltage transfer characteristic of a typical unloaded inverter showing the various input- and output-voltage parameters. Loading the output of the inverter lowers V_{OH} and raises V_{OL}. The electrical characteristics table in data sheets specifies minimum V_{OH} and maximum V_{OL} for various loads.

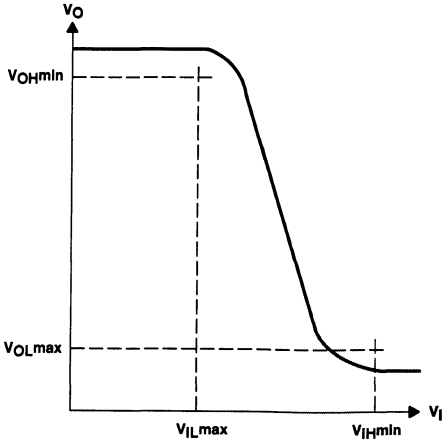


Figure 22. Voltage Transfer Characteristic of a Typical Inverter

[2] HCT devices are explained later. The HC4000 series devices are, pin-for-pin, functionally compatible, but not electrically compatible, with the older metal-gate CMOS devices. The HCU device is unbuffered.

Noise Margin

There are two noise margins to be considered: the low-voltage and the high-voltage noise margin. The voltage difference between V_{IL}max of the driven system/device and V_{OL}max of the driving system/device is the low-voltage noise margin. The voltage difference between V_{OH}min of the driving system/device and V_{IH}min of the driven system/device is the high-voltage noise margin (see Figure 23).

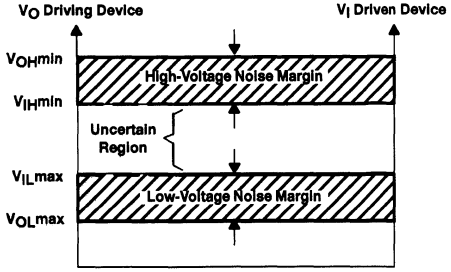


Figure 23. Noise Margins

It is desirable to have the noise margin as large as possible and the uncertain region (the difference between V_{IH}min and V_{IL}max) as small as possible. When an input voltage falls into the uncertain region, we do not know how the output, in conjunction with other inputs driven by that output, will respond. The problem with small noise margins is that any noise on the output of the driving system or device causes the signal to fall into the uncertain region and could possibly cause a bit error in the system. There are various sources of noise in digital systems. Three possible internal sources are inductive and resistive drops, capacitive coupling from another logic node, and mutual inductance with another logic node. Radio signals are possible external sources of noise.

As an aid for interfacing between the various TTL families, the eight parameters previously defined are shown in Table 3. The values are for V_{CC} = 5 V and T_A = 25°C (worst-case device parameters — the device will perform at least this well). All currents are designated positive when flowing into the device.

Table 3. Worst-Case Values of Primary Interfacing Parameters

PARAMETER	74HCMOS	AHC	74TTL	74LS	74AS	74ALS
V_{IH}min	3.5 V	3.85 V	2 V	2 V	2 V	2 V
V_{IL}max	1 V	1.65 V	0.8 V	0.8 V	0.8 V	0.8 V
V_{OH}min	4.9 V	3.8 V	2.4 V	2.7 V	2.7 V	2.7 V
V_{OL}max	0.1 V	0.44 V	0.4 V	0.4 V	0.4 V	0.4 V
I_{IH}max	1 μA	1 μA	40 μA	20 μA	200 μA	20 μA
I_{IL}max	−1 μA	−1 μA	−1.6 mA	−400 μA	−2 mA	−100 μA
I_{OH}max	−4 mA	−8 mA	−400 μA	−400 μA	−2 mA	−400 μA
I_{OL}max	4 mA	8 mA	16 mA	8 mA	20 mA	4 mA

Driving-Gate Output Model

Figure 24 shows the model of a driving gate derived from the data sheet specifications. $V_{OH(nl)}$ (nl = no load) is the high-level output voltage expected when the output gate is unloaded. $V_{OL(nl)}$ is the low-level output voltage expected when the output gate is unloaded. The values for these two voltages usually are not given on the data sheets. As a rule of thumb for MOS devices, the output switches between the power rails $V_{OH(nl)} = V_{CC}$ and $V_{OL(nl)}$ = GND; for bipolar devices (e.g., the TTL family) $V_{OL(nl)}$ is about V_{CC}(sat) or about 0.3 V. $V_{OH(nl)}$ varies within the TTL family. Standard TTL has a $V_{OH(nl)}$ within two base-emitter drops of V_{CC}($V_{OH(nl)} = V_{CC} - 1.2$ V); LS has a $V_{OH(nl)}$ within one base-emitter drop of V_{CC}($V_{OH(nl)} = V_{CC} - 0.6$ V). The data sheets specify V_{OH}max and V_{OL}max at a nonzero I_{OH} and I_{OL}, respectively. Therefore, to calculate the approximate series resistances, the following two equations can be used:

$$R_{OH} = \frac{|V_{OH(nl)} - V_{OH}min|}{I_{OH}} \quad (11)$$

$$R_{OL} = \frac{|V_{OL(nl)} - V_{OL}max|}{I_{OL}} \quad (12)$$

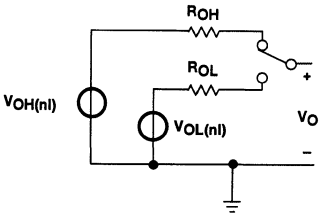


Figure 24. Output Model of a Driving Gate

Input-Gate Circuit

A simplified schematic of a high-speed CMOS input gate is shown in Figure 25. The diode (D1) and the transistors (Q1 and Q2) provide static discharge and input transient clamping for the device. Any inputs higher than V_{CC} + 0.5 V or lower than –0.5 V clamps the input. The capacitors (C1 and C2) represent the parasitic capacitances present at the gate input. The data sheet specifies that the input capacitance (C1 + C2) does not exceed 10 pF (typical is about 5 pF). The input capacitance is split between V_{CC} and ground of the device and provides a feedback path between V_{CC} and the input. If the input is driven by a high-impedance source, any transient noise on V_{CC} may be coupled back into the input.

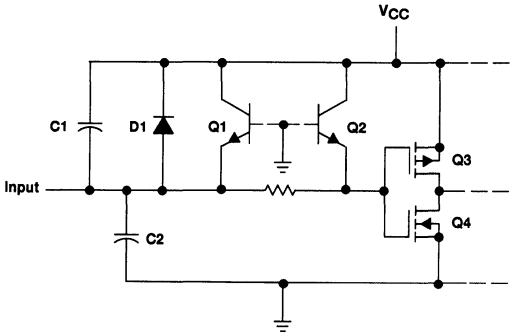


Figure 25. SN54/74HC Input Gate

CMOS-to-Standard-TTL Interface

CMOS devices can drive TTL loads with no additional interfacing required. The output voltages of CMOS devices are compatible with the input voltage requirements of TTL devices. The input current requirements of the TTL devices place a strict limitation on the number of TTL devices that CMOS devices can drive from a single output (the fan-out).

Figure 26 shows a CMOS output gate driving a TTL input gate. When the CMOS gate drives the emitter of Q3 low, a current flows into the CMOS gate from R1 and the emitter of the TTL gate. The maximum guaranteed current that the CMOS device can sink is 4 mA. However, the device can sink up to 25 mA, but the output voltage is not guaranteed above 4 mA. Therefore, the maximum TTL fan-out that a device can drive without exceeding the specified limit is two (I_{IL} for TTL is –1.6 mA).

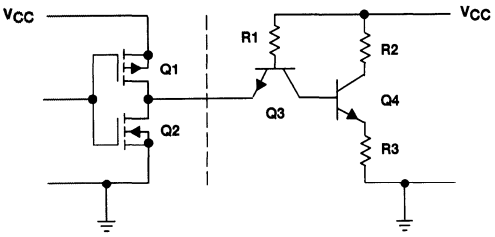


Figure 26. SN54/74HC-to-TTL Interface

Standard TTL-to-CMOS Interface

The interface for TTL driving CMOS is not as simple as the CMOS-to-standard-TTL interface. Using the voltage levels from Table 3, it is obvious that V_{OH}min of the TTL device and V_{IH}min of the CMOS device are not compatible. Figure 27 shows the schematic of the TTL-to-CMOS interface. The pullup resistor, R_p, eliminates the voltage incompatibility.

The lower limit of the pullup resistor is determined by the current-sinking capability of the driving device (TTL for this interface). When the TTL device output goes low, Q3 (see Figure 27) is required to sink a current of ($V_{CC} - V_{OL}$max)/Rp in addition to the sum of the output currents of the driven devices I_{IL} worst case. All of this is shown in the following equation:

$$R_p\text{min} = \frac{V_{CC} - V_{OL}\,\text{max(TTL)}}{I_{OL}\text{(TTL)} + n\ I_{IL}\text{(load)}} \quad (13)$$

where:

n = number of loads being driven
V_{CC} = voltage applied to the pullup resistor

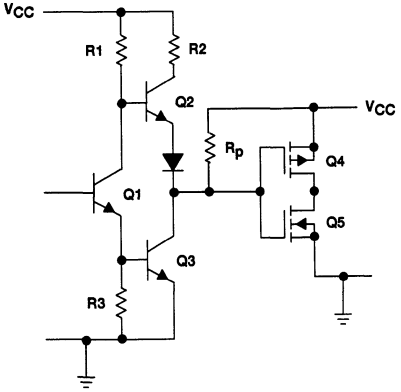


Figure 27. TTL-to-SN54/74HC Interface With a Pullup Resistor

Example 1. An SN74LS00 is driving three SN74HC00 devices.
V_{CC}min = 4.75 V, V_{OL}max = 0.4 V, I_{OL} = 8 mA, I_{IL} = 1 μA, and n = 3, therefore $R_p$min = 543 Ω.

The upper limit of the pullup resistor is determined by two factors:

1. Total input capacitance of the loads
2. Total high-level input currents of the loads

When the TTL output goes high, Q2 is turned off by the pullup resistor. Therefore, all the current that flows into the devices that are being driven flows through the pullup resistor, R_p. Therefore, the input voltage of the CMOS devices rises exponentially, with a time constant of R_pC_i (C_i = 10 pF max). The time constant cannot exceed the 500-ns rise-time requirement of the CMOS device. Along with this limitation, the total input currents must not cause the voltage drop across the pullup resistor to exceed V_{IH}min for the CMOS devices. Bringing all this into play, the following equation may be used to determine $R_p$max:

$$R_p\text{max} = \frac{V_{CC} - V_{IH}\text{min(load)}}{|n\ I_{IH}\text{(load)} - I_{OH}\text{(driver)}|} \quad (14)$$

where:

n = number of loads being driven
V_{CC} = voltage applied to the pullup resistor

Example 2. An SN74LS00 is driving three SN74HC00 devices.
V_{CC} = 5.25 V, V_{IH}min = 3.675 V, I_{IH} = 1 μA, I_{OH} = 0, and n = 3, therefore $R_p$max = 525 kΩ.

However, if the rise time is calculated using this value of $R_p$max, the recommended 500 ns is exceeded.

From the relationship:

$$V_{IH}\text{min} = V_{CC}\text{max}\left(1 - e^{-t/R_pC_i}\right) \quad (15)$$

with:

V_{IH}min = 3.675 V
V_{CC}max = 5.25 V

then:

$$R_p = \frac{t}{1.2\ C_i} = 13.8\Omega\ (t = 500\text{ ns and } C_i = 30\text{ pF}) \quad (16)$$

Generally, this rise-time constraint is the limiting factor on the upper limit of the pullup resistor.

CMOS-to-LS Interface

The interface of CMOS to LS is very similar to the interface of CMOS to TTL (see Figure 28). As shown, there is no pullup resistor required. When the LS input is pulled low, the current flows through R1 and D2 into the CMOS output. In the worst-case condition, this current is about 0.4 mA. Because the CMOS output parameter I_{OL} specifies a 4-mA current sink for the device, the maximum LS fan-out is ten.

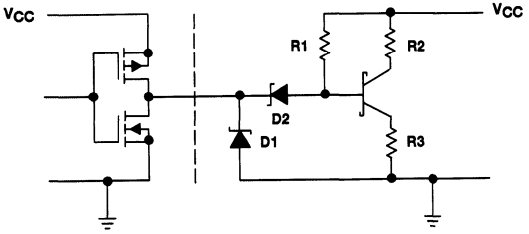


Figure 28. SN54/74HC-to-LS Interface

LS-to-CMOS Interface

For an LS device to drive a CMOS device, a pullup resistor must be used because the V_{OH}min of the LS is less than the specified V_{IH}min of the CMOS device. Figure 29 shows the schematic of the LS/CMOS interface. The upper and lower limits of the pullup resistor are determined by the same method as the TTL/CMOS interface. The upper limit of the pullup resistor is limited by the input currents and the input capacitance.

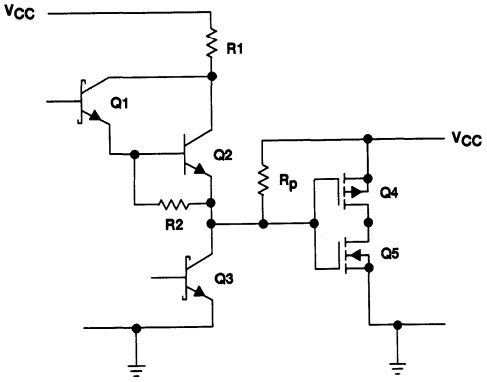


Figure 29. LS-to-SN54/74HC Interface With a Pullup Resistor

CMOS-to-ALS Interface

The output logic level of CMOS devices is completely compatible with the input logic levels of ALS devices. The interface structure with ALS is shown in Figure 30. As with the other CMOS-to-TTL interfaces, there is no pullup resistor required. The fan-out of ALS devices is determined by the amount of current that flows through Q3 into the CMOS device and the amount of current the CMOS device can sink. When the input of the ALS device is low, there is 0.1 mA flowing through Q2. The maximum current that the CMOS device can sink (according to the parameters) is 4 mA. This corresponds to an ALS fan-out of 40.

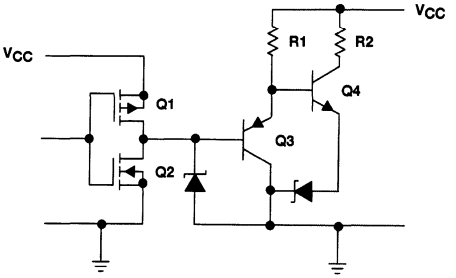


Figure 30. SN54/74HC-to-ALS Interface

ALS-to-CMOS Interface

The high-level output voltage of ALS devices is incompatible with the required high-level input voltage of CMOS devices. Because of this incompatibility, a pullup resistor is required to make the two voltage levels compatible. The method of determining the upper and lower limits of the pullup resistor is the same as the other two TTL-to-CMOS interfaces (see Figure 31).

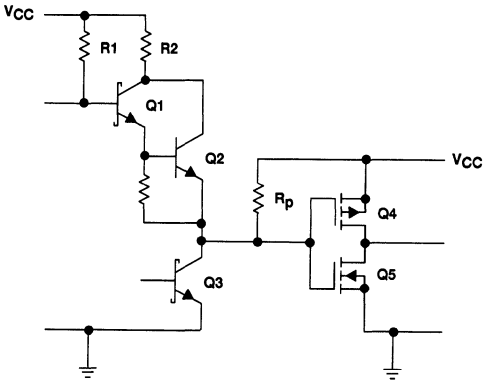


Figure 31. Interface With a Pullup Resistor

CMOS-to-AS Interface

As in the case of the other CMOS-to-TTL interfaces, no pullup resistor is required (see Figure 32) because the input voltage levels of AS are compatible with the output voltage levels of CMOS. The fan-out of AS devices is limited by the low-level input current (I_{IL}) of AS and the current-sinking capability of CMOS (I_{OL}). I_{IL} for the AS is 2 mA, and the current-sinking limit of CMOS is 4 mA. Therefore, the fan-out is two AS devices.

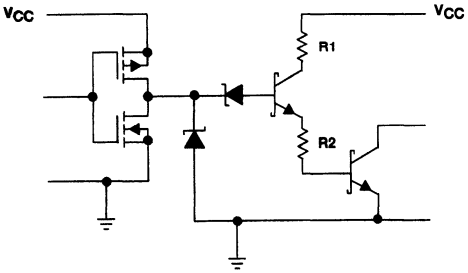


Figure 32. SN54/74HC-to-AS Interface

AS-to-CMOS Interface

Not all the output logic levels of AS are compatible with the input logic levels of CMOS. Table 4 shows there is incompatibility between the V_{OH} of AS and V_{IH} of CMOS. As with other TTL-to-CMOS interfaces, a pullup resistor is required (see Figure 33). The appropriate value of the pullup resistor is determined by the same procedure previously explained.

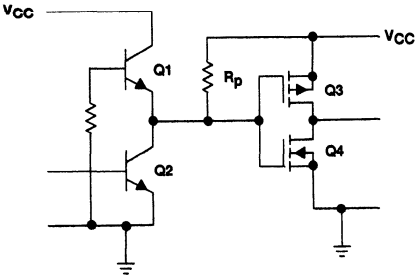


Figure 33. AS-to-SN54/74HC Interface With a Pullup Resistor

CMOS-to-NMOS Interface

NMOS is used extensively in large-scale integration products such as microprocessors, microcomputers, and memories. The logic levels of NMOS are usually TTL compatible. CMOS devices can drive NMOS devices with no pullup resistors. The input impedance of NMOS is very high, which is similar to the input impedance of CMOS.

NMOS-to-CMOS Interface

A pullup resistor may be necessary when an NMOS device drives a CMOS device. The method of determining the value range of the pullup resistor is the same as the method described previously for TTL. A quick look at NMOS output parameters and CMOS input parameters will determine if a pullup resistor is required.

Using HCT Devices to Interface to CMOS From TTL

There are two methods to interface from a TTL system (standard TTL, LS, AS, ALS):

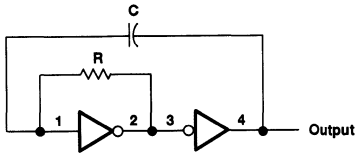
1. Use of pullup resistors (as previously described)
2. Use of HCT devices (by far the easier method)

The HCT device inputs are TTL compatible; the outputs are both TTL and CMOS compatible. Therefore, all the interface requires is to connect the TTL system output into the HCT device, and the output of the HCT device can then be used for the input of the CMOS system.

Oscillators

RC Oscillators

Simple oscillator circuits using a minimum number of components can be designed with high-speed CMOS devices, e.g., two HC04, HCU04, or HC02 gates. These oscillators generate a period of approximately 1.8 RC seconds (see Figure 34).



R = 2.7 kΩ to 2.7 MΩ, C = 50 pF to 10 μF

Figure 34. Simple RC Oscillator Using Two HC04 Gates

Crystal-Controlled Oscillators

A crystal or ceramic resonator can be used to set the oscillator period (see Figure 35). The value of the resistor, typically 100 kΩ, may require special selection to ensure oscillation at the desired fundamental resonator frequency. The capacitor, typically 100 pF, is required to dampen parasitic oscillations in the 30-MHz to 50-MHz range.

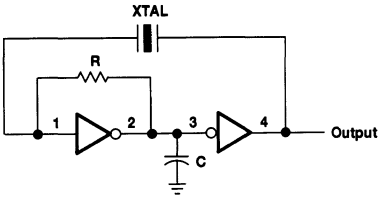


Figure 35. Oscillator Circuit Using a Crystal to Set the Period

Voltage-Controlled Oscillators

Voltage-controlled oscillators (VCOs) can also be designed using a minimal number of components. Figure 36 shows a VCO using NAND and inverter gates. This VCO design exploits the phenomena of the slight variations in the propagation delay of an HC gate with changes in the supply voltage. The HC00 is connected as a three-stage ring oscillator with a buffer. As the control (supply) voltage, V_C, is varied, the ring oscillator's frequency changes according to the following:

$$f_{out} \approx 5.8 \times V_C \quad (17)$$

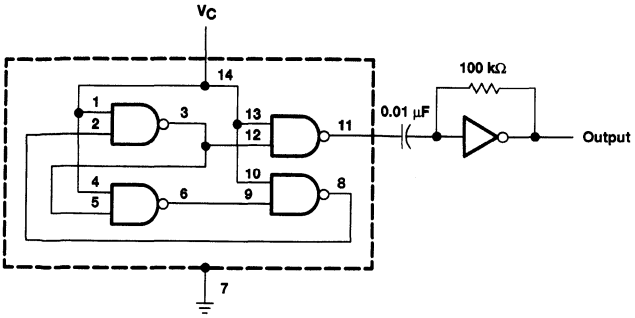


Figure 36. VCO

The inverter, which is powered by a separate voltage source, serves to restore the oscillator output voltage to 5 V, peak to peak. This function is required because the HC00 switches from rail to rail (as do all HC devices). The magnitude of the oscillator output voltage is thus dependent on V_C. The 100-kΩ resistor across the inverter provides bias such that operation is within the linear operating region of the gate. The capacitor serves as an ac-couple between the oscillator and inverter.

The VCO output is linear for control voltages in the range of 1.5 V to 4.5 V (see Figure 37).

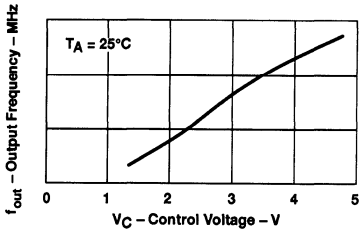


Figure 37. VCO Output Frequency vs Input Voltage

To prevent oscillator "bleed-through" onto the V_{CC} line, adequate decoupling of the HC device power supply is required.

Drivers for LEDs and Relays

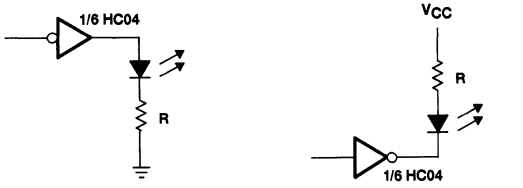
Introduction

SN54/74HC devices are capable of sinking or sourcing up to 25 mA (35 mA for high-current devices) per gate. As the device sinks or sources more current, V_{OH}min or V_{OL}max levels begin to fall or rise, respectively.

Because of these characteristics, SN54/74HC devices can be used to drive LEDs and relays.

Driving LEDs

Figure 38 shows an HC04 driving a TTL221 gallium phosphide light-emitting diode. The resistor performs the function of current limiter. The luminous intensity of the LED depends on the amount of forward current.



a) V_{IL} at the Input Turns on the LED b) V_{IH} at the Input Turns on the LED

Figure 38. HC04 Driving an LED

Example 3. Using 10-mA forward current and 2.2-V forward voltage, the value of the current-limiting resistor can be calculated using the following equations:

V_{IL} at the input:

$$R = \frac{V_{OH} - 2.2\ V}{10\ mA} \tag{18}$$

V_{IH} at the input:

$$R = \frac{V_{CC} - 2.2\ V - V_{OL}}{10\ mA} \tag{19}$$

It should be noted that, as used here, V_{OH} and V_{OL} are not the V_{OH}min and V_{OL}max specified in the data book. Figures 39 and 40 show typical values for V_{OH} and V_{OL} for an HC00.

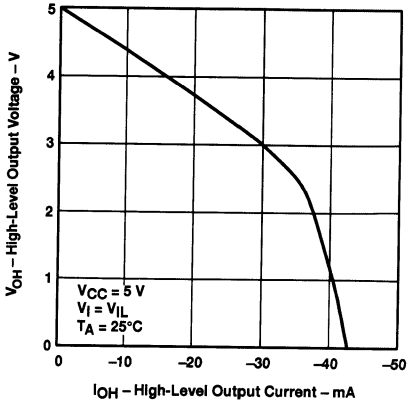


Figure 39. Typical Values for V_{OH}

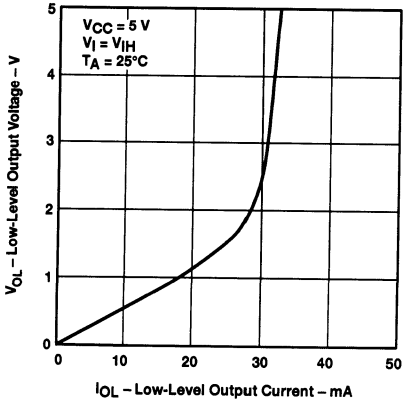


Figure 40. Typical Values for V_{OL}

Driving Relays

Multiple gates can be connected in parallel to increase the current-sinking or sourcing capability of SN54/74HC devices. Figure 41 shows two HC04 gates connected in parallel for a relay-driver application.

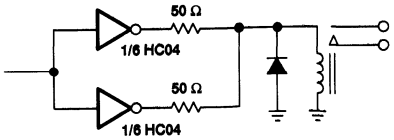


Figure 41. SN54/74HC04 Gates Connected In Parallel to Drive a Relay

Precautions should be taken to prevent one gate from passing a disproportionate amount of current. Small resistors (typically 50 Ω) in series with the output gate distribute the current more evenly amon the gates.

In all applications in which the SN54/74HC output is required to source or sink substantial current (6 mA to 25 mA), particular attention should be paid to providing adequate power supply decoupling for the driving device.

SN54/74HC Interchangeability Guide

Introduction

The following has been prepared as a guide to interchanging devices from other logic families, both bipolar and CMOS, with those from the SN54/74HC family. This is not intended to be a comprehensive guide since interchangeability can depend on many factors, and only careful comparisons of data sheets can provide definitive answers. The considerations listed below are based on information accumulated in answering a large number of inquiries in this area.

First, a brief review is given on each logic technology, then a discussion is given on the various aspects involved in attempting to interchange that technology with the SN54/74HC family.

TTL: Transistor-Transistor Logic

TTL is the generic name for several bipolar families that have evolved over the last 20 years. Low-power Schottky (LS) is the most widely used bipolar logic family today. Other families, e.g., Schottky (S), advanced Schottky (AS), and advanced low-power Schottky (ALS) are also used, depending on the speed-versus-power performance required by a given system design.

4000 Series: Metal-Gate CMOS Logic

The device type numbers in this series have a variety of prefixes, although "CD" is probably the most widely recognized. The suffix "B" is frequently used, indicating an improvement over the original family; i.e., buffered outputs and typical output sink and source current capabilities of ±1 mA. This logic family became popular because it offered very low power consumption, even though it is slower than TTL, with a typical operating frequency of about 5 MHz, has a low level of ESD protection, and is susceptible to latch-up problems.

40H00 Series: Metal-Gate CMOS Logic

This series was designed to overcome the speed limitations of the original 4000 family. Even though these devices are somewhat faster, they are still slow when compared to LS.

74C00 Series: Metal-Gate CMOS Logic

The distinguishing feature of this family is that the pinouts correspond to those of TTL, making interchangeability easier. However, the devices exhibit many of the same speed/power limitations as those of the 4000 series. The fan-out is typically higher than the 4000 series, however, with typical output sink and source capabilities of ±1.75 mA.

74SC00 Series: Silicon-Gate CMOS Logic

This series was the forerunner to the SN54/74HC family or, more closely, to the SN54/74HCT family. The 74SC family was designed to overcome many of the 4000 series deficiencies, particularly the slower speed and the lower drive capability.

The "SC" designation should not be confused with that of TI's standard cell family (SN54/74SC series).

Interchangeability Considerations

Listed below are the highlights of benefits derived from replacing other logic families with SN54/74HC; also listed are important considerations that may affect the feasibility or desirability of such replacement. All comparisons are, by necessity, general in nature.

LS

Considerations:

1. SN54/74HC high-level input voltages are not TTL compatible. In a mixed-family system (LS output driving HC input), it is necessary to use SN54/74HCT pullup resistors or level shifters.
2. SN54/74HC has less drive capability than some LS functions.
3. LS open-collector outputs have higher breakdowns than SN54/74HC open-drain equivalent functions.

HCMOS advantages:

1. Lower system power consumption
2. Improved noise immunity
3. Wider supply-voltage range

Other TTL Families

Considerations:

1. SN54/74HC high-level input voltages are not TTL compatible. In a mixed-family system (TTL output driving HC input), it is necessary to use SN54/74HCT pullup resistors or level shifters.
2. SN54/74HC has less drive capability than some TTL functions.
3. TTL open-collector outputs have higher breakdowns than SN54/74HC open-drain equivalent functions.
4. Some of the TTL families offer greater operating speed; e.g., S, AS, and ALS.

HCMOS advantages:

1. Lower system power consumption
2. Improved noise immunity
3. Wider supply-voltage range

4000 Series and 74C00 Series

Considerations:

1. Although most applications use a 5-V supply, these older families operate in the 3-V to 15-V range.
2. SN54/74HC must be operated with a supply voltage in the 2-V to 6-V range.

HCMOS advantages:

1. Higher frequency of operation
2. Improved ESD protection and latch-up performance
3. Higher output drive capability

As a quick reference guide, Table 4 highlights the advantages and disadvantages of interchanging other logic families with high-speed CMOS.

Table 4. Highlights of Interchangeability

	TTL FAMILY (TTL, LS, S, ALS, AS)	METAL-GATE CMOS
Power	HCMOS offers lower system power consumption than any of the TTL families.	Power consumption of HCMOS is less than metal-gate CMOS.
Speed	HCMOS operating speed is comparable to LS. Some TTL families (S, AS, and ALS) offer greater operating speed.	HCMOS operating speed is much faster than metal-gate CMOS.
Input voltage	The V_{IH}min of HCMOS is not compatible with the V_{OH}min of TTL. In mixed-family systems, it is necessary to use HCT devices, pullup resistors, or level shifters.	HCMOS input voltage levels are compatible with metal-gate CMOS outputs only when the power supply voltage for the metal-gate CMOS devices is between 2 V and 6 V.
Output voltage	The output voltages of HCMOS are TTL compatible.	HCMOS output voltage levels are compatible with metal-gate CMOS inputs only when the power supply voltage for the metal-gate CMOS devices is between 2 V and 6 V.
Drive capability	The output current capability of HCMOS is not as large as the TTL family.	HCMOS has a higher current drive capability.
Fan-out (LS devices)	HCMOS has a smaller fan-out to LS devices than the TTL family.	HCMOS has a higher fan-out to LS devices.
Supply voltage	HCMOS has a wide operating supply-voltage range (2 V to 6 V).	Operating supply-voltage range of metal gate is larger than HCMOS (from 3 V to 15 V).
ESD and latch-up	TTL-family devices are not as vulnerable to ESD and latch-up damage.	HCMOS has an improved protection circuitry against ESD and latch-up.

Electrostatic Discharge (ESD)

Introduction

In recent years, the semiconductor industry has made great strides in developing faster, lower power, and smaller devices. During the 1990s, many devices will be produced with minimum feature size of structures on a silicon chip of 0.25 μm. To put this in perspective, a typical human hair is about 75 μm in diameter. However, as feature sizes get smaller and smaller, ESD sensitivity (the voltage level at which the device will sustain damage) also gets lower. This means that ESD protection and ESD handling procedures will become even more important in the future to avoid ESD damage.

All semiconductor devices have an ESD voltage threshold above which they will sustain damage. While circuit designers can provide some on-circuit ESD protection (typically in the 2000-to-4000-V range for the human body model and 200 V to 300 V for the machine model), this is well below the static-voltage levels found in work areas without ESD protection. Proper ESD handling and packaging procedures must be used throughout the processing, handling, and storing of unmounted ICs and ICs mounted on circuit boards.

What is ESD and How Does It Occur?

Static charge is an unbalanced electrical charge at rest. It is created by insulator surfaces rubbing together or pulling apart. One surface gains electrons while the other surface loses electrons. This results in an unbalanced electrical condition recognized as static charge.

When a static charge moves from one surface to another, it becomes ESD. ESD is a miniature lightning bolt of static charge that moves between two surfaces that have different potentials. It can only occur when the voltage differential between the two surfaces is sufficiently high to break down the dielectric strength of the medium separating the two surfaces. When static charge moves, it becomes a current that damages or destroys oxides, metallizations, and junctions. ESD can occur in any one of four different ways: a charged body can touch an IC, a charged IC can touch a grounded surface, a charged machine can touch an IC, or an electrostatic field can induce a voltage sufficient to break down the dielectric.

Latent Defects

Devices with latent ESD defects are called "walking wounded" because they have been degraded but not destroyed by ESD. This occurs when an ESD pulse is not sufficiently strong to destroy a device but, nevertheless, causes damage. Often, the device suffers junction degradation through increased leakage or a decreased reverse breakdown, but the device still functions and is still within data-sheet limits. A device may be subjected to numerous weak ESD pulses, producing cumulative degradation until the device fails. There is no known practical screen for walking-wounded devices. To avoid this type of damage, devices must be continually accorded ESD protection, as outlined later.

What Voltage Levels of ESD Are Possible?

It has been shown that human beings can be charged up to 38,000 V just by walking across a rug on a low-humidity day. For an ESD pulse to be seen, felt, or heard, it must be in the range of 3000 V to 4000 V. Many devices can be damaged well below this threshold.

How to Avoid ESD Damage to ICs

Because ESD can occur only when different potentials are involved, the best way to avoid ESD damage is to keep the ICs at the same potential as their surroundings. The logical reference potential is ESD ground. So the first and most important rule in avoiding ESD damage is to keep ICs and everything that comes in close proximity to them maintained at ESD-ground potential. Four supplementary rules support this first rule:

1. Any person handling the ICs should be grounded either with a wrist strap or ESD-protective footwear used with a conductive or static-dissipative floor or floor mat.
2. The work surface where devices are placed for handling, processing, testing, etc., must be made of static-dissipative material and be grounded to ESD ground (see Figure 43).
3. All insulator materials must either be removed from the work area or they must be neutralized with an ionizer. Static-generating clothing can be covered up with an ESD-protective smock.
4. When ICs are being stored, transferred between operations or workstations, or shipped, they must be maintained in a Faraday-shield container whose inside surface (touching the ICs) is static dissipative.

Humidity

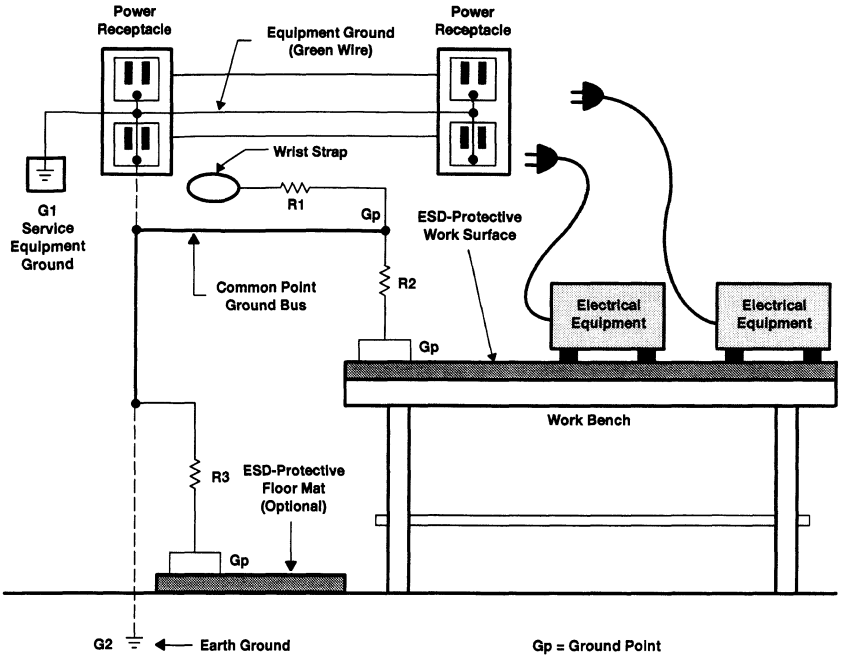
Where insulators are present, humidity is a very important factor in the generation of static electricity. Humidity affects the surface resistivity of insulator materials. As humidity increases, the surface resistivity decreases. This means that insulator materials rubbed together or pulled apart in a humid environment generate lower static charges than the same materials rubbed together or pulled apart in a dry environment. Where it is possible to control humidity, it is recommended that relative humidity be maintained between 40 percent and 60 percent. Higher humidity becomes very uncomfortable for humans, and lower humidity increases the risk of static generation from insulators. Humidity is a supplementary control and is not sufficient by itself to reduce static voltages to safe levels.

Training

All personnel who come in close proximity to ESD-sensitive ICs must receive ESD training initially and then again each year as a minimum. No ESD program can be successful unless the people who handle the ICs understand the need for ESD controls.

ESD Specification

Each area handling ESD-sensitive devices is operated in accordance with the established ESD handling procedure. The latest version of this controlled document is maintained in each area and is accessible to all area personnel.



NOTES: 5. G1 (equipment ground) or G2 (earth ground) is acceptable for ESD ground. Where both grounds are used, they are connected (bonded) together.
6. R1 is mandatory for all wrist straps.
7. R2 (for static dissipative work surfaces) and R3 (for ESD-protective floor mats) are optional. ESD-protective flooring is connected directly to the ESD ground without R3.
8. This ESD-protected workstation complies with JEDEC Standard No. 42 and EIA-625.

Figure 42. ESD-Protected Workstation (Side View)

ESD Coordinator

One person is identified who has overall responsibility for the ESD program. This person is responsible for writing the ESD handling procedure and keeping it updated, ESD training, and material evaluation.

Audits

Periodic audits ranging from daily to yearly are held to ensure that all ESD handling procedures are being followed and that all ESD materials (wrist straps, heel straps, ionizers, table mats, floor mats, etc.) are functioning properly.

TI ESD Handling Procedure

The TI worldwide ESD handling procedure is available to customers upon request.

Moisture Sensitivity of Plastic Surface-Mount Packages

Some plastic surface-mount packages are classified as moisture sensitive because the moisture that has been absorbed inside the package can expand rapidly during exposure to the fast-rise-time, high-temperature stress of reflow soldering and mechanically damage the package (often referred to as "popcorn"). Surface-mount packages are subjected to much higher solder reflow temperatures than their through-hole counterparts. The bodies of the through-hole parts are shielded from the hot-wave solder by the PC board, while surface-mount parts are subjected to the full solder reflow temperature.

All plastic packages absorb some moisture at room ambient conditions. The amount of moisture absorbed is based on a number of factors, including room temperature and humidity. However, there is no threshold level of moisture absorption or gain that applies to all plastic surface-mount packages that makes them moisture sensitive. Conversely, all plastic surface-mount packages that are essentially moisture-free during reflow soldering will be free of moisture-induced stress failures.

It is important, therefore, to know which packages are moisture sensitive so they can receive special care in handling to minimize moisture absorption and subsequent moisture-induced stress damage during the reflow soldering operation.

At TI, plastic surface-mount packages are tested for moisture sensitivity using JEDEC test method A112, Moisture-Induced Stress Sensitivity for Plastic Surface-Mount Devices. Packages that are found to be moisture sensitive are baked (to drive out the moisture) and then placed in a protective dry-pack bag that contains a humidity indicator card and sufficient desiccant to maintain a very low humidity level in the bag. A caution label (as defined in JEDEC publication 113) is attached to the bag and indicates the minimum floor life of the packages once they are removed from the protective dry environment of the bag. There are seven possible moisture sensitivity levels (two in Level 5) as shown in the table below. JEDEC publication 113 defines the labels required for each level.

LEVEL	DRY-PACK BAG/LABEL REQUIRED?	FLOOR LIFE @ 30°C, 60% RH
1	No	No limit
2	Yes	1 year
3	Yes	168 hours
4	Yes	72 hours
5	Yes	24 or 48 hours (noted on label)
6	Yes	6 hours after mandatory bake

Plastic surface-mount packages that are not moisture sensitive per JEDEC test method A112 do not need to be dry packed or handled in a special way to minimize moisture absorption prior to reflow soldering, provided that the package body temperature does not exceed 220°C during reflow soldering.

Floor life is defined as the time after the devices have been removed from the protective dry-pack bags until the devices are subjected to reflow soldering. If this floor life is exceeded, there are instructions on the dry-pack bag label indicating how long the devices must be baked, and at what temperature, to restore them to a safe condition for reflow soldering.

Dry packing is a method of controlling the moisture absorption during shipping and storage. All product that is classified as moisture sensitive with a rating of 2, or higher, is dry packed and labeled as moisture sensitive with the bag label outlining the necessary precautions for handling the product. As long as the devices are rated as moisture sensitive, dry packing is used regardless of whether the components are shipped in tubes (magazines), tape and reel, or trays. Components rated as nonmoisture sensitive (Level 1) need not be baked and dry packed.

The dry-packing process starts at the manufacturer's final packing stage. The components are initially baked and then placed inside a moisture-vapor barrier bag along with desiccant to absorb moisture and keep the humidity inside the bag at a safe level (<20% RH).

The customer should check the humidity indicator immediately after opening the bag to determine whether the moisture level has been exceeded. If the 20% dot on the humidity indicator card is pink and the 30% dot is not blue, the components have been exposed to an excessive moisture level and should be rebaked before being subjected to the surface-mount process. If baking is required, devices may be baked for:

1. 192 hours at 40°C + 5°C/–0°C and <5% RH for all component containers (tray, magazines, or tape and reel); or
2. 24 hours at 125°C ±5°C for device containers rated at 125°C or above

Moisture-sensitive components can be resealed in their original bag with the original desiccant if:

a. Humidity indicator card shows 20% RH
b. Components have not been out of the bag for more than 2 hours, and
c. Components have not been exposed to conditions greater than 30°C/60% RH

If the 2 hours of exposure is exceeded, the floor life should be adjusted accordingly. Reduce the floor-life level by 1 hour for each hour over the 2-hour limit the material is out of the bag. For example, if the rating is Level 4 and the material has been out for 4 hours, the floor life shown on the label is reduced from 72 hours to 70 hours (suggestion: close bag within 10 minutes after any opening).

Total time out of the bag is cumulative. Each time that the bag is opened and resealed, the corresponding time out of the bag should be deducted from the remaining floor life. The above process may take place repeatedly until the floor-life hours are used up, in which case rebaking of the remaining components is required. Rebaking would return the residual components to the original Level-4 status with the corresponding floor life of 72 hours.

The moisture indicator cards should be used to assist in monitoring the moisture level and maintaining control of the humidity below the 20%-RH level. If there is any doubt as to the moisture condition of the parts, baking is recommended to restore the components to a safe, usable condition, ready for board assembly.

Conclusion

Within the constraints given above, the SN54/74HC family can be regarded as a pin-for-pin equivalent to the other logic families. The SN54/74HC family is ideally suited for system upgrading, system shrinking, or especially, new system design.

SN54/74HCT CMOS Logic Family Applications and Restrictions

SCLA011
May 1996

TEXAS INSTRUMENTS

Contents

List of Illustrations

Introduction

This report describes applications, features, and system design of the SN54/74HCT high-speed CMOS family. To simplify interfacing of TTL outputs to high-speed CMOS inputs, Texas Instruments (TI) introduced HCT circuits, a subgroup of its HC family. HCT features and functions are identical to HC devices with the exception of modified input circuitry which makes the input threshold voltage compatible with TTL circuits. HCT outputs are similar to the HC family.

The TTL/HC Interface

TTL output voltages and HC input voltages are incompatible, especially between the TTL high-level output voltage (V_{OH}) and the HC high-level input voltage (V_{IH}). This problem can be solved in three different ways. The first way is to use HCT devices with their TTL-compatible input voltages to interface between TTL and HC circuits. Another solution is to provide pullup resistors at the TTL outputs to ensure an adequate high-level TTL output voltage. The third method requires the use of level shifters.

Of the three alternatives mentioned, using HCT circuits to solve the incompatibility problem is the most convenient. Designed to meet the requirements of this application, HCT devices allow the engineer to benefit from the advantages of HC devices (low power consumption) without using discrete components such as pullup resistors.

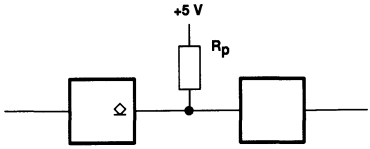


Figure 1. TTL-CMOS Interface With Open-Collector Output and Pullup Resistor

Using pullup resistors to accommodate TTL output signals to interface with HC input circuits (see Figure 1), the design engineer has to choose the resistance that is appropriate for the application. The minimum value of the resistor is determined by the maximum current I_{OL} that a TTL circuit can supply at the low-level output (V_{OL}).

$$R_p\text{min} = \frac{V_{CC}\text{max} - V_{OL}\text{min}}{I_{OL} + n \times I_{IL}} \quad (1)$$

where n is the number of HC inputs to be driven, and I_{IL} is their input current. I_{IL}, having a value of only a few nanoamperes, is negligible in all calculations.

In the case of a SN74ALS03, the following equation defines $R_p$min:

$$R_p\text{min} = \frac{5.5\ \text{V} - 0.4\ \text{V}}{8\ \text{mA}} = 640\ \Omega \quad (2)$$

To calculate the upper limit of this resistor, a sufficient V_{IH} high level must be ensured.

$$R_p\text{max} = \frac{V_{CC} - V_{IH}\text{min}}{n \times I_{IH}} \quad (3)$$

In this situation, the input current of HC devices is negligible and very high values are also obtained.

When calculating the maximum allowable resistance, it is important to ensure that the maximum allowable rise time (t_r = 500 ns) at the HC input is not exceeded. The following equation then applies:

$$V_{IH} = V_{CC}\left(1 - e^{\frac{-t}{R_p \times C}}\right) \quad (4)$$

where C is the total load capacitance in the circuit. C is composed of the output capacitance of the driving gate (≈10 pF), the total input capacitances of gates to be driven (≈5 pF each), and the line capacitance (≈1 pF/cm). The actual value is calculated by solving the equation for R_p:

$$R_p = \frac{-t}{C \times \ln\left(1 - \frac{3.5\ V}{5\ V}\right)} \quad (5)$$

Assuming the total capacitance, C, is 30 pF, the maximum resistor is:

$$R_p = \frac{-500\ ns}{30\ pF \times \ln\left(1 - \frac{3.5\ V}{5\ V}\right)} = 14\ k\Omega \quad (6)$$

Faster rise times result in lower impedance and more power consumption. The previous calculation is based on the assumption that the driving gate has an open collector. Conditions become more satisfactory, however, when a gate with totem-pole output (i.e., SN74ALS00) is used. In that case, the gate output provides the voltage to be brought up to the value V_{OH} = 2.7 V in less than 10 ns (the rise time of the TTL signal). The pullup resistor only has to pull the level to 3.5 V within the desired time. According to the previous formula, and with a required rise time of t_r = 50 ns, the resistor is defined by the following calculation:

$$R_p max = \frac{-50\ ns - 10\ ns}{30\ pF \times \ln\left(1 - \frac{3.5\ V - 2.7\ V}{5\ V - 2.7\ V}\right)} = 3.12\ k\Omega \quad (7)$$

The upper limiting value of the resistor is primarily dictated by the rise time required. The larger the resistance, the longer the rise times and propagation delay times. Reducing the resistance increases speed and power dissipation.

The third method of accommodating TTL signals to HC circuits is accomplished with special level shifters. This solution is not recommended because the level shifter itself has no inherent logic functions and increases component and space requirements.

For design engineers, using HCT circuits to match TTL signal levels with HC devices is the most convenient and efficient way of solving incompatibility problems. HCT devices contain the necessary level shifters and additional logic functions in a single circuit. Furthermore, the designer is not forced to compromise among signal rise time, system speed, and power consumption of the stages.

Operating Voltages of HCT Circuits

HCT circuits feature a limited operating voltage range due to the fact that they have to work with TTL voltage levels. Since internal switching layout is equivalent to HC circuits (with the exception of the input stage), these components could be operated from a 2-V to 6-V range. For HCT circuits operating at less than 4.5 V, the load-level noise margin is reduced and becomes incompatible with TTL thresholds, thus losing one of the primary advantages of the HCT devices.

Noise of HCT Circuits

The noise margin of a logic family is a very important consideration in system design. Composed of low-level and high-level noise margins, each of these components has to be considered separately. The high-level noise margin is the voltage difference between the guaranteed output voltage (V_{OH}) of the driving gate and the guaranteed input voltage (V_{IH}) of the triggered gate. Accordingly, the low-level noise margin can be defined as the voltage difference between the guaranteed output voltage (V_{OL}) and the input voltage, V_{IL} (see Figure 2).

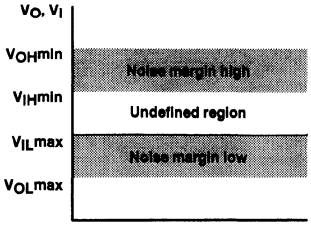


Figure 2. Noise Margin

Regarding magnitude relations, it is desirable to keep both noise margins as large as possible and the undefined range between them as narrow as possible. If the noise margin is not large enough in a certain application, internally or externally sourced interference can modify (i.e., falsify) a signal to fall within the undefined range. Internal noise is caused by inductive or ohmic drops or by inductive and capacitive couplings with other signaling lines. The coupling between signal lines is the more critical aspect in most cases. Figure 3 shows the voltage conditions for HC, HCT and TTL circuits.

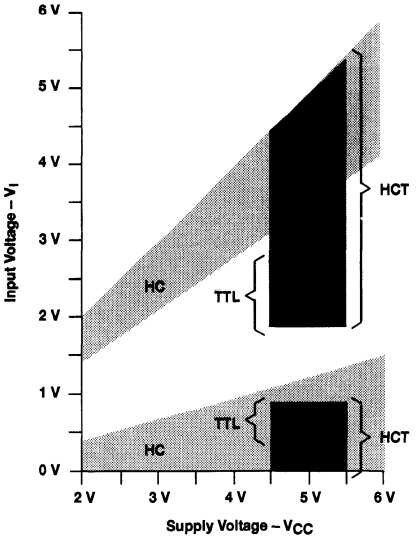


Figure 3. Guaranteed Noise Margins for HC, HCT, and TTL Devices

Since a certain percentage is always transmitted from the noise-emitting line to the interfered line, it is not the absolute noise margin (in volts) that is of consequence, but rather the quotient of the absolute noise margin and the signal-voltage swing. The percentile high- and low-level noise margins (S) would be defined by the following equations:

$$S_H = \frac{V_{OH} - V_{IH}\text{min}}{V_{OH} - V_{OL}} \times 100\% \quad (8)$$

$$S_L = \frac{V_{IL}\text{max} - V_{OL}}{V_{OH} - V_{OL}} \times 100\% \quad (9)$$

To obtain realistic values, the guaranteed V_{OH}min and V_{OL}max data sheet voltage values must not be used when calculating signal deviation $V_{OH} - V_{OL}$. Data-sheet specifications would indicate a smaller signal deviation and thus a wider noise margin. V_{OH} and V_{OL} values should be based on the low- and high-level voltages supplied by the circuit under normal operating conditions. The following table lists the different voltages for HC, HCT, and TTL circuits, and the resulting noise margins. All calculations use a supply voltage of V_{CC} = 5 V to achieve comparable results.

Table 1. Voltage Levels and Noise Margins

	HC	HCT	TTL	UNIT
V_{OH}typ	4.9	4.9	3.4	V
V_{OL}typ	0.1	0.1	0.3	V
Signal voltage swing V_{OH}typ – V_{OL}typ	4.8	4.8	3.1	V
V_{IH}min	3.5	2.0	2.0	V
V_{IL}max	1.0	0.8	0.8	V
S_H V_{OH}min – V_{IH}min	1.4	2.9	0.7	V
S_L V_{IL}min – V_{OL}min	0.9	0.7	0.4	V
S_H	29.1	60.4	22.5	%
S_L	18.7	14.6	12.9	%

As you see, the low-level noise margin (S_L) is the most critical value for all three logic families, ranging from 18.7% (HC) to 12.9% (TTL). With respect to noise margins, HC devices feature significantly better performance than bipolar logic circuits. In practice, however, the ability of individual circuits to attenuate the noise impressed into a line is the most important. The test setups in Figures 4 and 5 are used to measure the actual noise margin expected in a system. The measured value refers to the crosstalk between two parallel lines. Twenty-five centimeters, usually the maximum length that occurs on a printed circuit board, is regarded as a basic line length.

In Figure 4, the signals are propagating across the line in the same direction. A noise that is induced by line 1 on to line 2 is immediately shorted by the low output impedance of the gate. Signal A in Figure 4 shows the signal on the noise-emitting line, and signals B and C show the noise generated on line 2 at the low and high levels. Both HC and TTL maintain noise values that stay below their allowable limits.

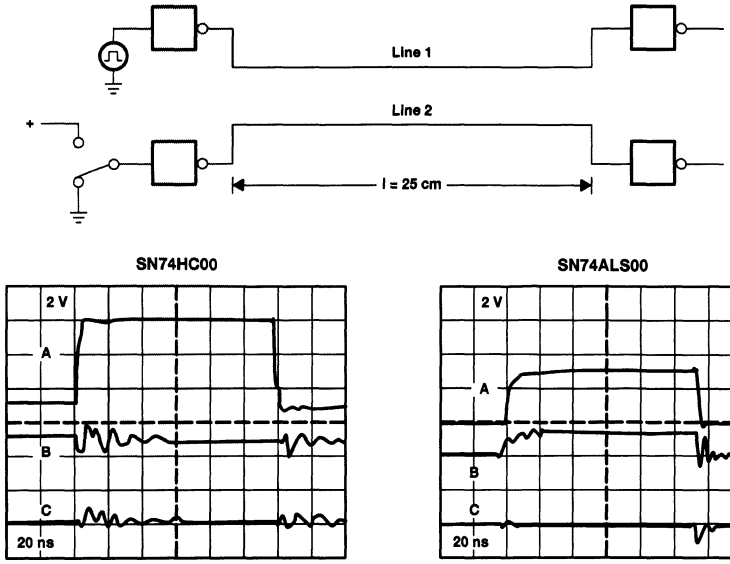


Figure 4. Crosstalk (First Case)

The same configuration is used in the second case, but signals on both lines propagate in opposite directions. A noise impressed on the parallel-running line by the interfering line is not attenuated immediately because at that place the line is terminated by its high-impedance input only. The noise becomes more effective and runs across the line up to the driver output. The low output impedance of the driver output shorts the noise to a large extent. The attenuated interfering signal is reflected at the beginning of the line, and then, after double signal propagation time, the noise is eliminated at the end of the interfered line as well. Due to the larger signal swing (deviation) of HC circuits (4.8 V) as opposed to TTL devices (3.5 V), a larger noise amplitude can be expected. This value does not fully explain the significant amplitude differences in the oscillographs shown in Figure 5. In this case, the output impedance at the low level is significantly lower for TTL circuits (R_i = 10 Ω) as compared to HC devices (R_i = 50 Ω).

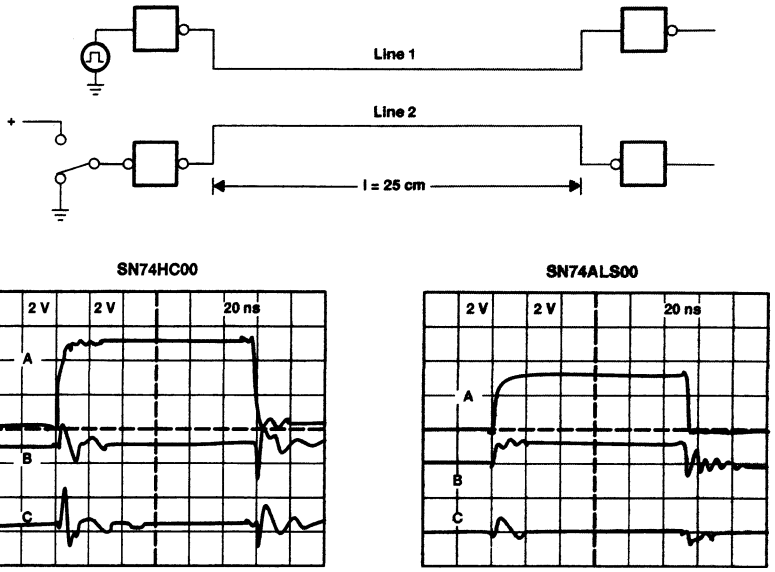


Figure 5. Crosstalk (Second Case)

In addition, the slew rate of the edge (dv/dt), particularly the positive edge of HC circuits, is significantly larger in value compared to TTL circuits. However, HC devices usually operate without interference because the typical threshold voltage at HC circuit inputs amounts to 2.5 V, and this value is not reached in the demonstrated examples. In contrast, the noise amplitude of HCT circuits significantly exceeds the typical threshold voltage of 1.5 V.

To summarize, inherent noise remains below the critical limits within a pure TTL or HC system. When HCT devices are used, the maximum line length should not exceed 10 cm to maintain crosstalk below critical values. Because the logical application of HCT devices is interfacing between HC and TTL circuits, and line lengths are normally shorter, this requirement presents no serious restriction.

Power Consumption of HCT Circuits

The threshold voltage of a CMOS circuit is determined by the geometry of the input transistors. These transistors are designed to sink the same input current at the required threshold voltage. The resulting voltage at the output is equivalent to 50% of the supply voltage V_{CC}. For an HC circuit, the channel width of the p-channel transistor of the input is approximately twice the value of an n-channel transistor. The purpose is to make both transistors have the same current characteristics, thus making the threshold voltage of their input at about 50% of the supply voltage V_{CC}. This circuit area has been modified for HCT devices: the n-channel transistor is about seven times wider than the p-channel transistor (see Figure 6). This shifts the threshold voltage in a way that it amounts to 30% of the supply voltage. At a supply voltage $V_{CC} = 5$ V, the threshold voltage is $V_T = 1.5$ V, similar to the threshold voltage of TTL circuits.

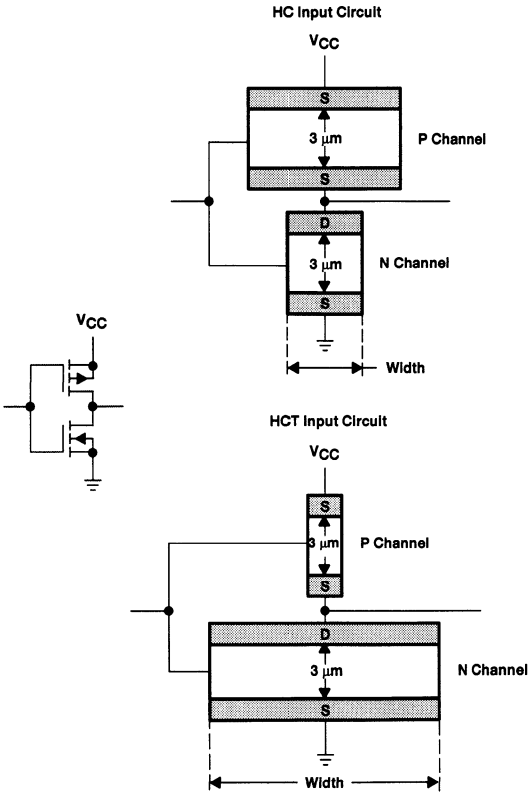


Figure 6. Input-Stage Structure of HC and HCT Circuits

Some compromises are necessary for HCT circuits to reach the parameters required. An unlimited size reduction of the p-channel transistor is impossible without reducing the drain current and thus the whole circuit speed. This is why the n-channel transistor must be enlarged to shift the threshold voltage accordingly. The result is that the supply current of the circuit rises (see Figure 7) if the input voltage is not equal to the supply voltage (p-channel transistor off) or to ground potential (n-channel transistor off). In this case, both transistors are conducting, especially when HCT circuits are triggered by TTL voltage levels. TI includes the parameter ΔI_{CC} for HCT circuits, a value that specifies the increase of the supply current I_{CC} if driven by TTL levels ($V_{IL} = 0.4$ V, $V_{IH} = 2.4$ V). This parameter allows the circuit design engineer to calculate the expected power consumption.

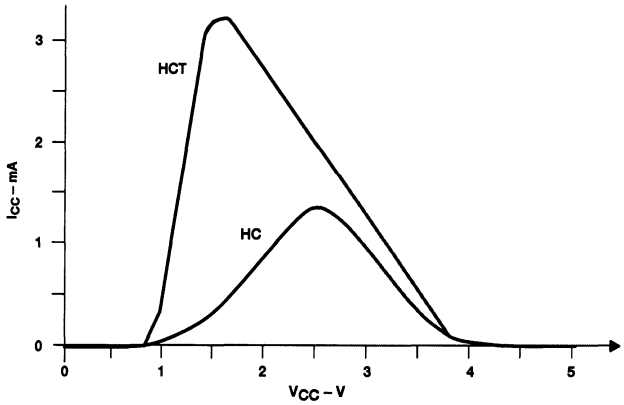


Figure 7. Supply Current as a Function of the Input Voltage

Figure 8 shows the effects of power consumption in a complete system. It shows power consumption of an SN74HCT243 with all four inputs triggered. In one case, the input signal has HC levels (V_{IL} = 0 V, V_{IH} = 5 V); in the other case, TTL levels (V_{IL} = 0.4 V, V_{IH} = 2.4 V). The duty cycle of the input signal is 50%. Each output has a load C_L = 50 pF. As you see, supply current is about 4 mA higher for a device triggered by TTL levels.

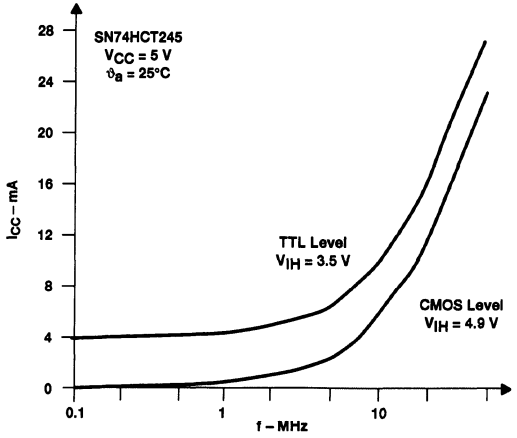


Figure 8. Current Consumption as a Function of Frequency

For frequencies above 5 MHz, this effect is of secondary importance, since current consumption is then determined primarily by the power required for reversing the charge of the load capacitance. Moreover, the increase of current consumption for devices driven by TTL levels is much lower in practice. The reason is that TTL circuits supply a typical voltage swing that is significantly higher than the data sheet value used for the measurement in Figure 8.

Delay Times

Another restriction in the use of HCT circuits results from increased transmission delay times. Although these circuits do not contain more stages than HC devices, the time of reversing charge at the output of the first stage is extended because of the smaller p-channel transistor and the higher capacitance of the n-channel transistor. This prolongs the delay time approximately 1–2 ns for HCT circuits as compared to HC circuits.

Bergeron Analysis

The speed of the ALS and HC logic families and the associated higher slew rate (especially for HC devices) force the system design engineer to carefully evaluate the behavior of electrical waves on the lines. In addition, line reflections have to be considered when the rise and fall times of logic signals are faster than the propagation time of signals on unterminated lines. Under certain circumstances, these reflections can distort the transferred signals so that the receiver at the other end of the line cannot recognize the signal.

Because digital circuits have no linear input and output characteristics, the equations known for evaluating line reflections are not applicable. A better solution is to use the Bergeron diagram, a graphical method that supplies results with sufficient precision for the examples in question. Figure 9 shows the high- and low-level output characteristics of an SN74ALS245A, as well as the input characteristic of an HC device. Because the input current of these circuits is very low (and negligible), this characteristic coincides with the V axis in the range from 0–5 V. The voltage curve at transmitter and receiver for the positive and negative edges is obtained by drawing the resistance line with slope Z_O and $-Z_O$ onto the graph (see Figure 10). Both cases achieve voltages that fall within the required limits (V_{IL}max = 0.8 V, V_{IH}min = 2.0 V), and the undershoot at the negative edges at the right sides of the pulses is sufficiently damped by the diodes integrated into the input circuitry of HC devices.

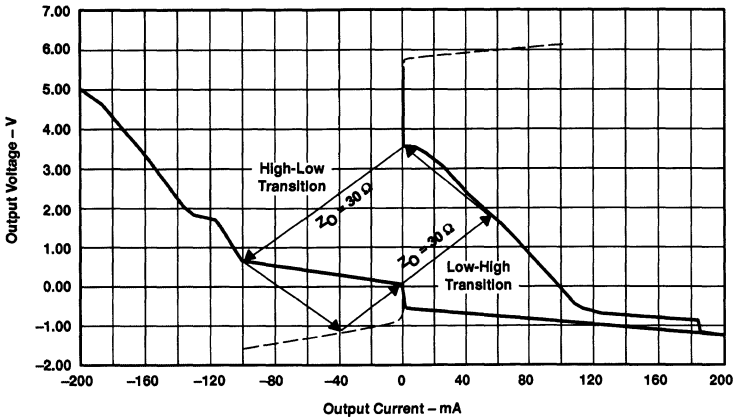


Figure 9. Bergeron Diagram, SN74ALS245 Driver

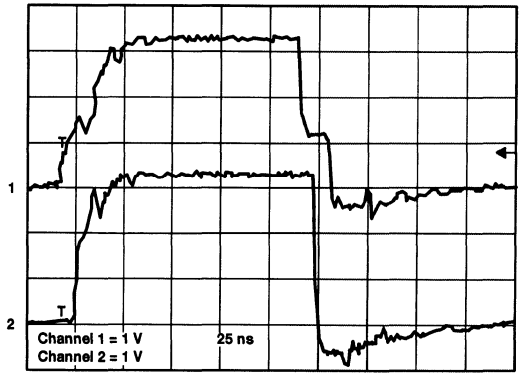


Figure 10. Line Reflections, SN74ALS245 Driver

Figures 11 and 12 show the associated diagrams for an HC or an HCT driver. There is no problem with the positive-going edge. At the line end, a voltage of 3.5 V is applied which is a valid high for both HC and HCT. At the negative edge, the voltage at the line end reaches a level of approximately 1 V. This value is sufficient to drive an HC circuit, but cannot securely drive an HCT device that requires a low-level value below 0.8 V.

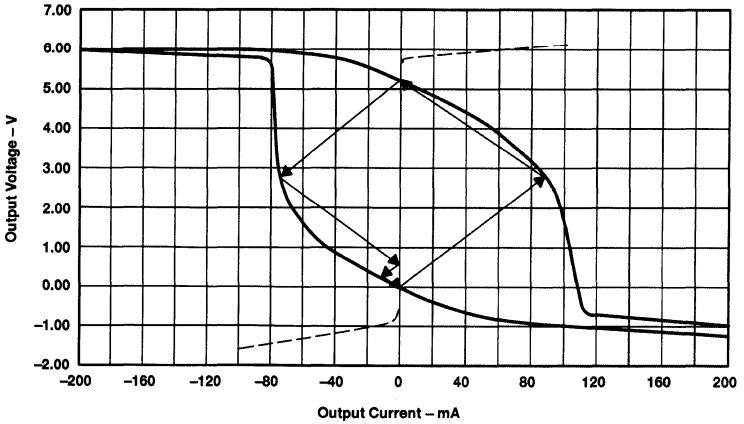


Figure 11. Bergeron Diagram, SN74HC245 Driver

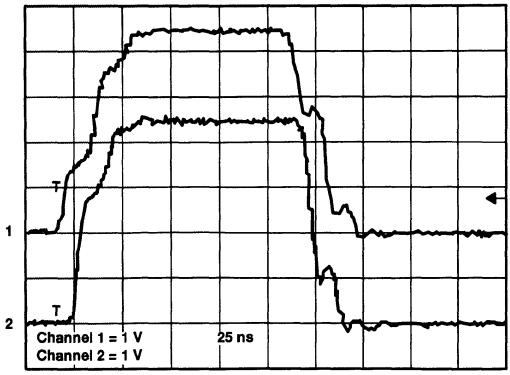


Figure 12. Line Reflections, SN74HC245 Driver

Summary

The SN74HCT circuit family from TI is a subgroup of the SN74HC series. Whereas devices of both families are equivalent in their features and functions, the HCT input circuitry was modified to meet interfacing requirements. These devices can be driven by TTL circuits directly, without the need for additional components. Thus, the HCT family offers an ideal, simple, and cost-effective solution for mixing systems using both TTL and HC devices. However, employing HCT instead of HC devices in pure CMOS systems cannot be recommended. There are several advantages in using HC technology, such as the broad supply-voltage range and the reduction of any adverse effect caused by the lower switching threshold on dynamic behavior. Due to the lower noise margin, there is an increased risk of interference caused by crosstalk, especially when the lines on the printed circuit board exceed a certain length. Moreover, the reduced switching threshold no longer ensures faultless operation of advanced bus systems used in microprocessor applications today.

Using High-Speed CMOS and Advanced CMOS Logic in Systems With Multiple V_{CC} Supplies or Partial Power Down

Rick Curtis
Texas Instruments Incorporated

SCLA008
April 1996

TEXAS INSTRUMENTS

Using High-Speed CMOS and Advanced CMOS Logic in Systems With Multiple V_{CC} Supplies or Partial Power Down

CMOS devices offer a designer many desirable features, the most important one being low-power consumption. However, in some systems a designer finds that even the low-power consumption of CMOS is insufficient to meet power supply constraints. Therefore, some designers use partial system power-down or multiple V_{CC} supplies to meet their system power requirements.

When a system uses multiple V_{CC} supplies or partial power down, designers must take into account several important device parameters when high-speed CMOS (HC) or advanced CMOS (ACL) devices are used. This is necessary to avoid excessive power dissipation and prevent damage that could lead to a degradation in the reliability of the device. These parameters are the continuous input and output diode currents (I_{IK} and I_{OK}) and the continuous output current (I_O). I_{IK} and I_{OK} refer to the continuous current flowing through the input and output electrostatic discharge (ESD) protection circuits. Figure 1 shows functionally equivalent schematics of the ESD structures for HC and ACL devices.

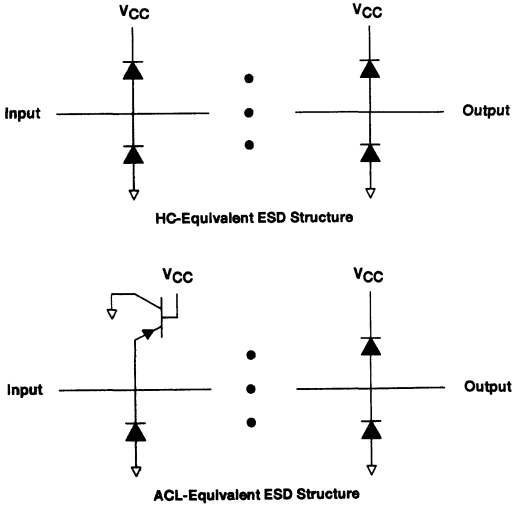


Figure 1. Simplified ESD Structures for HC and ACL Devices

I_O is the continuous current flowing through one of the two output transistors. Table 1 shows the absolute maximum rating for I_{IK}, I_{OK}, and I_O for both HC and ACL devices, as listed on device data sheets.

Table 1. Absolute Maximum Values for I_{IK}, I_{OK}, and I_O

PARAMETER	ABSOLUTE MAXIMUM	
	HIGH-SPEED CMOS (HC)	ADVANCED CMOS (ACL)
I_O	±25 mA (standard) ±35 mA (high-current)	±50 mA
I_{IK}	±20 mA	±20 mA
I_{OK}	±20 mA	±20 mA

To understand how I_{IK}, I_{OK}, and I_O can affect a system design, consider an example of a partial system power down. Figure 2 shows a partial power-down situation where a device powered with V_{CC} = 5 V is driving a device without power applied. The input voltage to the nonpowered device exceeds V_{CC} by more than the threshold voltage (0.6 V to 0.8 V), causing the ESD protection structure to conduct whenever the output of the driver is in a high state. Therefore, the driving device powers up the receiving device and any other device sharing the same V_{CC} line. If no current limiting is provided, the maximum I_O of the driving device and the maximum I_{IK} of the receiving device could be exceeded.

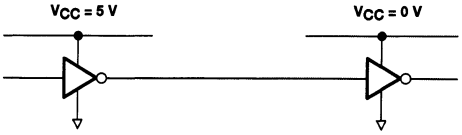


Figure 2. Example of Partial System Power Down

Several methods are available to protect the driving and receiving devices during partial system power down. If the driving device has 3-state outputs, placing the outputs in the high-impedance state provides the best solution. However, if this is not a viable option, some method of current limiting must be provided. Figure 3 shows several methods that can be used, with current-limiting series resistors being the simplest. The value of the resistor is chosen to limit the current into the receiving device to less than 20 mA. The major drawback to using a current-limiting resistor is power dissipation. Another drawback is the effect that the resistor has on the input transition time at the receiving device during normal system operation. If the total capacitance of the interconnects and receiving devices is high (i.e., a high-capacitance bus), a current-limiting resistor increases the input transition time. A system designer must ensure that the addition of the resistor does not increase the input transition time above the maximum input transition time of the receiving device.

A second method of current limiting involves the use of a pullup resistor and a diode (see Figure 3). The advantage of this method is that it allows the use of a large resistance, thereby holding power dissipation to a minimum. The disadvantage of this method is that it requires the use of additional components and results in a higher value of V_{IL} at the receiving device.

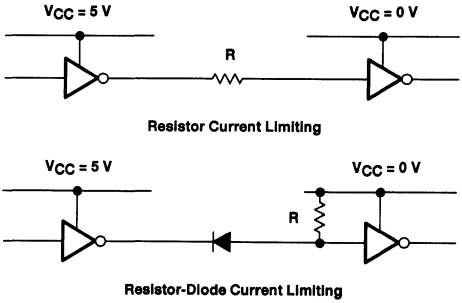


Figure 3. Current Limiting for a Partial System Power Down

A second example of how a partial power down can cause unwanted operation is the case of two drivers connected to the same bus with one device powered down, as shown in Figure 4. In this case, the first bus driver attempts to power up the second bus driver and any other devices sharing the same V_{CC} line through the output ESD structure of the unpowered device.

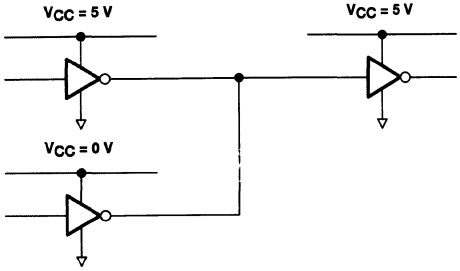


Figure 4. Partial Power Down With Bus Drivers

Several methods are available to solve this type of problem. One method is simply to use a current-limiting resistor as outlined above. Another solution is to isolate the unpowered driver from the V_{CC} line by putting a diode between the power pin and the V_{CC} supply. If the unpowered device is a transceiver, pullup or pulldown resistors are required on the output control inputs to disable the outputs. Not disabling the transceiver outputs allows the transceiver to power up the unpowered devices that are driven by its outputs. When an isolating diode is used, the V_{CC} at the driver is always a diode forward drop below the voltage of the supply, resulting in a degradation of V_{OH}. Figure 5 illustrates these circuit solutions.

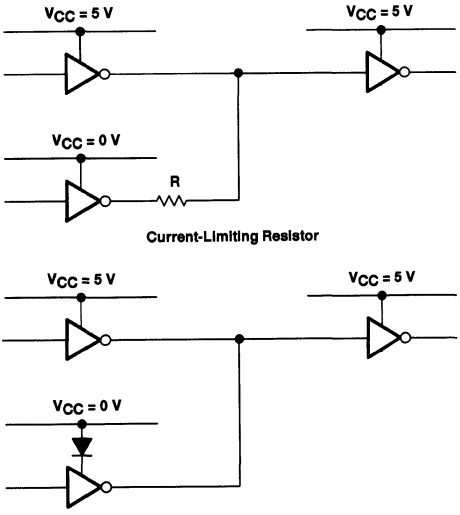


Figure 5. Current Limiting for Bus Drivers During Partial Power Down

Another example of a system that could require current-limiting protection is one that uses multiple V_{CC} supplies, or a system that provides each card with its own on-board voltage regulator. If the V_{CC} supplies of two connecting devices differ by more than 0.5 Vdc, a current-limiting scheme should be considered if the driving device is a CMOS device and is connected to the high V_{CC}. This is necessary because V_{OH} of a CMOS device is the same as V_{CC} when the I_{OH} requirement is very small. Therefore, the input ESD protection diode could conduct if the V_{CC} of the driver (or V_{OH}) exceeds the V_{CC} of the receiver by more than 0.5 Vdc. The resulting current flow causes the degradation of the diode, not the voltage.

NOTE: This applies only to supplies that vary by more than 0.5 Vdc. Dynamic switching currents could cause transient voltage spiking on V_{CC} lines such that a 0.5-V difference between supplies could easily exist. These transients do not cause a problem if they have a short duration (less than 20 ns).

Partial system power down offers a designer a convenient method to save on system power consumption. However, when a partial power-down scheme is used, a designer must ensure that no damage occurs to devices and that excessive power dissipation is avoided. The designer must also take similar precautions when using multiple V_{CC} supplies if the supplies of two connecting devices differ by more than 0.5 Vdc.

Contents

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a three-part type number as explained in the following example.

EXAMPLE: SN 74AHC244 DB LE

Prefix

SN = Standard prefix
SNJ = MIL-STD-883 processed and screened per JEDEC Standard 101

Unique Circuit Description

MUST CONTAIN SIX TO ELEVEN CHARACTERS

Examples: 74LV00
74AHCT16245

Package

MUST CONTAIN ONE TO THREE LETTERS

D, DW = plastic small-outline package
DB, DL = plastic shrink small-outline package
DBV = plastic small-outline transistor package
DGG, PW = plastic thin shrink small-outline package
FK = leadless ceramic chip carrier
J, JT = ceramic dual-in-line package
N, NT = plastic dual-in-line package
W, WD = ceramic flat package
(from pin-connection diagram on individual data sheet)

Tape and Reel Packaging

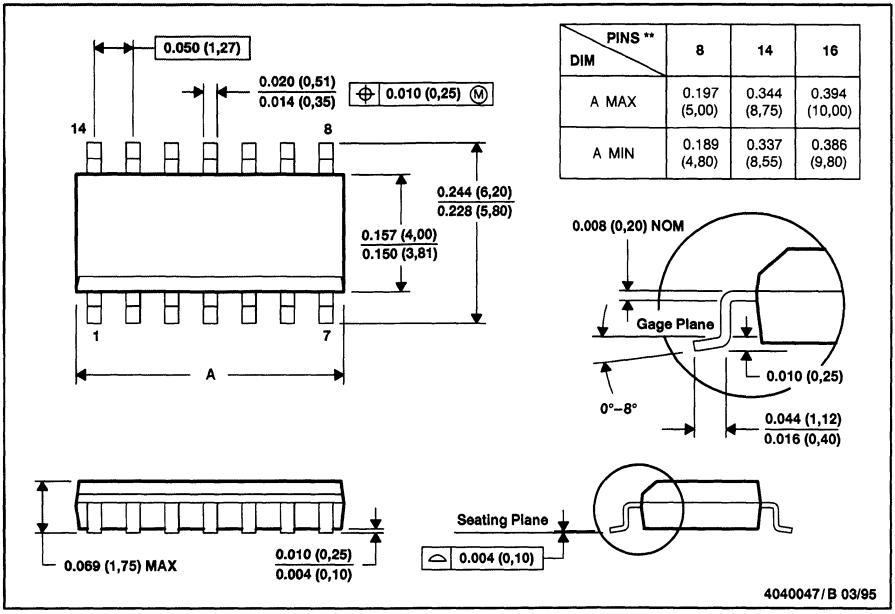
Valid for surface-mount packages only. All orders for tape and reel must be for whole reels.

MUST CONTAIN ONE OR TWO LETTERS

LE = Left embossed tape and reel (required for DB and PW packages)
R = Standard tape and reel (optional for D and DW packages)

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN

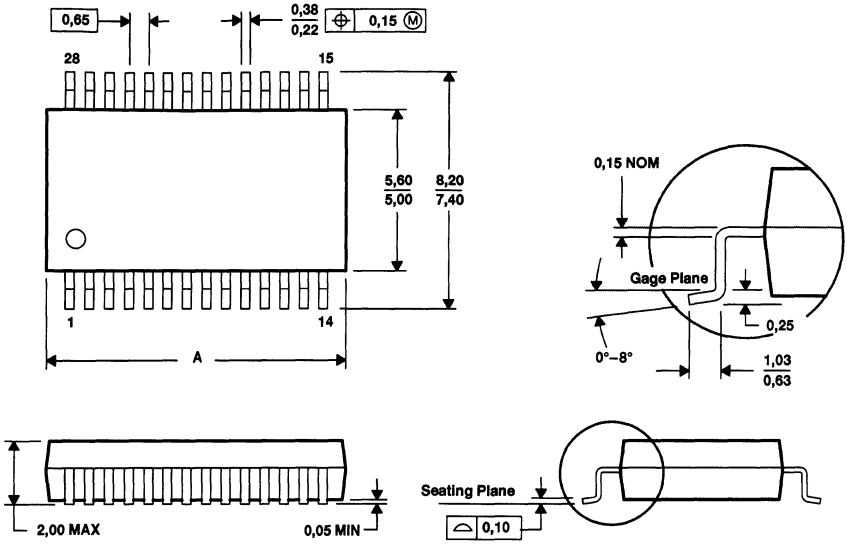


DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Four center pins are connected to die mount pad.
E. Falls within JEDEC MS-012

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

28 PIN SHOWN

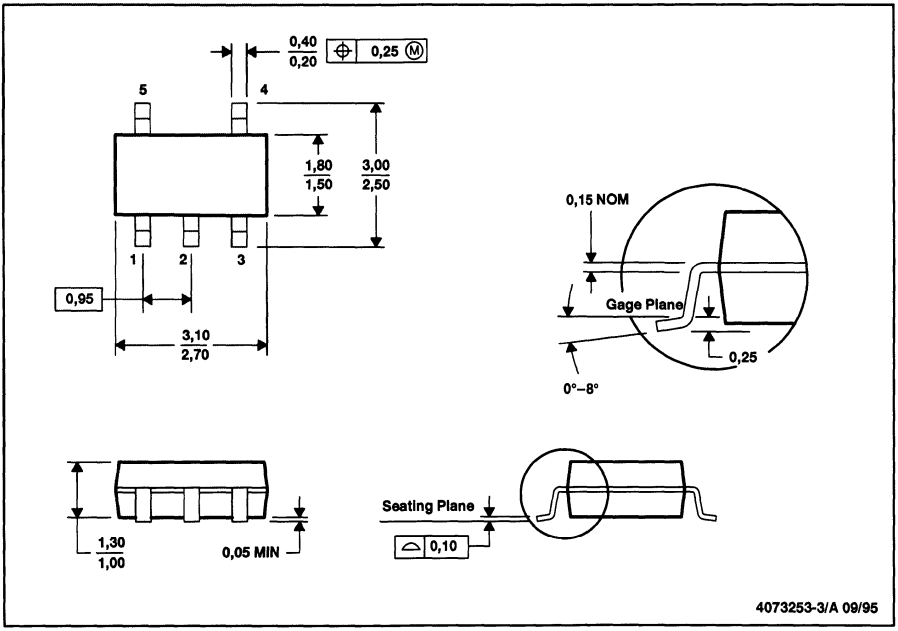


DIM \ PINS **	8	14	16	20	24	28	30	38
A MAX	3,30	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	2,70	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 / C 10/95

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

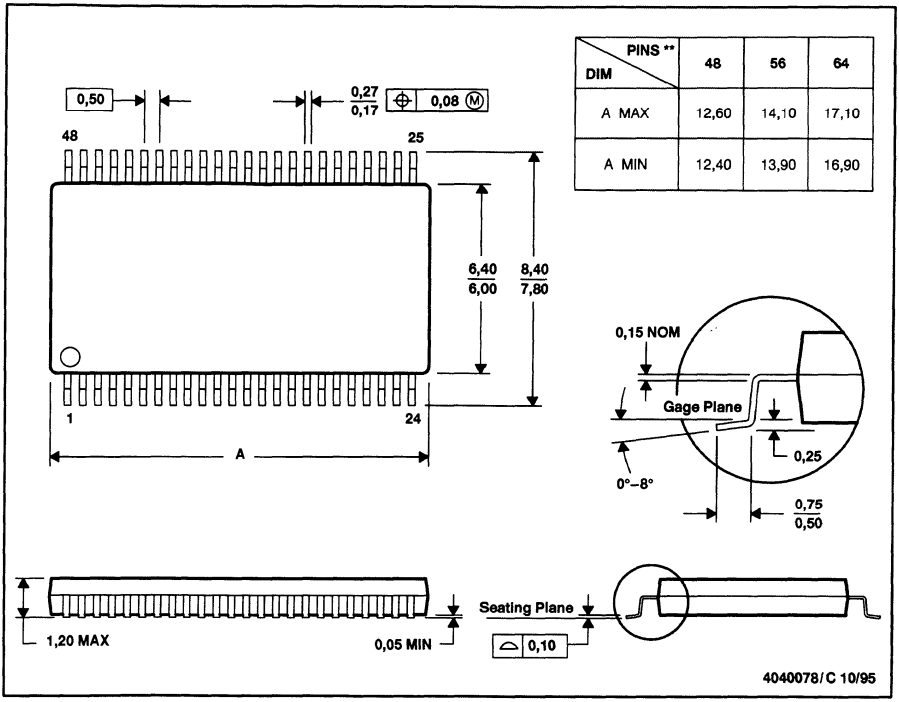
DBV (R-PDSO-G5) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PIN SHOWN

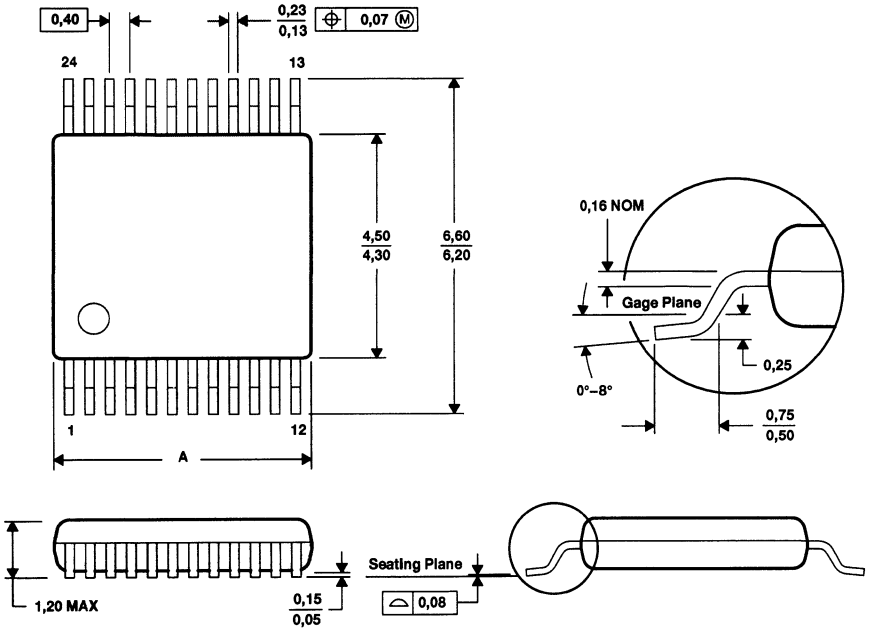


DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-153

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

24 PIN SHOWN



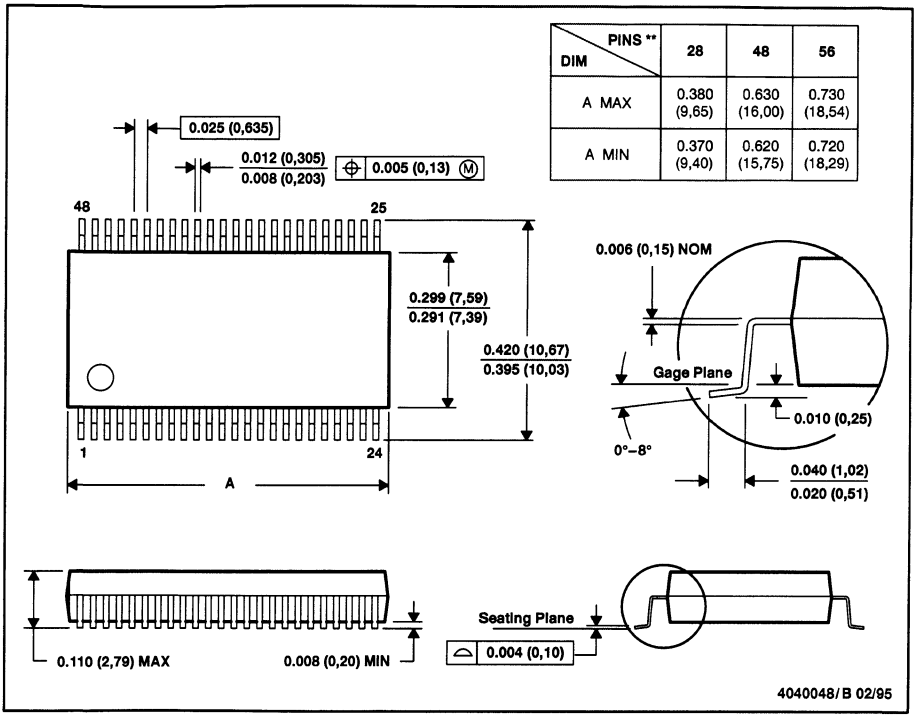
DIM \ PINS **	14	16	20	24	48	56
A MAX	3,70	3,70	5,10	5,10	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	9,60	11,20

4073251/A 08/95

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

DL (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PIN SHOWN

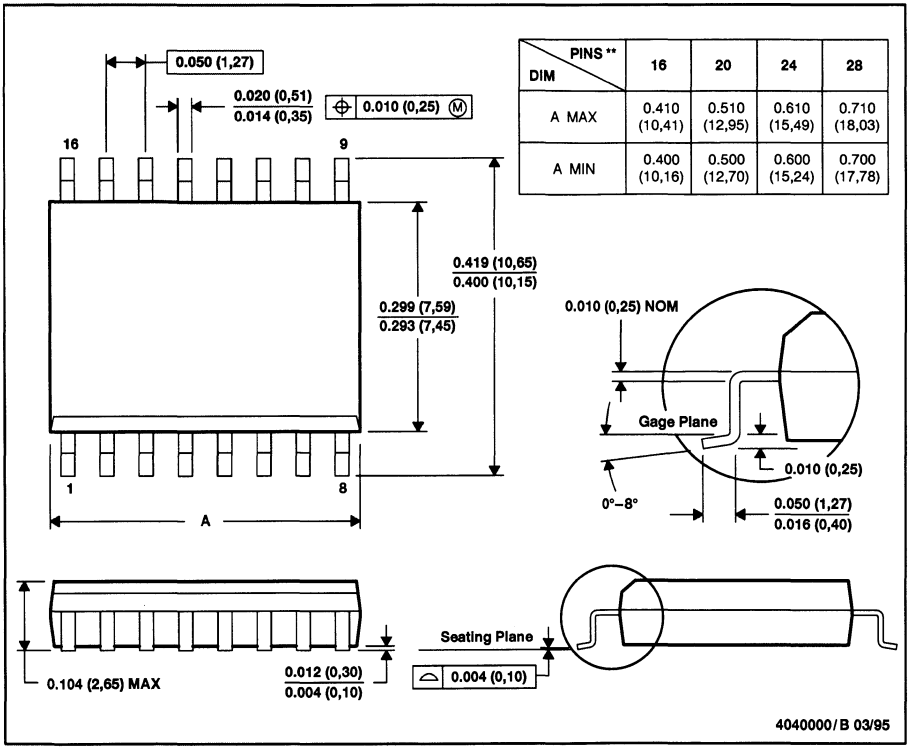


DIM \ PINS **	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PIN SHOWN

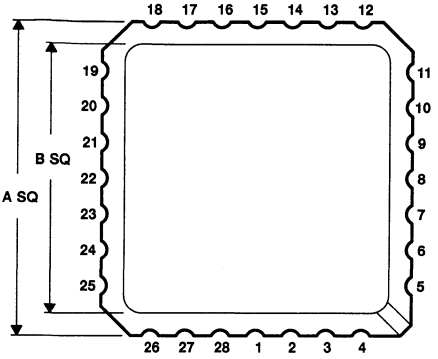


DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

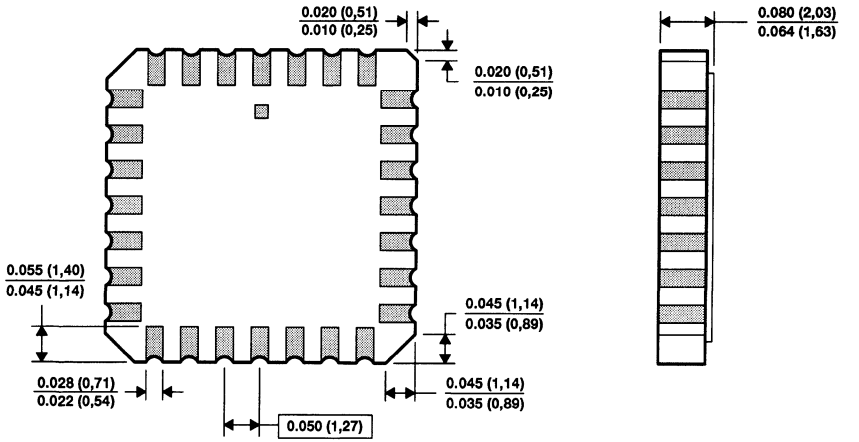
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

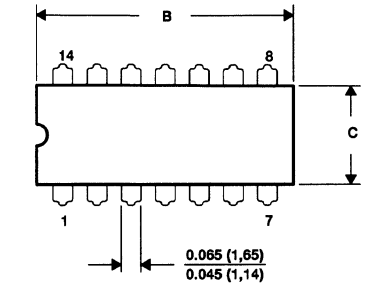


4040140/C 11/95

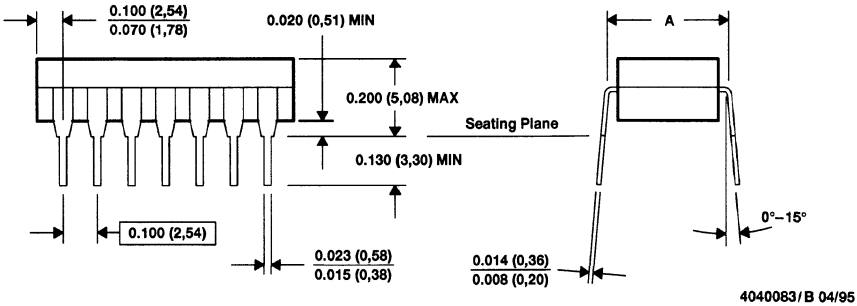
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

J (R-GDIP-T)** **CERAMIC DUAL-IN-LINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	14	16	18	20	22
A MAX	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.410 (10,41)
A MIN	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.390 (9,91)
B MAX	0.785 (19,94)	0.785 (19,94)	0.910 (23,10)	0.975 (24,77)	1.100 (28,00)
B MIN	0.755 (19,18)	0.755 (19,18)	—	0.930 (23,62)	—
C MAX	0.280 (7,11)	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)	0.388 (9,65)
C MIN	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	—



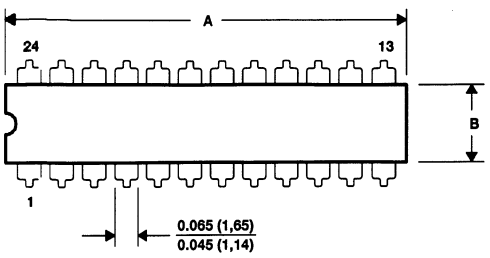
4040083/B 04/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL-STD-1835 GDIP1-T14, GDIP1-T16, GDIP1-T18, GDIP1-T20, and GDIP1-T22

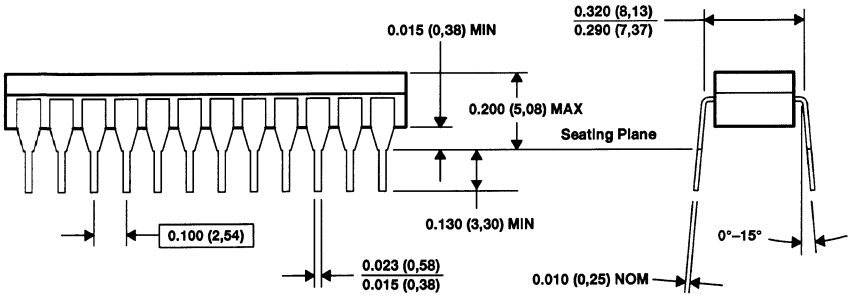
MECHANICAL DATA

JT (R-GDIP-T)** **CERAMIC DUAL-IN-LINE PACKAGE**

24 PIN SHOWN



DIM \ PINS**	24	28
A MAX	1.280 (32,51)	1.460 (37,08)
A MIN	1.240 (31,50)	1.440 (36,58)
B MAX	0.300 (7,62)	0.291 (7,39)
B MIN	0.245 (6,22)	0.285 (7,24)



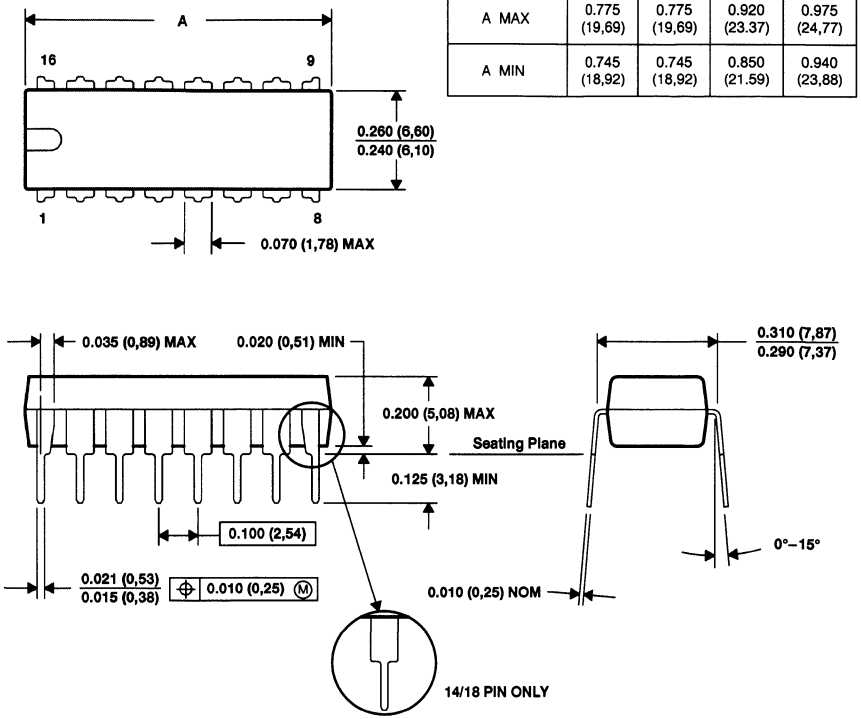
4040110/B 04/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL-STD-1835 GDIP-T24 and GDIP-T28 and JEDEC MO-058AA and MO-058AB

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PIN SHOWN

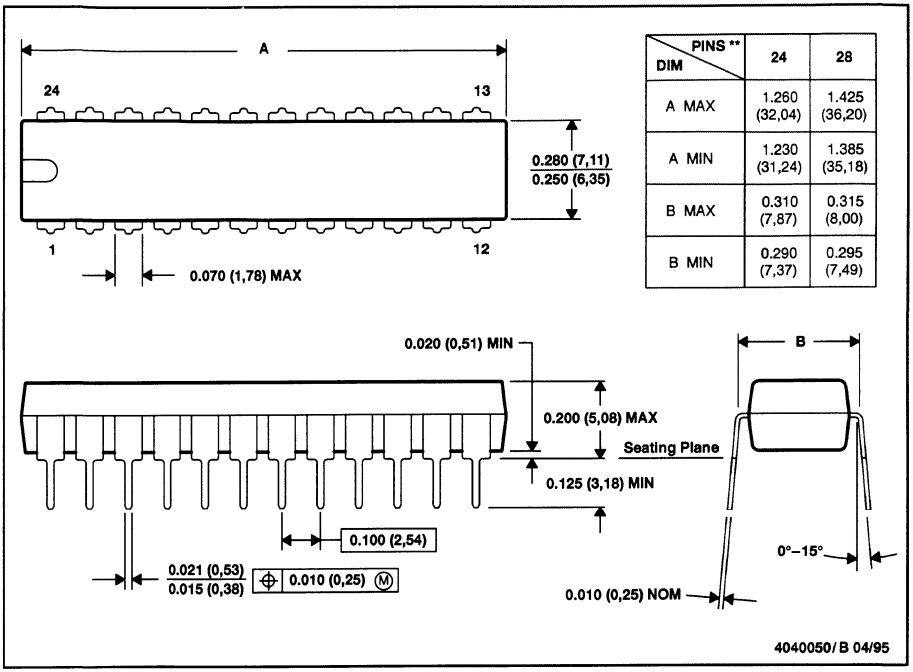
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20 pin package is shorter then MS-001.)

NT (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

24 PIN SHOWN

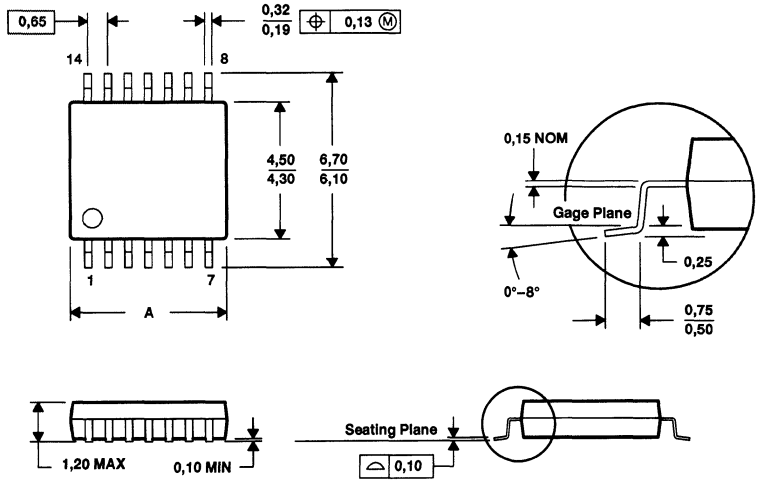


DIM \ PINS **	24	28
A MAX	1.260 (32,04)	1.425 (36,20)
A MIN	1.230 (31,24)	1.385 (35,18)
B MAX	0.310 (7,87)	0.315 (8,00)
B MIN	0.290 (7,37)	0.295 (7,49)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



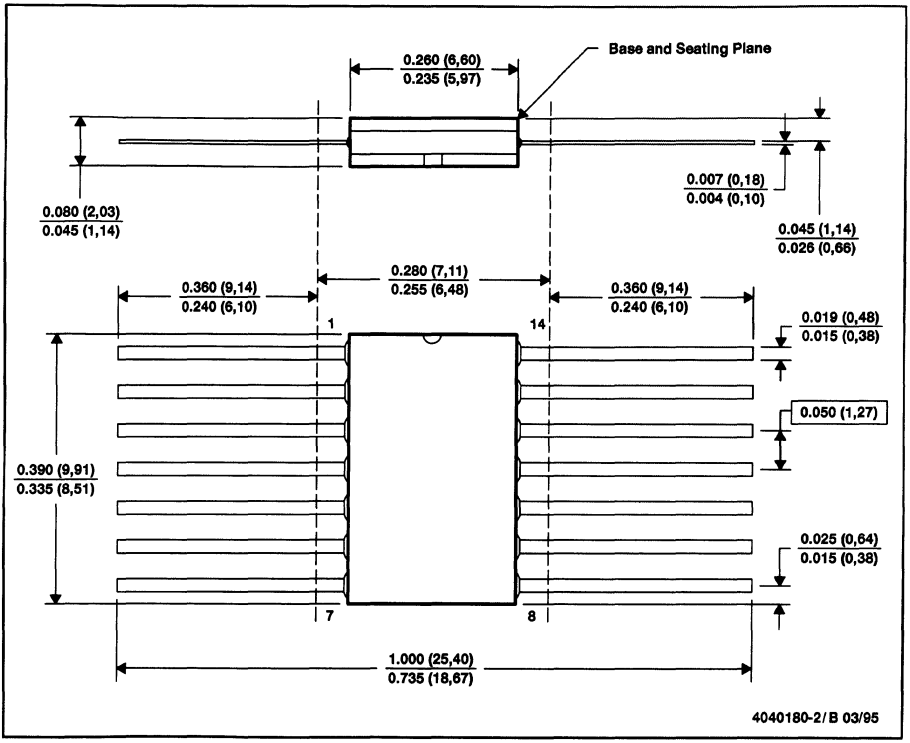
DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/D 10/95

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

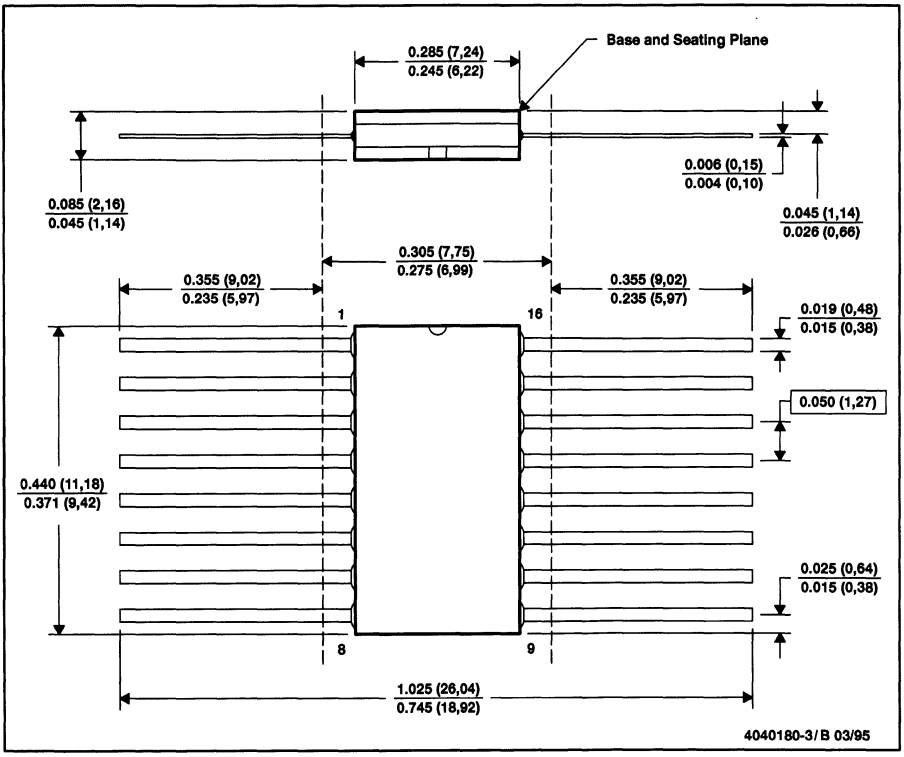
MECHANICAL DATA

W (R-GDFP-F14) **CERAMIC DUAL FLATPACK**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

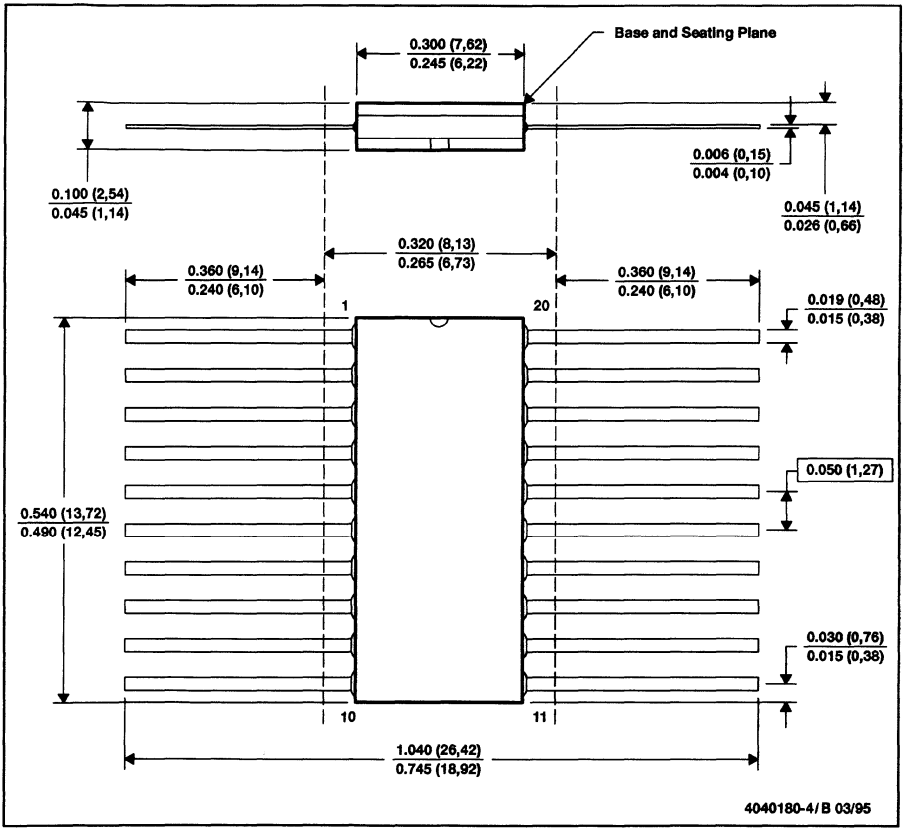
W (R-GDFP-F16) **CERAMIC DUAL FLATPACK**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL-STD-1835 GDFP1-F16 and JEDEC MO-092AC

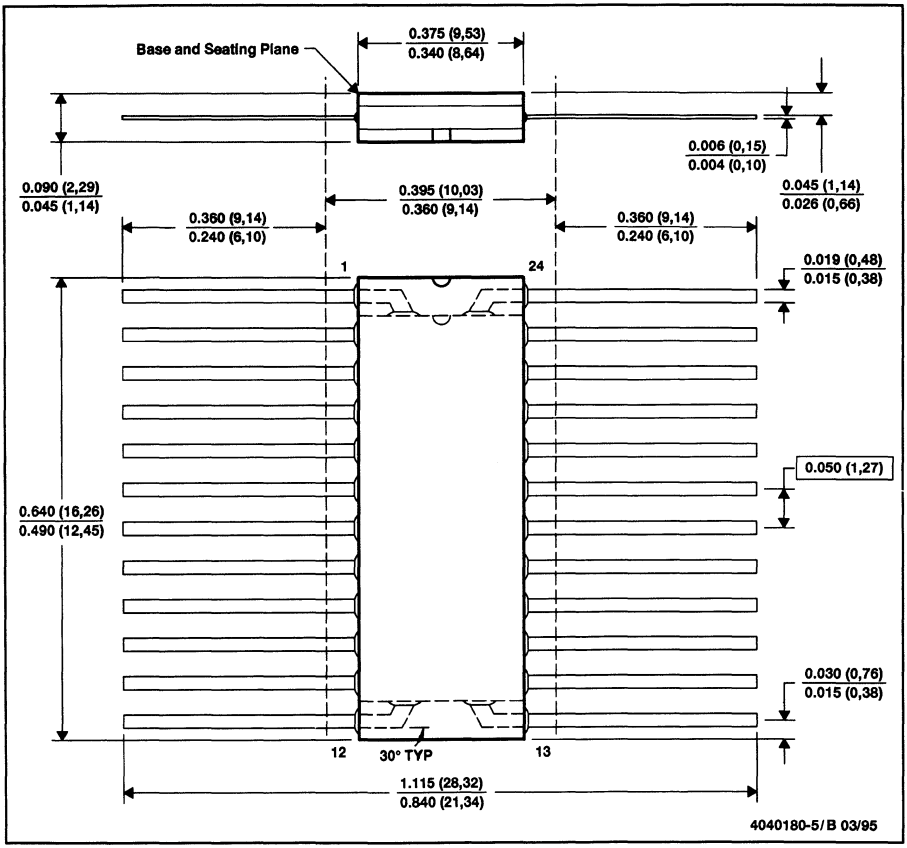
MECHANICAL DATA

W (R-GDFP-F20) **CERAMIC DUAL FLATPACK**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL-STD-1835 GDFP2-F20

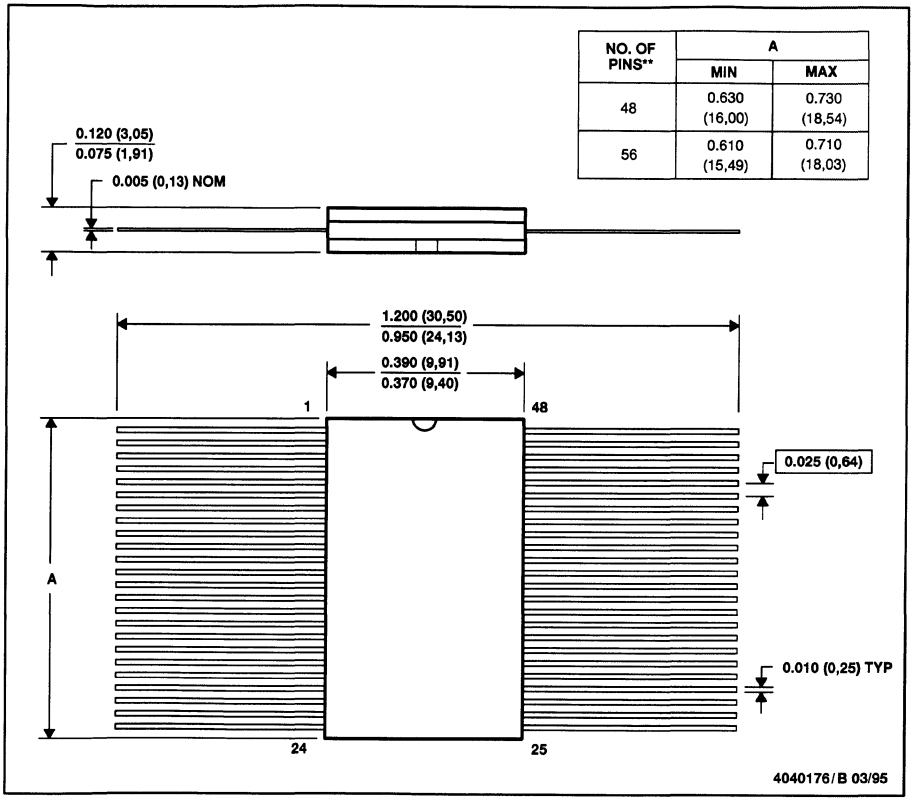
W (R-GDFP-F24) **CERAMIC DUAL FLATPACK**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
E. Index point is provided on cap for terminal identification only.

WD (R-GDFP-F)** **CERAMIC DUAL FLATPACK**

48 PIN SHOWN



NO. OF PINS**	A	
	MIN	MAX
48	0.630 (16,00)	0.730 (18,54)
56	0.610 (15,49)	0.710 (18,03)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for pin identification only
E. Falls within MIL-STD-1835: GDFP1-F48 and JEDEC MO-146AA
GDFP1-F56 and JEDEC MO-146AB

Notes

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Printed by Staples Printers, Rochester, ME2 4LT. England

 Printed in UK

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